TEXAS INSTRUMENTS

1992 LINEAR DESIGN SEMINAR

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Texas Instruments

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Signal Conditioning

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Contents Section 1

1. Introduction

1.1. Signal Conditioning System

This section of the seminar will discuss some of Texas Instruments high performance linear signal conditioning products available today.

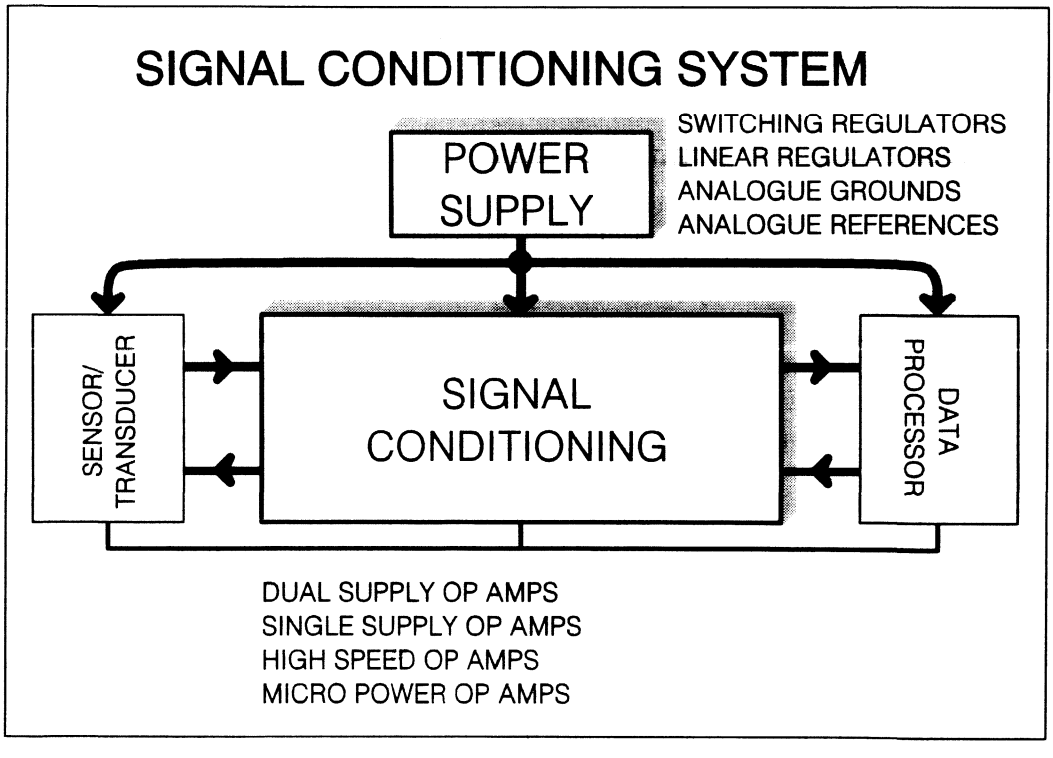


Figure 1.1 Signal conditioning system

Designing both Analogue and Digital systems entail some consideration of the supplies required and used. So when considering a whole signal conditioning system, be it just analogue or be it with analogue preconditioning and digital processing of the data fedback from the sensors careful thought must be given the power supply used , as well as to the op amps used.

Op amps will normally fall into two simple fundamental categories, although devices that fit into the same category may vary enormously in other parameters. The simplest category is whether or not they

can function from a single supply. This quite often differentiates between the two forms of op amps. These categories can then be further split, with high speed op amps fitting with the dual supply op amps, while micro-power op amps fit with the single supply op amps.

Voltage Regulators will also normally fit into two basic categories: Switching regulators and Linear regulators.

Switching regulators come into their own when dealing with either large drop-out voltages (the voltage drop between the input and output), large output currents or where the output voltage must be increased above the input voltage.

Linear regulators are normally much easier to design and use as well as being less noisy. There are however different forms of Linear regulators;- **serial** and **shunt** regulators. The **serial** regulator acts as a variable resistor between the input and output; the resistance will decrease as the output current increases. A **shunt** regulator also works as a variable resistor, this time the variable resistor is between the output and ground with a fixed resistor between the input and the output. As the output current increases, the variable resistor increases shunting less current to ground.

1.2. Designing the Right Op Amp

Texas Instruments is and will continue to be a leading supplier of Cost Effective Performance operational amplifiers. To maintain this position, performance products must be developed which satisfy the demands of both the system design engineers and the end equipment. Texas Instruments must therefore understand exactly what these requirements are.

To be able to provide the Right op amps for the market place, any company must have a clear understanding of 'The Total Need'. This understanding must reach beyond the 'Quest for the Ideal op amp' - many other factors need to be considered.

Texas Instruments has identified the following areas as being crucial in the development and supply of performance amplifiers;

1) New Technologies

It is essential for design engineers to be able to use the most advanced and suitable technologies to enable the development of performance products. Skilled designers can only do so much - eventually the actual technology becomes the limiting factor. Throughout Texas Instruments' history it has placed great emphasis into developing leading technologies to enable the production of performance products. Texas Instruments is the industry's leading supplier of products designed using Bifet and LinCMOS™ processes. Excalibur, Texas Instruments' new complementary Bipolar/Bifet technology, has enabled the development of a number of precision, high speed, low power op amps - all of which are proving extremely popular in a wide range of different applications. The development of advanced, quality, performance technologies is one of Texas Instruments' strengths and these skills are being put to good use in all areas of linear products. These technologies will be discussed in this seminar.

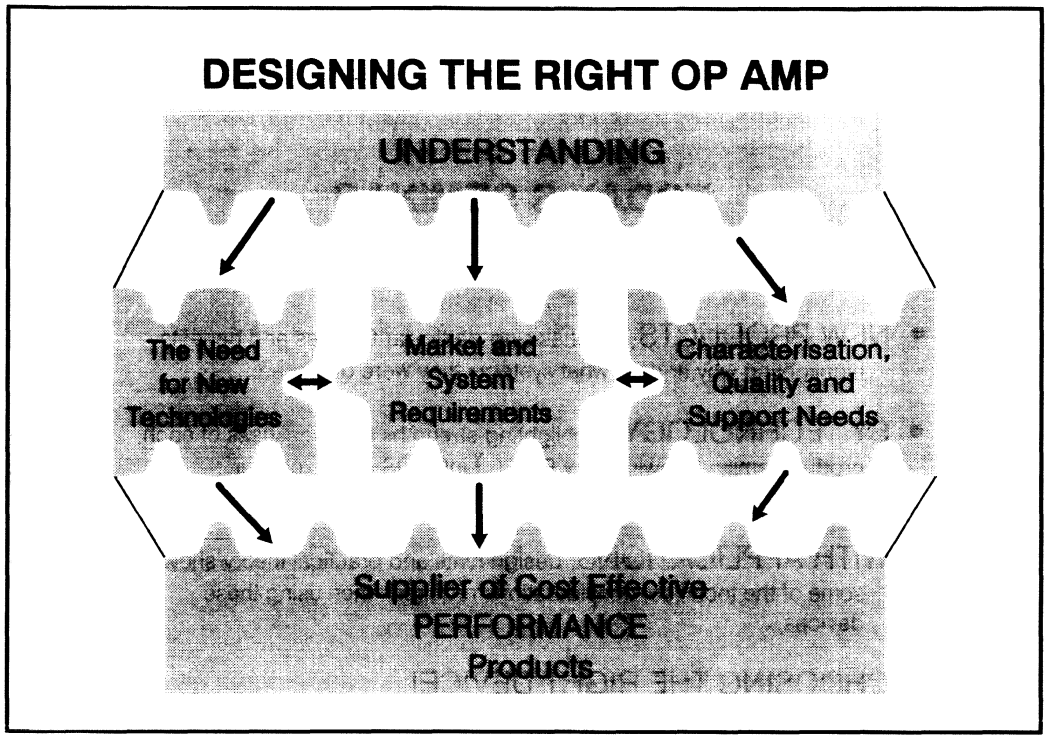


Figure 1.2 - Designing The Right Op Amp

2) Market and System Understanding

Texas Instruments focuses its products at particular applications and market segments. By understanding actual system requirements is it possible to provide devices that are highly suited to actual end equipment. Texas Instruments has op amps ideally suited to applications in the following areas;- Automotive, Telecom, Instrumentation, Test and Measurement, Industrial Control, Audio and many others. By understanding the demands of these systems, an op amp's parameters can be fully optimised.

3) Characterisation and Design Support Material

Having an operational amplifier that performs well is not enough - it must also be easy to use and its particular characteristics well understood. Texas Instruments, like many other companies, is putting significant effort into giving excellent support and design information. Characterisation data has meant that the datasheet for a single op amp is now normally longer than 30 pages!

To ease system design and enable circuit simulation, Texas Instruments has generated **Spice Macro-Models** for virtually all of its op amps and comparators.

1.3. Today's Seminar

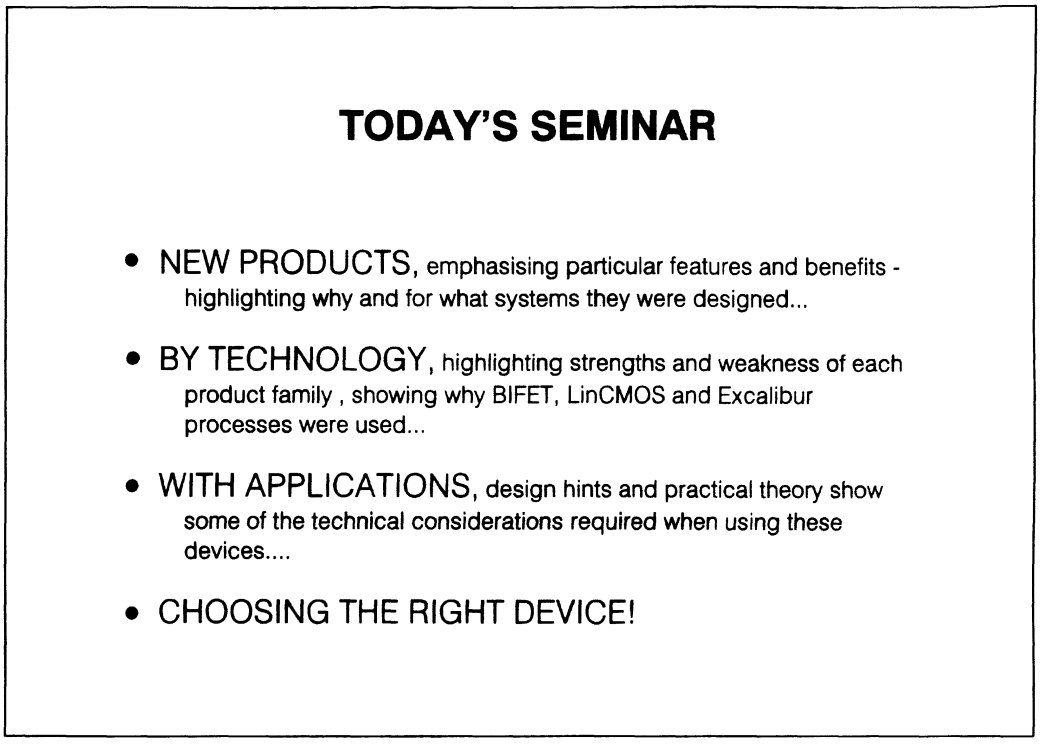


Figure 1.3 Today's seminar

The signal conditioning section aims to show the benefits of Texas Instruments' range of high performance devices and how the technology used adds to the capabilities of the devices.

2. Power Supplies

2.1. Power Supply Requirements

When designing the power supply for any system, consideration needs to be given on the number of supply voltages required, the power handling capabilities of the supplies as well as the ultimate generator of the input.

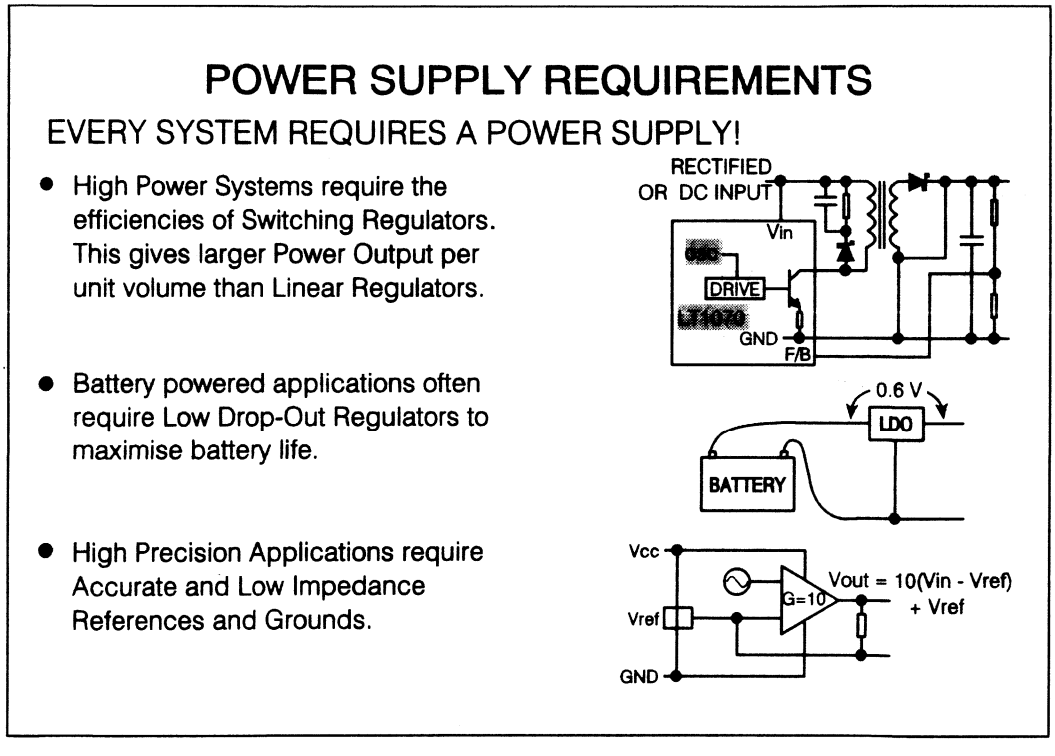


Figure 1.4 Power supply requirements

Switching regulators allow larger output currents and output powers than linear regulators. This is due to switching regulators making use of the energy stored in the magnetic fields of the inductors, as well as its switches being either hard on or totally off. The latter point greatly reduces the power wasted within the switching element. This allows switching regulators to deal drop-out voltages greater than 30 V whilst passing currents greater than several amperes.

This means that switching regulators can provide much larger levels of power per unit area than linear regulators.

The negative sides of switching regulators are their requirement for inductors and their magnetic fields, and by their very nature they produce a much more noisy output voltage.

When dealing with smaller input voltages and output currents, Low Drop-Out Linear voltage regulators make much better use of the board space area. The advantage of low drop-out regulators is that their drop-out voltage is very much smaller than the original linear voltage regulators. The low drop-out voltage of these regulators can be used to maximise the lifetime of battery powered applications.

Single supply applications will normally require an extra low impedance voltage node that is used to refer output voltages to, or to bias the input stage to. For single supply op amps to work properly in inverting amplifier configurations their inputs must be raised above ground.

2.2.Switching Regulators

2.2.1. Texas Instruments Switching Regulators

One early monolithic form of switching regulator to be released onto the market was Texas Instruments' TL497. This is a simple and easy to design-with Pulse Rate Modulation (PRM) Controller Integrated Circuit, and as a result, has proved very successful. It however suffers from the problem, common to all PRM controllers, of enormous variation in oscillation frequency with load. At light loads the frequency can drop into the audible frequency range. More modern Switching Regulators use Pulse Width Modulation (PWM) Control.

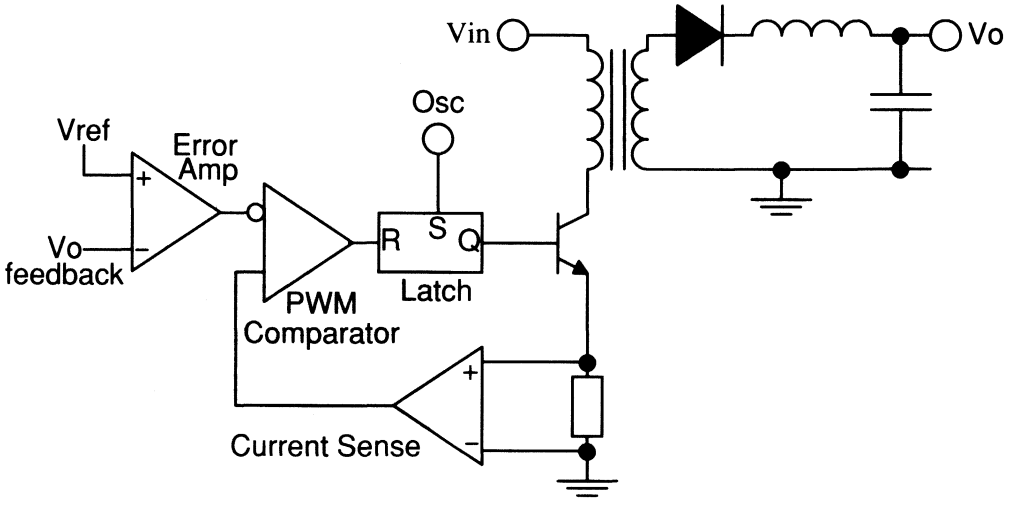
One of the first monolithic switching regulators to be released onto the market that used PWM was Silicon General's SG3524 family. Texas Instruments introduced its own version of that popular regulator along with its own TL493/4/5 family. These allowed higher switching frequencies and greater drive capabilities. The TL493/4/5 family was superseded by the TL594/5 family of switching regulators which had the added feature of undervoltage lockout.

Both families could be used to switch the load inductor (transformer) directly, or for heavier loads provide pre-drive for power switches. The TL594/5 family has recently had a new addition with the TL598. This uses two Totem-Pole output stages, whereas the previous members had two un-configured output stages. This enables the TL598 to act as a better pre-driver for the power switches.

2.2.2. Current Mode Control

A more recent innovation in Switching regulators is to use current mode control. This still uses PWM techniques, but now the current flowing through the power switch is also monitored and used to modulate the on-time of the switching regulator. This in effect uses a dual control loop, with the inner loop being the current control. The current flowing from the input through the inductor and the output power transistor, when it is switched on, is converted to a voltage by a low valued sense resistor. This provides direct feedback of the current flowing through the inductor.

This signal is fedback to the PWM comparator, where it is measured against the error signal generated by the outer loop. This loop compares a fraction of the output voltage to an internal reference and provides an error signal in proportion to the difference between the desired and actual output voltage. This error signal is the same as is used in normal voltage mode converters.



In this way, the drive to the output switch from the latched flip-flop is turned off when the sensed inductor current reaches the limit set by the V_{ERROR} signal. Hence the error signal controls the inductor current directly to provide inherent pulse by pulse current limiting.

Benefits of current mode control

Direct sensing of load current - Because the load current is measured directly and not just the load voltage, the current mode controller can respond very quickly to variations in the load. This is also true for changes in the input voltage.

Current compared to error signal - Measuring the current directly shuts off the output in a short circuit condition or if the inductor saturates.

Parallel Operation - Since both current and voltage are monitored, power is shared equally between any number of modules operating in parallel. This makes efficient use of a series of devices operating in parallel to provide additional current capacity.

Feed Forward - Variations in the line voltage are automatically corrected for by the current sense amplifier, as explained above. Therefore the dynamic range of the error amplifier is used to maximum effect to measure load variations.

2.2.3. High Efficiency Switching Regulator

One of the most recent additions to Texas Instruments' range of Switching regulators is LT1070 family of Current Mode Control Switching Regulators. Each member of the family includes the Power Switch, Oscillator, Accurate Voltage Reference and Frequency Compensation within the Monolithic Integrated Circuit.

All these features have helped this device to overcome the difficulties in designing Switching regulators and their large discrete component count, giving it the ease of use of a linear voltage regulator.

HIGH EFFICIENCY SWITCHING REGULATOR

LT1070/1/2 INTEGRATED CURRENT MODE CONTROLLERS

- Complete Integrated Switching Regulators with:
  - Oscillator . . . 40 kHz
  - Power Switch
  - Integrated 1.25 V Reference
- High Output Currents
  - LT1070 . . . . . 5 A
  - LT1071 . . . . . 2.5 A
  - LT1072 . . . . . 1.2 A
- Self-Protected Against Overloads
- Low Shutdown-Mode Supply Currents . . . . 50 μA

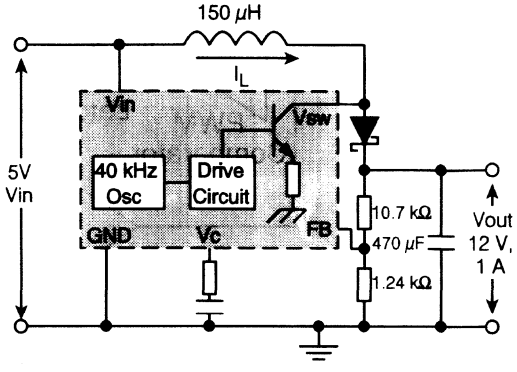


Figure 1.5 High Efficiency Switching Regulators

The LT1070s operate on a wide range input voltages from 3 V to 40 V. The LT1070s requires only 6 mA quiescent operating current, yet is capable of delivering up to 100W to a load without the need for external power devices. An externally generated shutdown signal on the V_C pin, can put the device into a sleepmode where it draws only 50 μA. The low voltage operation and tiny quiescent current allow the LT1072 to be used in battery powered applications.

The only extra components required over a standard linear regulator are 1 inductor and one diode!. The 1.25 V reference (accurate to 2.5%) and 40 kHz oscillator are included within the chip

Boost Converter

Figure 1.5 shows the LT1070 configured as boost converter, that is its output voltage is boosted above that of its input voltage. Its high level of integration makes the complete circuit much easier to design. The device can operate in this configuration with an input as low as 3 V, and an output of up to 50 V. The feedback resistors are chosen to set the feedback voltage to 1.25 V, with a current down the chain of 1 mA. The choice of inductor is a trade off between magnitude and board space. High values give larger power capabilities and lower ripples, but are physically larger and have slower transient response times. The lower values have reduced power and higher ripple but respond to transients more quickly. They can also lead to instability problems when used with Duty Cycles greater than 50%.

One way of choosing the value required is to specify the maximum ripple current, ΔI, in the inductor.

The fundamental equations for a boost converter are:-

Power Switch On					Power Switch Off				
ΔI	=	$V_{in} \cdot t_{on} / L$			$-\Delta I$	=	$(V_{in} - V_{out}) * t_{off} / L$		
Implies, t_{on}	=	$L \Delta I / V_{in}$		2.2.1	Implies t_{off}	=	$L \Delta I / (V_{out} - V_{in})$		2.2.2

Hence, $$t_{on} + t_{off} = L \Delta I \frac{V_{out}}{(V_{out} - V_{in}) V_{in}} = 1/f \qquad 2.2.3$$

So, $$L = \frac{V_{in}(V_{out} - V_{in})}{(\Delta I \, f \, V_{out})} \qquad 2.2.4$$

Choosing a maximum ripple of 0.5 A, and using the other values as shown in figure 1.5,

$$L = \frac{5 (12 - 5)}{(0.5 \, 40 \times 10^3 \, 12)} = 146 \, \mu H$$

The RC network connected to the V_C pin provides loop frequency compensation. This circuit operates at up to 90% efficiency (typical).

2.3. Low Power Low Drop-Out Regulators

Although switching regulators can provide high levels of output power at high efficiencies they will never replace linear regulators in all applications.

The areas that switching regulators fall down are in the noise and the EMI (Electro-Magnetic Interference) they produce. Reducing these effects can be very difficult, and tightening up on legislation on the amount of EMI that systems can produce will stretch some of the present industry standard applications to their limit.

Linear regulators do not however produce high levels of EMI. This is due to the fact they are not continually switching the output current on and off. This also greatly reduces the high frequency noise generated. This can sometimes lead to them being used to clean up the output voltage of a switching regulator.

In the past, all linear regulators were designed with a serial NPN pass transistor. The technologies used were developed to enhance the performance of the NPN transistor at the expense of the PNP transistor. This meant that the NPN transistors were very much faster and had very much higher current gains than their PNP counterparts. So for low noise and good line and load regulation NPN transistors had to be used, but this meant that quite often minimum drop-out voltages of 2 - 3 V had to be allowed for. So a device providing an output current of 1 A had to be capable of withstanding a minimum power dissipation of 2 - 3 W. The drop-out voltages used would normally have to be much larger than this to allow for the poor regulation of the source, which means that the devices had to withstand much larger power dissipation than 2 - 3 W.

The increase of low supply voltage applications and the increase of battery powered applications led to the development of serial voltage regulators that have much lower drop-out voltages. This has also come about with improvements in PNP transistors.

Normal voltage regulators have NPN transistors that require the base drive circuitry to be above the output voltage. It is this fact that increases the drop-out voltage. The Low Drop-out Regulators using PNP transistors have the base drive circuitry below the output voltage, thus allowing a much smaller drop-out voltage.

LOW POWER LOW DROP-OUT REGULATORS

LOW DROP-OUT VREGS IMPROVE SYSTEM EFFICIENCY

- Maximum Drop-Out Voltage of 0.6V at Maximum Specified output current:
  - TL750M . . . . . 750 mA
  - TL750L . . . . . 150 mA
- Low Quiescent Currents (@ Iout = 10 mA)
  - TL750M . . . . . 5 mA
  - TL750L . . . . . 2 mA
- **60 V Load-Dump Protection**
- **TL751 offers Greater Versatility with shutdown Capability.**

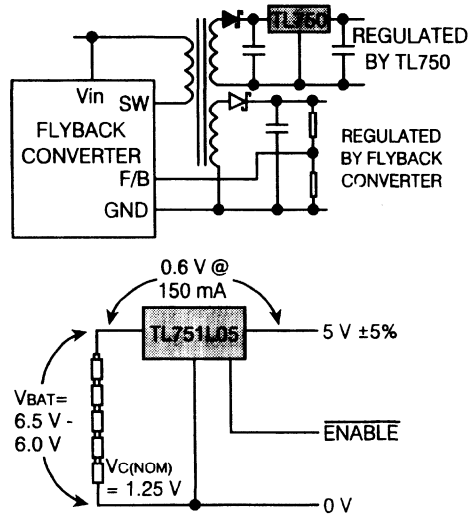


Figure 1.6 Low Power Low Drop-Out Regulators

Texas Instruments released its own family of Low Drop-out voltage regulators in the late eighties. These were aimed primarily at automotive applications, which was one of the driving forces behind low drop-out regulators. This is why the TL750/1L and TL750/1M families have 60 V load-dump protection specifications.

They can however be used in many other applications:-

As stated earlier linear regulators can be used to clean up the noise on the outputs of switching regulators. Low drop-out regulators can be used in multi-output switching regulator systems to provide better regulation on the un-monitored outputs. The low drop-out regulator can withstand very small drop-out voltages across it while still providing good line and load characteristics. The TL750s have a maximum drop-out voltage of 600 mV at their maximum rated output currents.

When used in this way the low drop-out regulators allow wide varying inputs to applied while still providing the output voltage required.

The increase of battery applications has made the low drop-out regulator essential for maximising battery lifetime. All batteries exhibit relatively large output resistances, which increase with battery life span. Low drop-out regulators help to increase the lifetime of the battery by reducing the output impedance of the battery. The Low drop-out regulator's small drop-out voltage adds to this further by allowing greater voltage drops within the battery than what standard serial regulators were capable of.

2.4. Advanced References and Grounds

All high accuracy systems will require some form of reference. This reference will either be on board or may just be there for calibration. External calibration is becoming increasingly expensive, resulting in a larger number of applications using high accuracy voltage and current references.

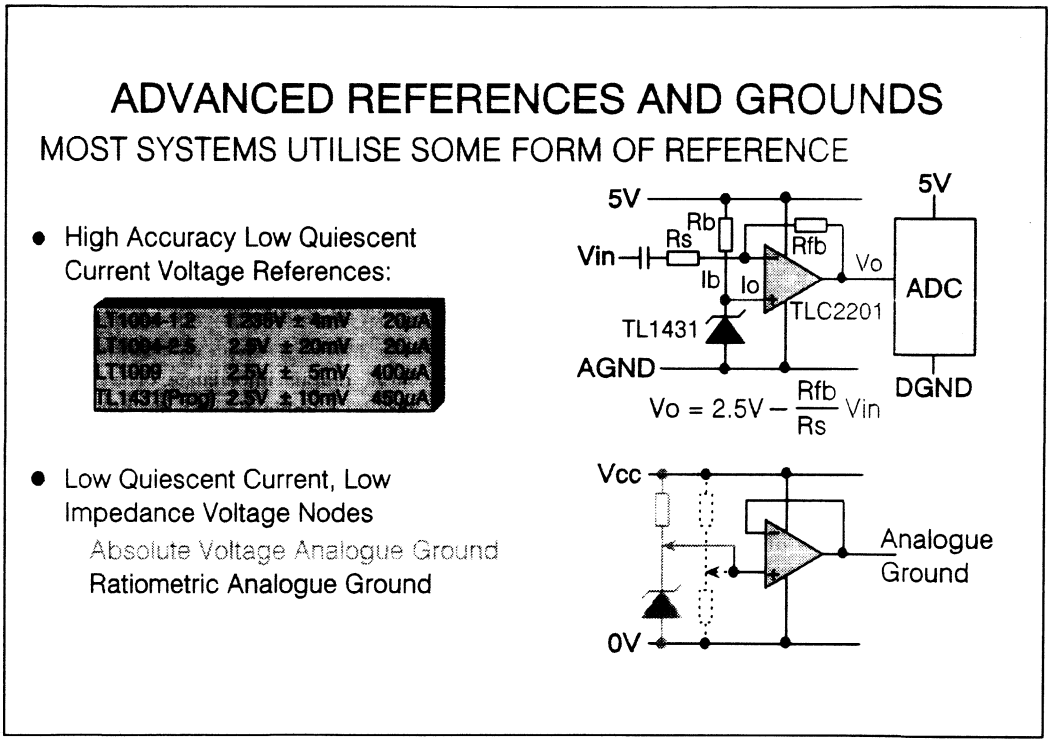


Figure 1.7 Advanced References and Grounds

The actual specifications for the references can differ from one application to another. The figure above shows two possible variations of the voltage reference.

In the first case, only a voltage source is required. This sort of reference crops up quite frequently in single supply applications. To get maximum output swing the non-inverting input of the op amp must

be raised above ground. The reference, a TL1431, is used to pull the non-inverting input above ground. However in this particular application the reference is not being expected to source large amounts of current.

As a result of that last point many of Texas Instruments' advanced references could have been used in this particular application. The tolerances and typical minimum holding currents are specified in the table below:-

Device	Output voltage (V)	Minimum Holding Current	Maximum Shunt Current	Tolerance (%)	Temperature Coefficient
LM385-2.5	2.5 (Typ)	20 µA	20 mA	2	20 PPM/°C
LT1004-1.2	1.235 (Typ)	10 µA		0.8	
LT1004-2.5	2.5 (Typ)	20 µA		1.2	
LT1009	2.5 (Typ)	400 µA		0.2	15 PPM/°C
TL431A	2.5 - 36	400 µA (Typ)	100 mA	1	23 PPM/°C
TL1431	2.5 - 30	450 µA (Typ)		0.4	23 PPM/°C

The TL431A and TL1431 were designed as shunt regulators, but due to their programmability and high accuracy they can be used variable high current references.

In the past a potential divider might have been used to provide the reference, this has an advantage that the non-inverting input would always track the supply voltage. This would help maintain the wide output swing, but could pass noise from the supply onto the non-inverting input of the op amp and through to its output.

Another problem of the resistor divider reference is its large output impedance. The Thevenin equivalent output resistance of the potential divider is the parallel combination of the two resistors forming the divider. In applications requiring low power this equivalent resistance can be about kilo-ohms. The dynamic impedance can be reduced by shunting the output by a capacitor.

One way of improving the dynamic impedance of the resistor divider is to buffer the output with an op amp. This can also offer power savings when used in conjunction with the references. All the references mentioned are basically shunt regulators. The total current supplied to the reference circuit will remain constant, with the current flowing to the reference being modulated by the load's requirements. This means that when supplying currents to highly fluctuating loads the references can waste large amounts of power, due to the reference shunting large amounts of current to ground. Using the op amp to buffer the reference can lead to significant power savings if the op amp has the drive capability required by the load.

2.5. TLE2425/6 - Virtual Ground Generators

The number of systems requiring some form of accurate reference voltage can be quite staggering. Just about all single supply applications require an accurate reference, which will need to be able to supply varying amounts of current.

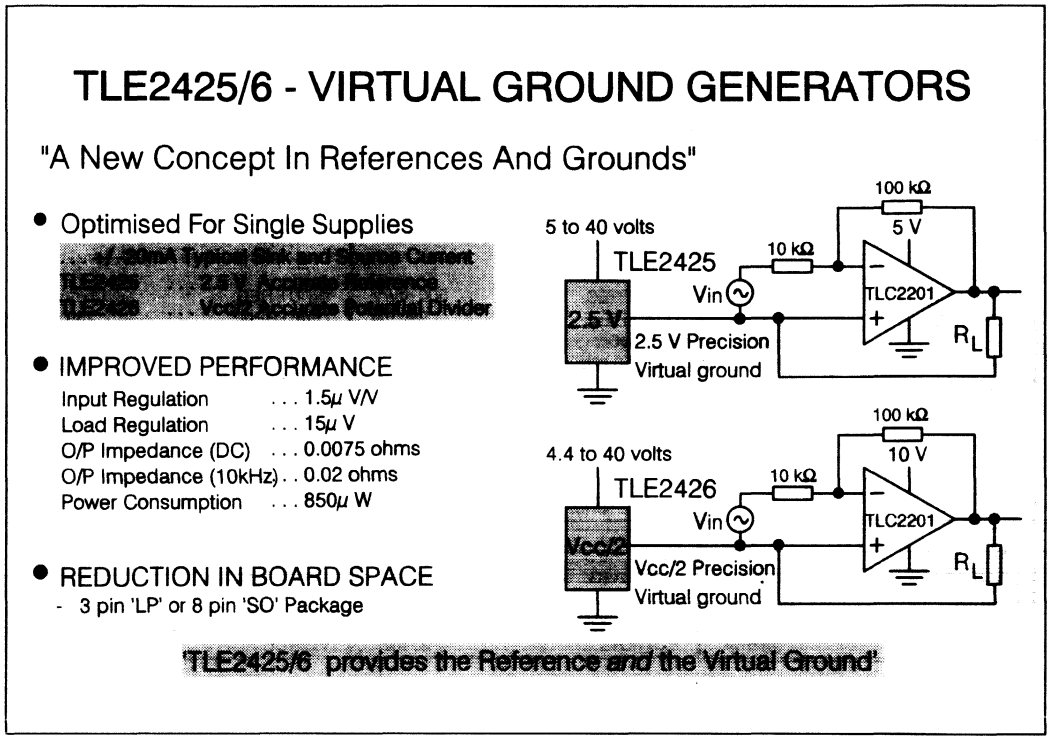


Figure 1.8 Virtual Ground Generators

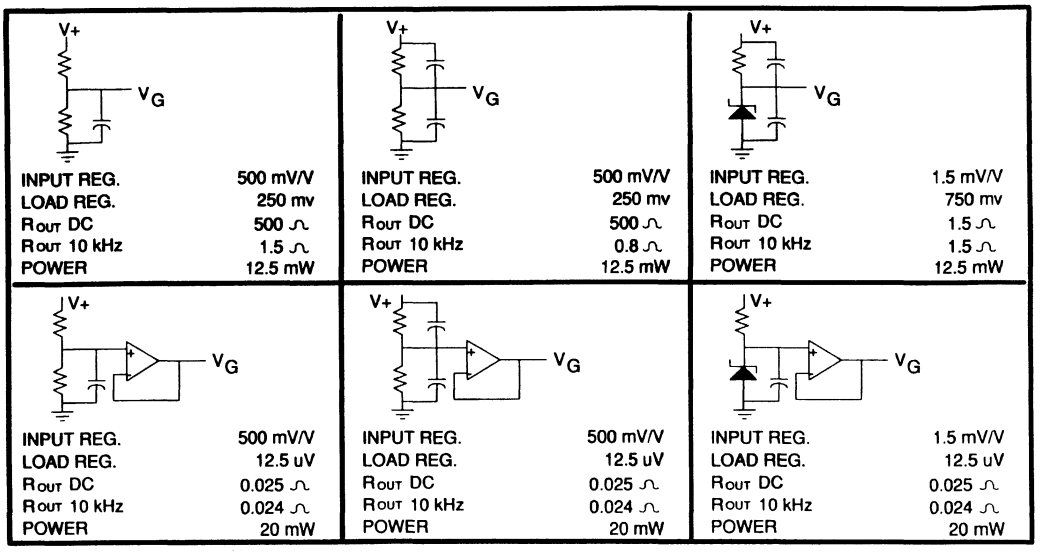
It is for those reasons why Texas Instruments developed the TLE2425 and TLE2426 series of "Analogue Grounds".

The TLE2425 contains an accurate low power 2.5 V reference that is buffered by a low power high output current capability op amp. This makes it ideal for 5 V supplied applications where either a low power reference is required, or a low impedance artificial ground is required. The TLE2425 requires only 170 μA of quiescent current while being capable of sourcing more than 20 mA of output current. No other integrated circuit can match this performance, and even discrete arrangements find it virtually impossible to meet the output current to quiescent current ratio, especially when the TLE2425 has been designed to drive capacitors of up to 100s of microfarads. No op amp can drive these orders of capacitors over this range without extensive compensation.

The TLE2426 is very similar to the TLE2425 except that it contains a high impedance potential divider. This provides an "Analogue Ground" equal to half the voltage applied across its IN and COMMON terminals. This makes it particular useful when trying to maximise the output swing of dual supply op amps (see later on for definition of dual supply op amps), whose outputs have not been designed to swing to either rail, but about the middle of the supplies.

The diagram below shows many different ways of providing the functions that the TLE2425 and TLE2426 provide in one integrated circuit.

EXISTING SOLUTIONS



Virtual Grounds For Single Supply Systems

2.6. Unbalanced Supply Cancelling

The TLE2426 can introduce great benefits when used as an analogue ground in an unbalanced supply system.

All op amps are 5 terminal devices; the positive and negative (ground) supply pins, the two inputs and the output. The op amp itself has no ground pin and therefore has no direct relation to the system ground, but only to half of the total supply voltage. Most op amps have been designed for their inputs to work in the middle of the supplies, hence their datasheet parameters tested and specified at mid-supply. So when operating op amps with unbalanced supplies the actual specified performance can differ from what is actually achieved in the application. Typical errors seen will be increased common-mode errors, loss of symmetry in output swing or even clipping.

The TLE2426 by halving the total power supply can be used as a half supply analogue ground. Referring both the inputs and loads to this ground reduces the common mode errors as well as the loss of symmetry in output swing.

An unbalanced supply will have one supply greater than the other, in the figure shown below the positive supply is at 5 V while the negative supply is at -12 V. This means that any op amp connected to these supplies whose input is referred to ground will have a much greater negative output swings

than on the positive. This can quite easily lead to clipping on positive excursions of the waveform, as shown in the figure.

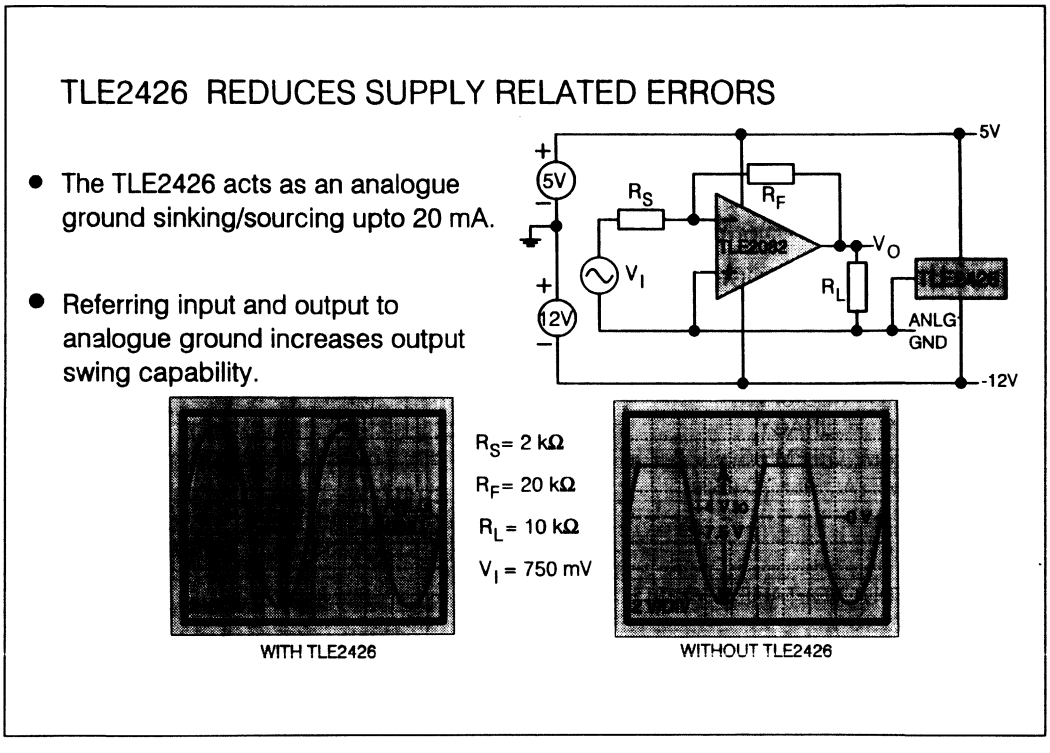


Figure 1.9 Unbalance Supply Cancelling

The use of the TLE2426 in providing a true low impedance ground allows both the inputs and outputs of the op amp to be referred to the new ground, and provide a symmetrical un-distorted waveform.

A potential divider could have been used to bias one or both of the inputs, which requires ac. coupling, but the input signal generator and output load would still be connected to ground. The loading of the op amp would still be unbalanced, with the positive excursions going up to 4 V and the negative excursions going down to -11 V, resulting in the op amp having to supply approximately 3 times the current to negative swings than positive swings. This itself can lead to distortion when driving heavier loads. The TLE2082 is specified to drive a minimum of 30 mA, resulting in this having little effect on its performance.

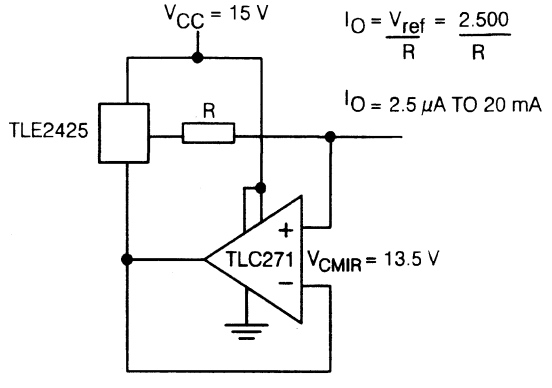
The TLE2426 can have further applications with dual supply rails where the application might call for isolation from other grounds.

2.7. TLE2425 Current Source

Due to its versatility, the applications of the TLE2425 are numerous. Although being ideal for maximising the performance of single rail 5 V applications, its accuracy and high output current make it well suited to function as a high performance current source

MORE THAN 3 DECADE HIGH OUTPUT CURRENT SOURCE

- OUTPUT CURRENT PROGRAMMED OVER 1000 TO 1 RANGE
- UNTRIMMED PRECISION:-
  - 0.75% ACURACY
  - 70 PPM/°C TEMP Co.
  - (R = METAL FILM, 0.25%)
- HIGH OUTPUT VOLTAGE SWING
  - 11 V to 0 V



TLE2425 : Enables precision and wide ouptut current range

TLC271 : CMIR includes GND low power consumption

TLE2425 Current Source

The usual principles of making a current source are to fix a voltage across a resistor and either mirror that current or to buffer it. This can have problems in referencing the current source and finding op amps that can deliver the currents sometimes required.

The diagram above shows one simple way of doing this. The TLE2425 with its accurate reference and high output drive capability greatly simplifies the design.

The minimum drop-out voltage of the TLE2425 is 1.5 V, placing the maximum voltage on the out of the TLE2425 at 13.5 V. This means that the maximum voltage on the common terminal of the TLE2425 will be 11 V. The feedback loop around the op amp means that the voltage at the inputs of the op amp will also be at 11 V.

The common mode input voltage range (V_{CMIR}) of the TLC271 extends from ground up to 1.5V from the positive supply. Which means for a 15 V, the voltage swing of the current source is well within the

common mode input range of the TLC271. To minimise the quiescent current of the whole current source, the TLC271 has its bias select pin (8) tied to the positive rail.

The accuracy of the system is limited by the accuracy of resistor, and by the input offset voltage of the TLC271 which will also effected by its common mode rejection ratio. Both of the limitations due to the TLC271 could be improved by using the TLE2021, this however would limit the lower voltage range of the current source.

3. Bifet Operational Amplifiers

3.1. Bifet Operational Amplifiers Overview

Bifet operational amplifiers were first introduced in the early 1970's and today they are among the most common op amp type. They are essentially bipolar op amps that use high voltage p-channel JFETs on the input.

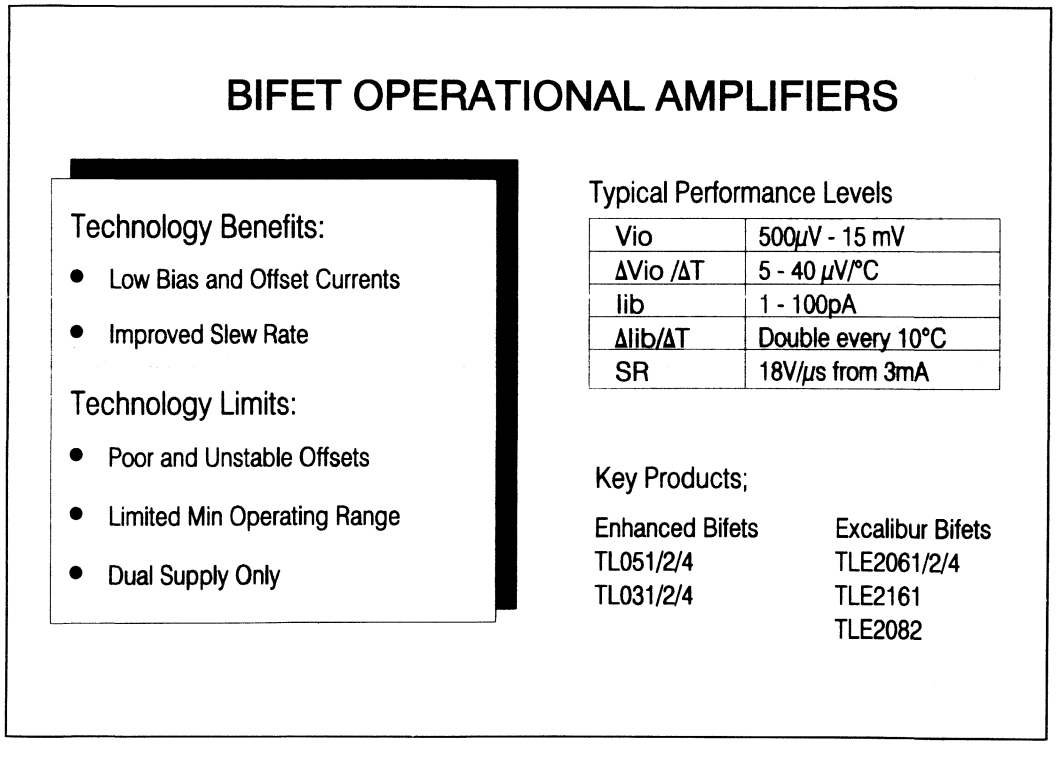


Figure 1.10 Bifet Operational Amplifiers

These JFETs have a number of advantages and disadvantages;

3.1.1. BIFET Advantages

High input impedance and low bias currents;

The inherent high input impedance of JFET transistors enables op amps with extremely low bias currents. This brings a number of significant advantages to many applications including integrators, sample and holds, and filter type circuits. Care must be taken however as the bias currents will double for every 10°C increase in temperature. At high temperatures a Bifet's bias current may be higher than some bipolar circuits!

Improved AC performance;

When JFETs are used in an op amp's input, the resulting gain of the op amp's differential input stage is significantly reduced. The amplifier's internal compensation capacitor (which provides device stability) can therefore also be reduced and the result is a significant increase in slew rate. For the same supply current a Bifet op amp can easily have up to a five fold increase in slew rate over a bipolar equivalent.

Reduced Input Noise Current;

A benefit of both CMOS and Bifet operational amplifiers are their improved noise current. This is very important when interfacing to sources of a very high impedance. The input noise current is determined by the shot noise of the gate current - this is very low at 25°C.

3.1.2. BIFET Disadvantages

Poor and unstable offset voltages;

Bifet designs have typically far greater offset voltages than their bipolar equivalents. Their less uniform DC characteristics and poor thermal drift make the essential accurate matching of the input transistors very difficult. They are also very prone to the induced stresses of plastic packages - real precision Bifets are normally only available in ceramic, metal can or hybrid packages.

Typical standard selection Bifets in a plastic package may only achieve 2 mV - 3 mV offset voltage and their stability will be poor. Newer designs, such as the TL051 and TL031 series, discussed later, have improved processing and design techniques to achieve new levels of precision and stability.

Poorer CMRR, PSRR and Open Loop Gain specifications;

The reduced gain of the Bifets input stage that enables the improved ac. performance also causes a reduction in various gain parameters of the device. This further reduces the suitability of the designs in precision applications.

Increased Noise Voltage;

A FET input stage will have a higher noise voltage and higher 1/f frequency when compared to bipolar devices.

3.1.3. Texas Instruments' range of Bifets

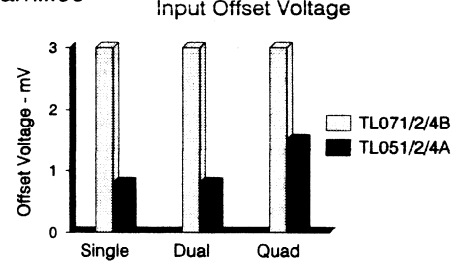
TL051/2/4 Family	TL071/2/4 Family	LF411/2
TL031/2/4 Family	TL061/2/4 Family	LF441/2
TLE2061/2/4 Family	TL081/2/4 Family	LF347/9
TLE2161		LF353
TLE2082		

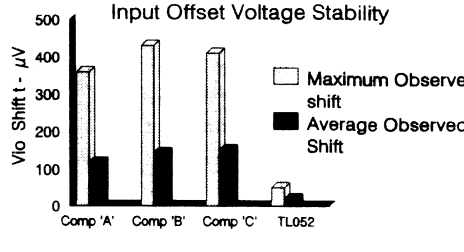
3.2. TL05X and TL03X Enhanced Bifet Series

Although extremely popular, one of the key factors that has restricted the use of Bifets in more applications is their relatively poor and unstable offsets. Achieving precision Bifets in plastic packages proved difficult and large yield loss meant relatively high prices. Realising this as a problem that should be addressed, Texas Instruments put considerable effort into developing a new family of cost effective, precise and stable Bifets. The result is the **TL051/2/4 and TL031/2/4** family of **Enhanced Bifets.**

Precision Alternative to TL07X and TL06X Families

- Lower Offsets with Improved Stability;
  - 800 μV Vio max
  - 6 μV/°C and 4nV/month drift
- Good AC Performance; 15V/μ s
- Improved Characterisation
  - Guaranteed Vio Drift
  - Guaranteed Noise
  - +/-5V and +/-15V Characterised





TL05X and TL03X Enhanced Bifets

New design, layout and processing techniques made it possible to produce the high level of performance as shown in the graphs above. Two selections of each device are available with the 'A' grade part achieving a maximum offset voltage of just **800 µV**. The stability is also greatly improved and maximum values are also given.

Almost all the original products are still being used with their initial datasheets and these new designs benefit further from considerable characterisation data. The parts are fully specified at both +/-5V and +/-15V supply voltages with maximum values given for parameters such as noise.

Many applications are benefiting from the increased DC precision of these parts. Applications such as Audio, which were previously been seen as having purely ac demands, are using these parts extensively. More typical applications in control loop systems or filter circuits are also seeing the benefits.

Both designs are improved alternatives to the industry standard TL07X and TL06X families (TL05X is an improved version of the TL07X, TL03X is an enhancement of the TL06X), and are specified over a 'C', 'I' and 'M' temperature ranges.

3.3. Low Droop Precision Peak Detector

Basic Peak Detector

Peak detectors measure the maximum value of a fluctuating voltage. A basic peak detector consists of an ideal diode through which a capacitor is charged to a voltage equal to the peak input voltage. As long as the peak input voltage is higher than the stored voltage on the capacitor, the diode conducts and charges the capacitor. When the input voltage decreases, the diode turns off, and the maximum input peak voltage is stored on the capacitor. To measure a new and lower peak value, the peak-hold circuit must be reset by a switch discharging the capacitor. If defined slopes of the peak detector are required, a resistor in series with the capacitor limits the charge current, and a bleed resistor across the capacitor ensures a defined discharge rate.

A near ideal diode with no voltage drop is implemented using a real diode in the feedback loop of an op amp. To avoid unwanted discharge of the capacitor from loading, this is normally buffered with an op amp with low input bias current.

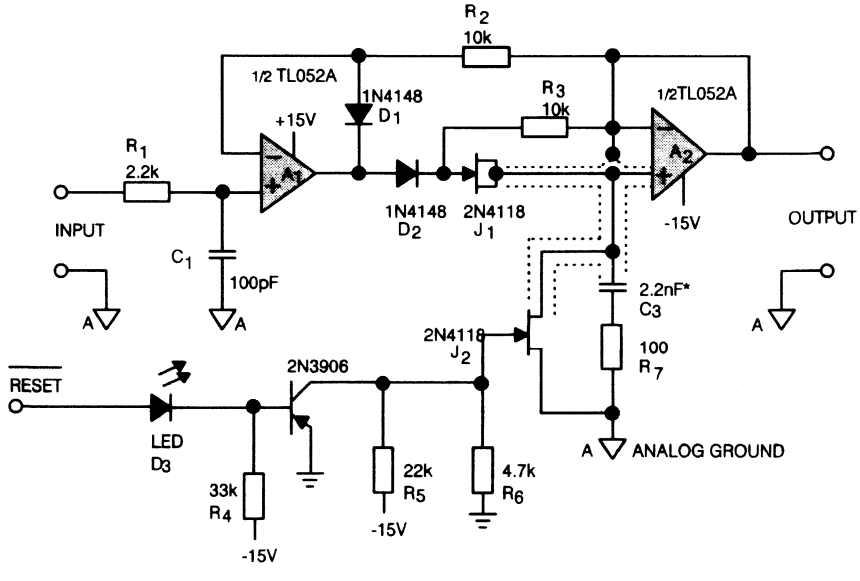
Improved Peak Detector

The shown low droop precision positive peak detector uses a TL052A dual JFET-input op amp to achieve very low DC errors and good holding characteristics. A bootstrapped diode circuit prolongs the holding time. The reset circuit is provided with a simple 5V logic interface. With A_1 configured as a non-inverting follower peak detector, this circuit stores the input voltage's positive peak across C_3. A_2 buffers the output. Note that leakage of the buffer op amp input, charging diode J_1, discharging switch J_2, and storage capacitor C_3, are all potential problem areas when accurate peak voltage levels have to be stored for long time periods.

Circuit Features

The actual circuit includes several features that minimise such leakage. J_1 is a low leakage 2N4118 n-channel JFET, that serves as a diode. Its small leakage is further reduced by minimising the voltage across it i.e. C_3 charges through D_2 and J_1, but because R_3 provides J_1 with a bootstrapped version of C_3's voltage, only D_2 sees a reverse voltage, maintaining the voltage across J_1 at the millivolt level resulting from D_2's leakage current through R_3. As the discharge switch's leakage current also

represents a main leakage path for C_3 an n-channel JFET device with a low leakage off-state and low on-state impedance is selected for J_2.



Low Droop Precision Peak Detector

The storage capacitor needs to be a low leakage type with a low dielectric absorption specification to prevent recovery errors in the stored voltage. Polystyrene, polypropylene or Teflon are the most suitable dielectrics for this application. The above features used to reduce the leakage of C_3 place the majority of the leakage to come from the buffer op amp's input bias current. TL052A has a maximum input bias current of 200 pA at 25°C. For a 2.2 nF capacitor, this leakage level leads to a maximum output voltage decay error given by:

$$\frac{dV}{dt} = \frac{I_{leakage}}{C_3} = 91\ \mu V / ms$$

Because of the overall feedback loop, the circuit achieves a high DC accuracy. A_2's offset and drift errors are servoed out in the peak sample period but do appear in the peak-hold mode. E.g. A_1 determines the peak output offset error in the acquisition period and A_2 in the hold mode. Consequently, DC precision op amps are required for both A_1 and A_2. As a dual op amp is more likely to have a closer offset matching, the output error due to offset shift between the peak sample and peak hold mode is reduced. TL052A has a 800 µV maximum offset voltage at 25°C.

Design Details

The circuit has an inherent potential to detect unwanted transient peaks, which simply lock out subsequent desired peaks. This characteristic justifies a low-pass filter formed by R_1 and C_1 to remove fast erroneous glitches on the input. The chosen time constant, R_1C_1 = 220 ns should not have a major impact on the peak detector's speed. The rate of the voltage rise across C_3 is either,

1. $\frac{I_{max}}{C_3}$ (where I_{max} is A_1's short-circuit output current) or,

2. The slew rate of A_1,

whichever is smaller. With TL052A's 50 mA typical short-circuit current and C_3 = 2.2 nF a maximum voltage rise of,

$$\frac{50mA}{2.2nF} = 22.7V/\mu s ;$$

can be calculated. This matches well with the op amp's specified 20.7V/ms slew rate. A high value of C_3 minimises error due to parasitic leakage. Diode D_1 clamps the output voltage of A_1 to (V_{in} - V_{D1}) to improve speed and to limit the reverse bias voltage of D_2. If D_1 is conducting under negative input conditions, R_2 ensures that the voltage value held on the capacitor C_3 is still present on the output of the peak detector. To ensure correct and stable operation, the maximum input frequency should be much lower than,

$$\frac{1}{2\pi R_3 C_{D2}};$$

where C_{D2} is the shunt capacitance of D_2. If required a capacitor can be placed across A_1 to optimise stability due to the load effect of C_3. Adjust this capacitor for minimum settling time. The circuit can be modified to capture negative peak values by reversing D_1, D_2 and substituting p-channel JFETs for J_1 and J_2. These alterations need however a modified reset circuit.

Proposed Improvements and Alterations

Replacing A_1 with a wider bandwidth TLE2141 improves speed and settling time. For low supply operation, an improved accuracy can be achieved by replacing A_1 and A_2 with the dual TLC2202 op amp offering much lower input bias current and lower offset voltage. However, speed has to be compromised.

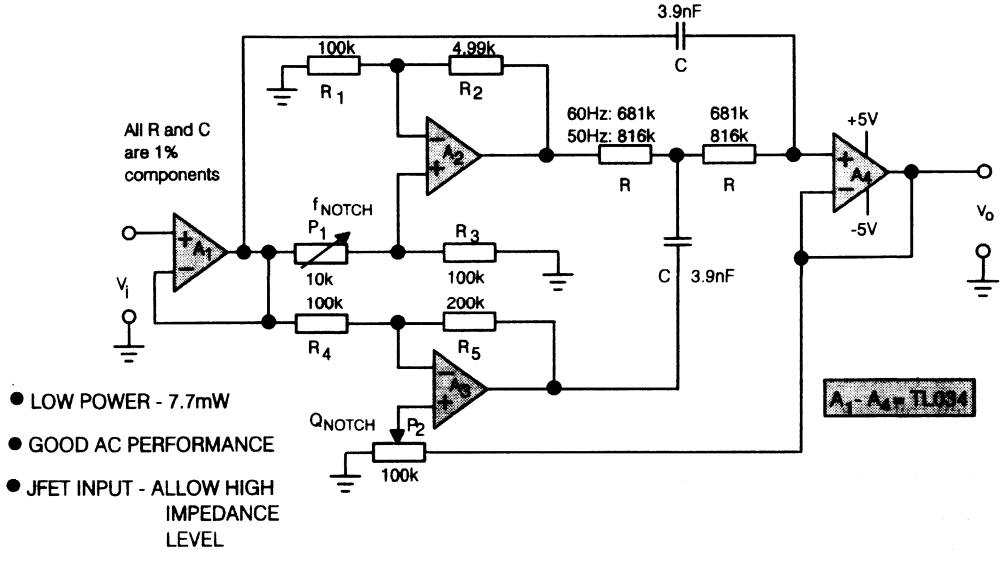
3.4. High-Q Active Notch Filter Removes Hum

What is a Hum Notch Filter?

A frequent problem when measuring signals from sensors is the presence of 50 Hz or 60 Hz mains hum in the signal. In severe cases the interference can completely obliterate the signal of interest. When different signal conditioning amplifiers with high common mode rejection ratios fail to solve the problem or where they are not used, filter techniques are often employed.

A Notch or Band-Stop filter in the signal path - tuned to the hum frequency - effectively reduces or eliminates 50 Hz or 60 Hz interference. Such a filter must have a linear phase response outside the notch region to avoid distortion of the desired signal. This is particularly important where ac-signals,

such as electro-physiological parameters are measured. The shown high-Q tuned active notch filter implementation uses a quad Enhanced Bifet op amp, the TL034, and has a minimum phase distortion.



High-Q Active Notch Filter Removes Hum

Basic Hum Notch Filter

Traditional, simple band-stop filters using only a single op amp configured for a parallel-T Notch Filter have the following disadvantages:

1. Even accurate components, say 1%, still give a worst case variation in the notch frequency of a few percent. This variation from the ideal frequency, combined with a deep notch with high-Q, easily results in a filter which is not tuned for the right frequency at the deepest part of the notch. Ageing and temperature drift of filter components cause similar problems. If the notch frequency differs - say 2-3% from the theoretical value - due to component tolerances lower hum rejection can be expected. A maximum attenuation of 20-30 times compared with the desired signal can be achieved nearly independent of the chosen Q value for the notch filter.

2. Trimming of the filter's notch frequency to match the hum frequency is not a trivial task with a simple parallel-T active notch filter as the notch frequency and filter Q usually interact.

High-Q Tuned Hum Notch Filter

The shown Bridged-T active notch filter configuration overcomes problem 1. and 2. It features independent tuning of the notch frequency, f_{notch} and the notch depth Q_{notch}. Initial trimming of f_{notch} with P_1 to match the mains frequency allows the tolerance of the filter determining components to be ignored. Residual component drift will now only cause minimal shift in the filter's notch frequency. Assuming 50ppm/°C drift of R and C over a ±25°C temperature range gives a minimum 50 dB (300 times) hum attenuation compared with the previous discussed 26-30 dB (20-30 times) for the simple parallel-T implementation - a ten fold improvement in terms of hum rejection.

In addition, the filter configuration allows for independent Q_{notch} tuning with P_2 if required. However, a fixed Q_{notch} factor is often desired for simplicity and can be set to a maximum stable value using a fixed resistor for P_2. With the TL034 in the shown configuration a Q_{notch} factor in excess of 1000 can be realised corresponding to more than 63 dB hum rejection when trimmed exactly to 50 Hz or 60 Hz respectively.

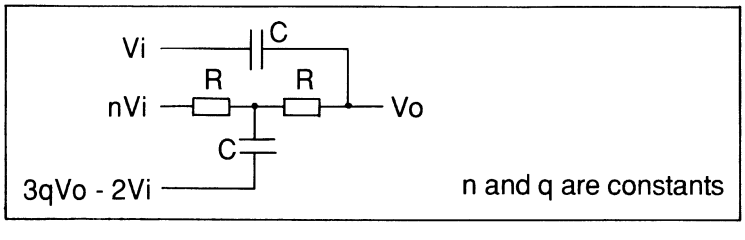
Why use the TL034 Bifet Op Amp?

The Enhanced Bifet TL034 used is an inexpensive op amp ideally suited for these types of applications:

1. Low Power Consumption, 8 mW typical combined with good ac-performance (2V/µs minimum slew rate and 1 MHz typical unity gain bandwidth) allows use in active filters for portable equipment.
2. The JFET input stage provides low input bias current and low noise current - thereby enabling high impedance components to be used. This is especially important in low frequency active filters, such as in 50 Hz and 60 Hz band-stop filters as the total physical volume can be significantly reduced by employing smaller capacitor values with a corresponding high impedance and insignificant physical size.
3. Low Offset Voltage (800 µV maximum @ 25°C) and stable offset voltage (5 µV/°C and 0.04 nV/month typically) adds little DC error to the signal of interest.

Filter Design Details

Basic RC Bridged-T Active Notch Filter:



Using superposition technique the transfer function can be derived as:

$$V_O = V_i \frac{R\|(\frac{1}{Cs}) + R}{\frac{1}{Cs} + R\|(\frac{1}{Cs}) + R}$$

$$+ nV_i \frac{\frac{1}{Cs} \| (R + \frac{1}{Cs})}{R + \frac{1}{Cs} \| (R + \frac{1}{Cs})} \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}}$$

$$+ (3qV_o - 2V_i) \frac{R \| (R + \frac{1}{Cs})}{\frac{1}{Cs} + R \| (R + \frac{1}{Cs})} \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}};$$

$$V_o = V_i \frac{R^2C^2s^2 + n}{R^2C^2s^2 + 3(1 - q)RCs + 1};$$

$$\boxed{\frac{V_o}{V_i} = \frac{R^2C^2s^2 + n}{R^2C^2s^2 + 3(1 - q)RCs + 1};} \qquad \omega_o = \frac{1}{RC} \Rightarrow$$

$$\boxed{\frac{V_o}{V_i} = \frac{s^2 + n\,\omega_o^2}{s^2 + 3(1 - q)\,\omega_o s + \omega_o^2};}$$

In the actual notch filter shown in this application n and q are implemented as follows:

$$n = (1 + \frac{R_2}{R_1}) \frac{R_3}{P_1 + R_3}; \qquad f_{notch} = f_o \sqrt{n}; \qquad \omega_o = \frac{1}{RC} = 2\pi f_o;$$

P_1 can be used to set $0.95 < n < 1.05$ placing a variation in f_{notch} of ±2.5% relative to f_o with the shown component values.

$$q = \text{Fractional potentiometer value of } P_2 \qquad Q_{notch} = \frac{1}{3(1 - q)};$$

P_2 can be used to vary the slope of the notch. To avoid instability when $q = 1$, a 27Ω resistor can be placed in series with P_2.

$$r = \frac{R_5}{R_4};$$

The ratio, r, is chosen to be 2 in this application. If r is exactly 2, a maximum notch depth can be obtained. A notch depth of 70 dB was measured using 1% components for the actual circuit. Ultimately, the maximum notch depth is determined by the matching of the two resistors, R, the two capacitors, C, and the op amps open loop gain. If $0 < r < 2$ a pair of complex conjugated zeros appear. If desired, R_5 can be made adjustable, allowing for adjustment of the notch depth. For $r > 2$ the circuit produces sinusoidal oscillations at the frequency, f_o.

A_1 is acting as impedance converter but is really uncommitted - it can be used to provide other sensor signal conditioning functions as required.

3.5. TLE2061/2/4 and TLE2161 Excalibur Bifets

The first Excalibur Bifets to be released by Texas Instruments are the TLE2061 family of low power, high output drive op amps. Designed using Texas Instruments' Excalibur technology (see figure 29), these devices offer a number of features not previously available from a Bifet.

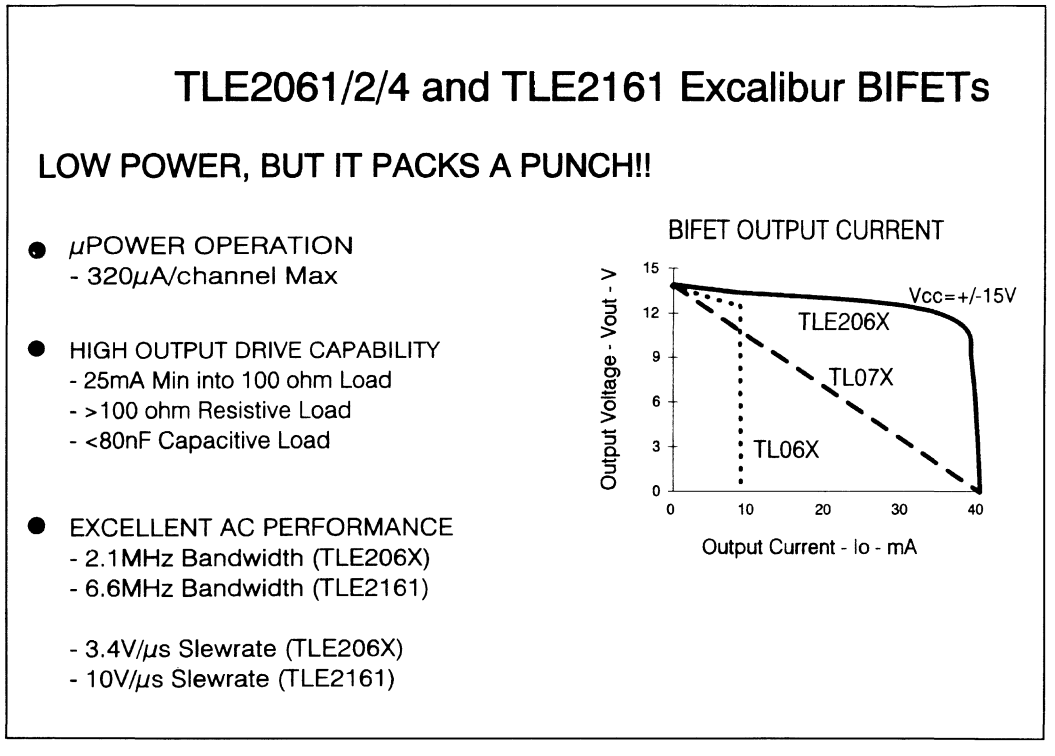


Figure 1.11 TLE2061/2/4 and TLE2161 Excalibur Bifets

The designer's task when developing these products was to produce a family of Bifets with microwatt power consumption but with the ability to drive heavy resistive and capacitive loads. The result is a part which typically consumes less than **300 μA** of supply current but can also deliver in excess of **25 mA of output current!** The device is guaranteed to drive 100 ohm resistive loads and will remain stable when driving capacitances up to 80 nF! A further feature of its excellent output performance is its relatively low distortion. Even with microampere supply currents, the **total harmonic distortion is 0.025%,** (Avd=2, f=10 kHz, R_L=10 kΩ).

The excellent output drive has enabled these devices to be used extensively in low power telecom circuits - the parts are particularly well suited in the 2 Wire - to - 4 Wire hybrid circuit found in line card and modem circuits which has a typical impedance of 600Ω.

DC wise the TLE2061 family also perform outstandingly, the maximum offset voltage for the TLE2061B is **500 µV**, with a specified Vio drift of 0.005 µV/month and 6 µV/°C. This is better still than the enhanced Bifets discussed previously.

Although achieving a very respectable **2.1 MHz bandwidth** and a **3.4 V/µs** slew rate, a decompensated version, the TLE2161 is also available to satisfy the more demanding ac requirements - this is discussed in figure 13.

Targeted initially at low power telecom equipment these versatile devices are finding applications in a number of other systems. Power supplies are making use of their high common mode input range, audio systems from its AC performance and standard low power instrumentation and filter circuits are benefiting from the combination of low offset voltages and low bias currents.

3.6. High Performance 2 - 4 Wire Converter

Driving transmission lines creates extra demands on any op amp. These demands are clearly shown in an application where the op amp needs to drive a 600Ω transformer coupled telephone line with the minimum of distortion.

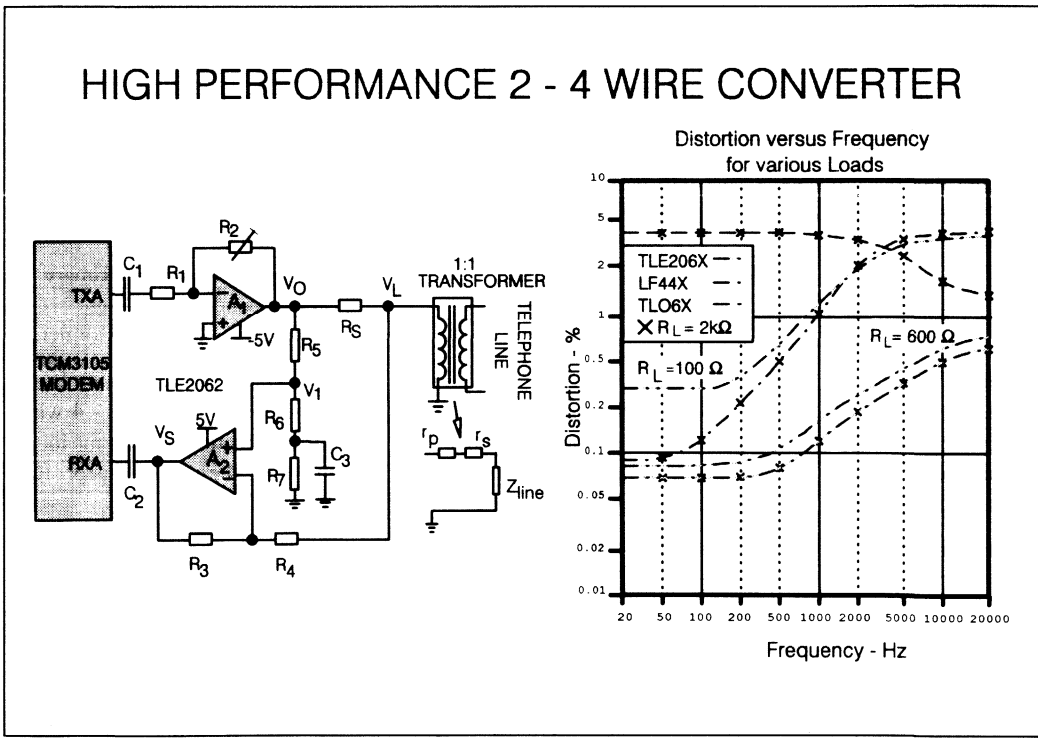


Figure 1.12 High Performance 2 - 4 Wire Converter

The telephone line will be carrying information in both directions, minimising cable costs, resulting in the primary of the isolating transformer acting as both an input and an output. So when the modem is driving the line (via TXA) some of the signal will be fed back to the input of the modem, RXA, by amplifier A2. This signal is reduced by the R_5, R_6, R_7 and C_3 network: The output of A1 is fed to the non-inverting input of A2 and is subtracted from the primary voltage. Careful choice of R_5, R_6, R_7 and C_3 minimises any signal from TXA being fed to RXA.

As the system is duplex the output impedance of the TXA op amp A1 must match the line impedance, but in order to achieve low distortion the output impedance of A1 must be low. The **TLE2062** was designed for applications requiring such a high drive capability and at the same time a low quiescent power consumption. The TLE2062 is capable of operating from ±22V down to ±3.5V, and when driving a 100Ω load from a ±5V supply has a guaranteed minimum output swing of ±2.5V . It provides this output with a very low level of distortion. As can be seen no other similar type of devices can provide either this output drive or the low level of distortion. All other devices offering similar performances require a power consuming ±12V or more supply voltage. Any distortion produced by the op amp will be sent down the telephone line via the transformer and will also be fedback to the receiver at RXA. The transformer's bandwidth limiting will help to reduce some of the distortion sent down the line, but it cannot reduce the distortion fedback to RXA. The distortion fedback to RXA can be difficult to counteract thus decreasing the quality of the telephone system.

To match the line's impedance, the TLE2062 has to have a series resistor R_S on its output. R_S will form a potential divider with the winding resistances of the transformer and the line impedance. Over the frequency range of interest, the matching transformer will add phase shift to the output V_L. So the choice of R_5, R_6, R_7 and C_3 should take this potential division and phase shifting into account. Looking from the line the impedance seen will be the winding resistances in series with R_S, and so R_S should equal the line impedance minus the winding resistances:-

$$R_S = Z_{line} - (r_p + r_s) \ldots .$$

where $r_s + r_p$ are the primary and secondary winding resistances of the transformer.

The actual impedance of the telephone line can vary enormously from the typical 600Ω, ranging from 1200Ω down to 100Ω, so the value of R_S will change depending on the position of the 2 - 4 wire converter in the system and the length of the telephone line. In this application, assuming ideal impedance of the line, the low output impedance of the TLE2062 means that the series resistor, R_S, will need to be around 510W, ($r_S + r_P$ = 100W).

Looking at the nodes V_O, V_L, V_1 and V_S yield the following equations:

$$V_1 - V_S = [V_L - V_S] R_1/(R_O+R_1)$$ Ignoring Z_L effect on R_O.

$$V_1 = V_O \times Z_1/(Z_O + Z_1)$$

$$V_L = V_O \times Z_L/(Z_S + Z_L)$$ Where $Z_L = Z_{line} + r_s + r_p$

R_O and R_1 are made equal to one another to maintain the received signal dynamic range. A value of 51 kW relieves any loading by A2 and provides a lower power compromise with any thermal noise. Therefore for V_S to equal zero :-

$$\frac{ZO}{Z1} = 1 + 2\frac{ZS}{ZL}$$

As stated, the value and largely the phase of Z_L will vary with frequency due to the telephone line and the transformers' inductive natures, and so these effects should be considered. With a 600W telephone line Z_L = 700W, and so

$$\frac{Z_O}{Z_i} = 1 + 2\frac{510}{700}$$

Therefore

$$Z_O = 2.46 \times Z_1.$$

Resistors R_5, R_6 and R_7 are used to provide the matching for Z_O/Z_1, while C_3 is used to counteract the phase shift and reduce the gain at higher frequencies. Using the values of 91 kΩ, 27 kΩ, 10 kΩ and 2 nF for resistors R_5, R_6, R_7 and capacitor C_3 yields attenuations in the region of 10 to 30 dB of the frequency range of interest. Reducing the power fed back to RXA by 10 to 1000.

3.7. TLE2161 and Decompensated Op Amps

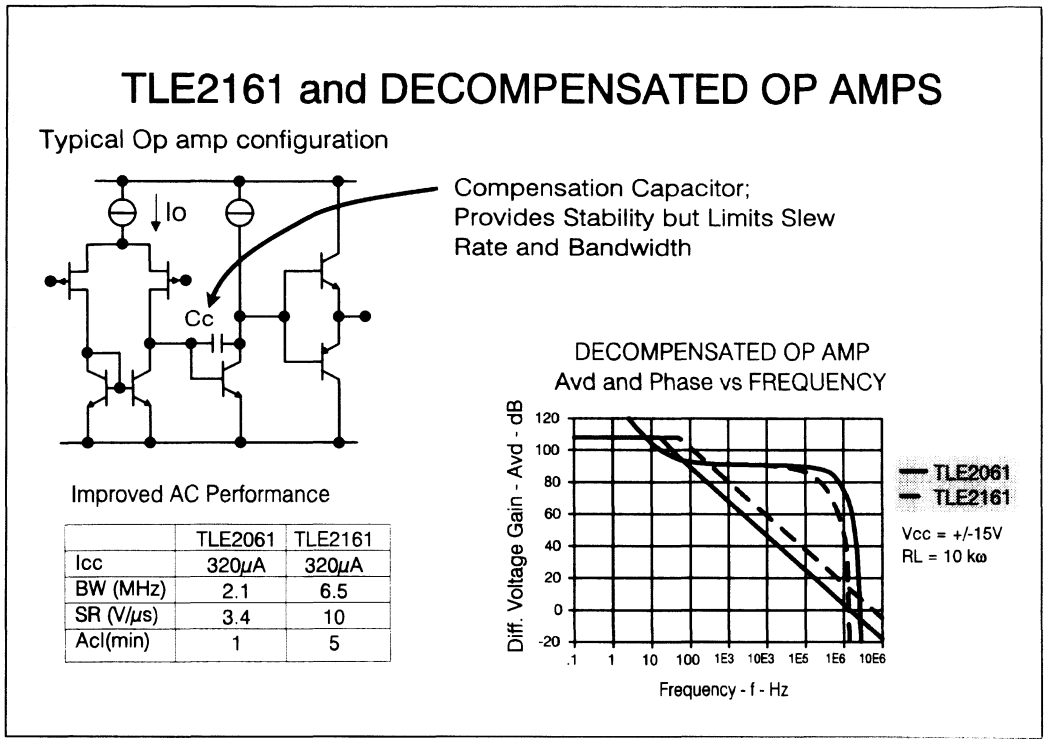
Manufacturers are continuing to release decompensated operational amplifiers, and the TLE2161, a decompensated version of the TLE2061, and is one the latest Bifets releases from Texas Instruments.

3.7.1. Decompensated Op Amps

The figure shows a simplified schematic of an op amp. The internal capacitor, Cc, is used to ensure that the device is stable. Its size is dependent upon the gain of the input stage and the position and number of internal poles within the amplifier. This capacitor ensures device stability and determines the slew rate and bandwidth of the op amp. Normally the capacitor is designed such that the amplifier is stable with closed loop gains down to 1. In a decompensated amplifier the size of this decompensation capacitor is reduced, the device will now no longer be unity gain stable. Instead the capacitor is chosen such that the amplifier is now stable at a different minimum closed loop gain (for most op amps this is 5).

The advantage therefore is a device which meets the same DC requirements as the compensated part but which has much improved slew rate and bandwidth performance.

The table below shows how, by decompensating the TLE2061, the TLE2161 has improved its ac performance, the DC performance is unchanged.



	TLE2061	TLE2161
Icc	320μA	320μA
BW (MHz)	2.1	6.5
SR (V/μs)	3.4	10
Acl(min)	1	5

Figure 1.13 TLE2161 and Decompensated Op Amps

	Bandwidth	Slew Rate	Icc
TLE2061	**2.1 MHz**	**3.4V/μs**	**280μA**
TLE2161	**6.5 MHz**	**10V/μs**	**280μA**

* Acl(min) = 5, values are typical.

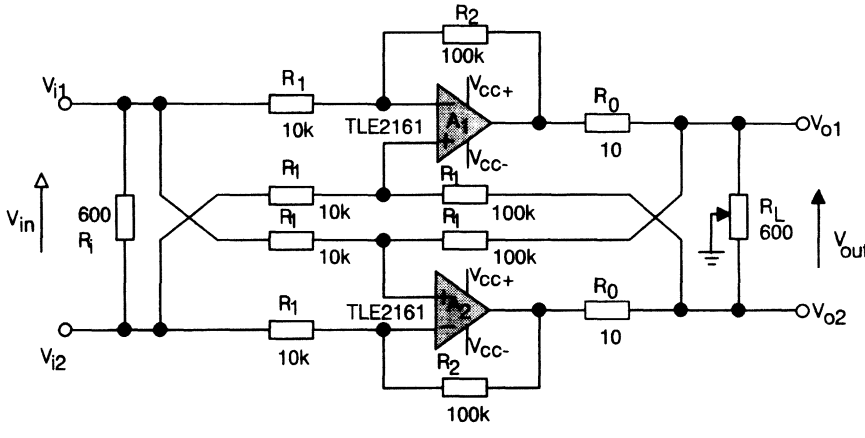
Another performance decompensated amplifier available from Texas Instruments is the TLE2037, low noise precision op amp. This has a bandwidth of 76 MHz, compared to 15 MHz for the compensated TLE2027.

3.8. Low Power Active Step-up Transformer

Transformers and Differential Transmission Lines

Small signal transformers are widely used in telecommunication equipment and professional audio applications to drive or terminate a differential or balanced transmission line with a characteristic line impedance of 600Ω. Such transmission lines provide a simple and noise immune media for transferring small ac signals in the speech or audio frequency range from microphones to amplifiers, from mixing desks to peripheral equipment or between nodes in telecommunication systems - not to mention the

standard telephone line as the best known application. Common mode noise and hum signals picked up by a differential line are effectively suppressed by the common mode rejection and balance of the receiver.



$$\text{DIFFERENTIAL GAIN} = 20\text{dB}: \quad \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

Vcc = ± 5V to ± 20V; Icc = 500uA; FREQUENCY RANGE: DC to 600kHz ± 1dB

Low Power Active Step-up Transformer

Transformers have of course the advantage of high isolation combined with robustness and passive operation. Their voltage transfer ratio is typically 1:1 but in some applications a signal level step-up or an impedance conversion is required. Using a transformer rather than a standard differential line driver amplifier allows for the drive of unbalanced loads without reduction in the output swing.

Differential line driver amplifiers need high output current capability to maintain the swing under heavy load conditions but have usually superior bandwidth performance and low output impedance.

Active Step-up Transformer

A differential-input differential-output amplifier can be constructed by parallel coupling of two differential input amplifiers. However, the illustrated low power active step-up transformer is more than a standard differential-input differential-output amplifier - the circuit's unique configuration is widely used in professional audio applications. The cross coupled feedback approach ensures that the output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 10 or 20 dB. The input of the differential line driver amplifier can be set for inverting, non-inverting or single ended operation. The shown differential input

configuration combined with the unique differential output approach provides an active differential-input differential-output amplifier acting in many respects exactly as a step-up transformer - hence the figure heading: Active Step-up Transformer

The very low 500 mA (typical) quiescent supply current makes this circuit especially suited for battery driven applications and portable equipment or for use in telecommunication and audio applications, where several identical circuits are used in the same equipment.

Why use the Excalibur TLE2161 Op Amp?

Similar circuits can be implemented with several different amplifiers - such as the TLE2027 and TLE2037 - both are also capable of driving low impedance loads over the speech or audio frequency range. However, the low power TLE2161 Excalibur op amp is unique in terms of power consumption. It operates in this application requiring only a quiescent supply current of 250 mA (typical) each, while simultaneously being capable of driving a 100 kHz $20V_{pp}$ signal into a 600Ω load!

The excellent AC performance for such a low power op amp is achieved by a JFET input stage, combined with Excalibur processing and decompensation for a minimum gain of five for stability. This combination yields a 10V/µs slew-rate and 6.5 MHz gain-bandwidth product allowing operation in both the speech and audio range. In addition to the shown application, these properties are useful in low power active filter design.

TLE2161's low offset, down to 500 µV max @ 25°C, does not disturb the DC balance of the line. Also, the JFET input's low input offset current adds insignificant errors to the total offset voltage even with the given high feedback impedance level.

Design Details

Ignoring the influence of R_O and R_L on the output voltage, V_{out} (assuming ideal op amps), the voltage transfer function of the circuit can be derived from:

$$V_{o1} - V_{o2} = \left(- V_{i1}\frac{R_2}{R_1} + V_{i2}\frac{R_2}{R_1+R_2}\left(1+\frac{R_2}{R_1}\right) + V_{o2}\frac{R_1}{R_1+R_2}\left(1+\frac{R_2}{R_1}\right)\right)$$

$$-\left(- V_{i2}\frac{R_2}{R_1} + V_{i1}\frac{R_2}{R_1+R_2}\left(1+\frac{R_1}{R_2}\right) + V_{o1}\frac{R_1}{R_1+R_2}\left(1+\frac{R_2}{R_1}\right)\right); \quad (1)$$

$$(V_{o1} - V_{o2}) = -\frac{R_2}{R_1}(V_{i1} - V_{i2}); \quad <=> \quad V_{out} = -\frac{R_2}{R_1}V_{in}; \quad \text{or}$$

$$\boxed{\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}} \quad (2)$$

If one of the differential outputs nodes - say V_{o1} is loaded heavily to ground by an unbalanced load or even shorted to ground, the opposite output amplifier, A_2 senses the decrease in V_{o1}'s output voltage and compensates by boosting its own output, V_{o2}. The sense feedback ensures that the gain remains as given by (2). The voltage at both non-inverting op amp inputs is approximately zero volt. When V_{o1} decreases, the voltage on the non-inverting input of A_2 increases, thereby raising the voltage V_{o2} to

maintain the output voltage, V_{out}. Also, the voltage drop across R_O is adjusted out. Consequently, the line driver with differential input can drive unbalanced loads, exactly like a true transformer.

In order to ensure that one output can drive the total output swing, when the other is shorted, the output swing under normal balanced load conditions must be held below half the maximum swing. With an input signal, $V_{in} = 2V_{pp}$, the output swing, $V_{out} = 20V_{pp}$. This level can easily be sustained by one op amp if the other 's output is shorted to ground.

The choice of resistor impedance for R_1 and R_2 is a compromise between on one side, low power consumption for small signal levels and high input impedance, against on the other side, significant speed requirements. If the feedback resistor, R_2, is larger than 100 kΩ it may add further phase shift due to parasitic input capacitance, that could lead to instability. Additionally, the common mode rejection will be reduced as accurate matching of high impedance resistors is difficult. Good input common mode rejection requires well matched values of all R_1s and all R_2s.

The circuit operates from ±5V to ±20V supplies and the maximum output swing is of course limited by the applied supply voltage. At very high frequencies however, the slew rate limitation of the op amp influences the maximum output swing. To produce a non-slew rate limited $10V_p$ sinusoidal signal at 100 kHz, $10 \times 2\pi \times 100 \times 10^3$ V/s = 6.3V/µs minimum slew rate is required. This is well below the op amp's specified minimum of 7V/ms.

Measured Performance

Measured typical performance is given in the table.

Parameter	Test Conditions		Measured Performance	Unit
Frequency Response	$V_{out} = 5V_{pp}$, $R_L = 600\Omega$	$V_{cc} = \pm 15V$,	0 - 600 ±1	kHz dB
Maximum	Balanced Load,	f = 20 kHz,		
Output Voltage	$R_L = 600\Omega$,	$V_{cc} = \pm 20V$	54.6	V_{pp}
Swing	$R_L = 600\Omega$,	$V_{cc} = \pm 15V$	42.6	V_{pp}
	$R_L = 600\Omega$,	$V_{cc} = \pm 5V$	12.8	V_{pp}
	$R_L = 300\Omega$,	$V_{cc} = \pm 5V$	11.6	V_{pp}
	$R_L = 100\Omega$,	$V_{cc} = \pm 5V$	8.0	V_{pp}
Max Common Mode	$V_{cc} = \pm 20V$		±17.9	V_{pp}
Input Voltage Range	$V_{cc} = \pm 15V$		±12.8	V_{pp}
	$V_{cc} = \pm 5V$		±3.0	V_{pp}

At low frequencies, the common mode rejection ratio of the circuit depends on resistor matching. However, at high frequencies, it is affected by the op amps own common mode rejection ratio. Using resistors with 1% tolerance, more than 50 dB common mode rejection was obtained for frequencies less than 10 kHz.

3.9. TLE2082 High performance Bifet

The latest member of Texas Instruments' vast family of Bifets is the TLE2082. This is high speed, low noise dual Bifet. In common with all the most recent releases of Texas Instruments' Bifets the TLE2082 is constructed using the Excalibur technology.

TLE2082 DUAL EXCALIBUR BIFET

HIGH SPEED AND LOW DISTORTION!

- HIGH-GAIN BANDWIDTH PRODUCT
  ..... 10 MHz
- HIGH UNITY GAIN SLEW RATE
  ..... 40 V/μs
- FAST SETTLING TIME ....400 ns to 10 mV
  10 V STEP ....1.5 μs to 1 mV
- LOW VOLTAGE NOISE
  ..... 13.7 nV/√Hz

LOW CURRENT NOISE
..... 2.8 fA/√Hz

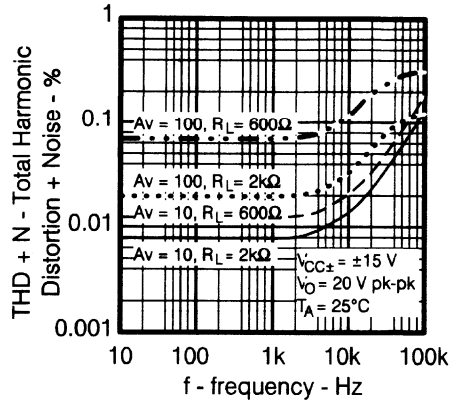


Figure 1.14 TLE2082 High performance Bifet

Texas Instruments was one of the first semiconductor manufacturers to supply Bifets (Fairchild were the first with their 100 mV offset offering. One of Texas Instruments' great strengths in their linear product range is its family of Bifets. In the mid-eighties this was reinforced by the introduction of the TL030s and TL050s. The derivation of Excalibur Texas Instruments has enabled to continue this long history in Bifet op amps with the TLE2060s, and now the TLE2080s.

The TLE2082 has been developed to meet the higher requirements of today's new applications. This covers audio applications as well as high speed control applications. The strength of all Bifets is their very high slew rate. The TLE2082 has taken this a stage further with its 10 MHz unity gain bandwidth and large 40 V/μs slew rate. The specifications are further added to by its low noise voltage of 13.7 nV/$\sqrt{\text{Hz}}$ making it ideal for high speed low noise transducer interface.

The very low Total Harmonic Distortion (THD) figures make it ideal for audio applications, replacing the TL050s and TL070s which had become standard members in many high performance audio systems.

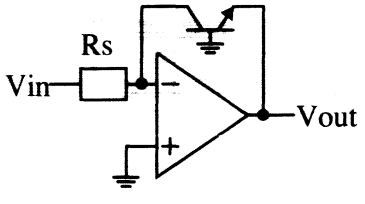
The low noise and high speed make the TLE2082 well suited to industrial control applications. The high slew rate is equally well matched by its very fast settling time. The TLE2082 takes just 400 ns to settle within 10 mV of its final steady state value for a 10 V, and just 1.5 µs to within 1 mV.

With audio and control applications in mind the TLE2082 was designed to have a large output current drive capability, exceeding that of the TLE2060s and the TLE2037. This is realised in a minimum output current capability of ±30 mA, enabling the device to drive long cables, and even some heavy and demanding audio loads.

3.10. Fast Logarithmic Converter

The TLE2082 was designed for high speed applications which require high stability or high drive capability. Another application well suited to the TLE2082 is in a Log Amplifier.

A log amplifier exploits the logarithmic dependence of V_{BE} on I_C, and produces an output voltage equal to the logarithm of the input voltage.



The basis of a log converter is an op amp configured as an inverter that has a NPN transistor as its feedback loop. This results in the input being converted into a current via the source resistor, R_S. The input current then flows through the transistor's collector causing the base-emitter voltage to change with the input voltage.

The base of the transistor is tied to ground so the output will be 1 base emitter voltage below ground.

Assuming the op amp has a virtual short between its inputs the collector current will be:

$$I_C = \frac{V_{IN}}{R_S} \qquad \text{Neglecting } I_{IB}$$

But

$$I_C = I_{ss} e^{\frac{V_{BE} q}{kT}} \qquad V_O = -V_{BE}$$

This establishes the link of V_{IN} to V_O.

$$V_O = -\frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log\left[\frac{V_{IN}}{R_S I_{SS}}\right]$$

The logarithmic relationship between the output voltage and the input voltage can clearly be seen. The temperature effects can also be seen, first of all in the kT/q factor, but also in I_{SS}. I_{SS} has a negative co-

efficient while kT/q has a positive co-efficient. These normally react to give V_{BE} its normal negative temperature co-efficient. This is where the subtleties of log amplifiers come into play.

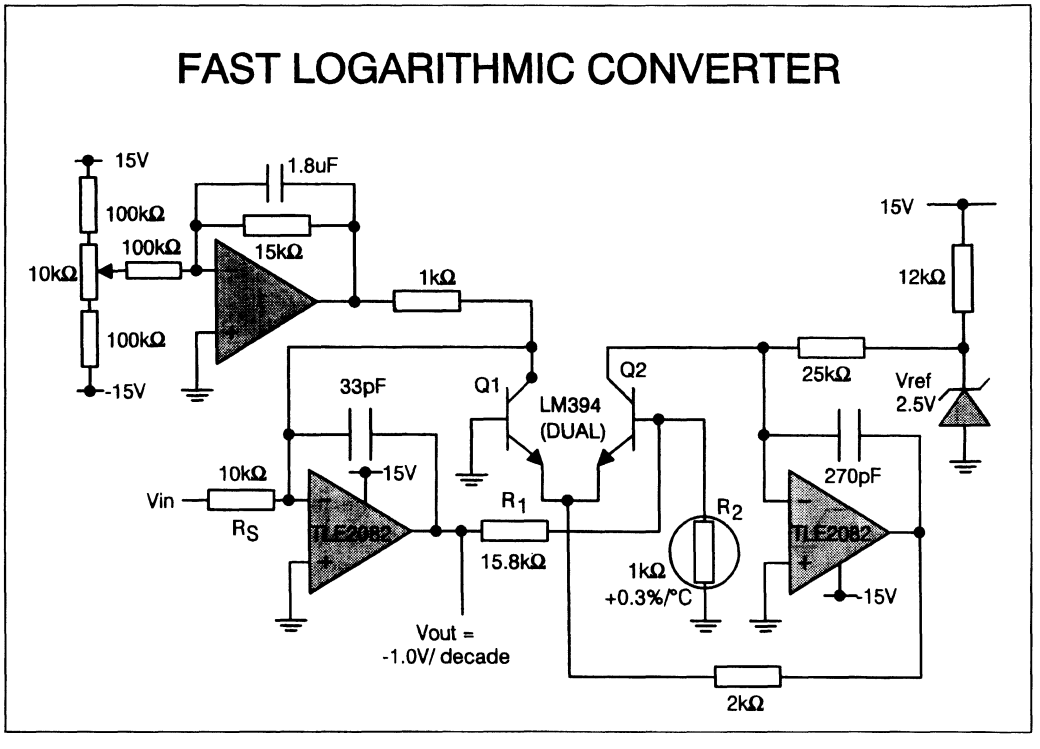


Figure 1.15 Fast Logarithmic Converter

The figure above shows one way of overcoming some of the temperature drift problems of the log amplifier. This is very similar to the fundamental log amplifier shown earlier except that two very accurately matched transistors are used, instead of just one transistor. Another difference is that the TLE2082 is driving the base of the second transistor (ignoring resistors R_1 and R_2), placing both transistors within the feedback loop. The output of op amp A1 will be the base-emitter drop of Q2 minus the base-emitter drop of Q1, this fact will be exploited to reduce the temperature effects.

Once again the input voltage will be converted into current by R_S, this current flows into the collector of Q1, causing its emitter to drop by 59 mV/decade of collector current. The emitter of Q2 is connected to the emitter of Q1.

The LT1009 and the virtual earth of op amp A2 set up a fixed current source of 100 µA. This is used to bias Transistor Q2 setting up a constant V_{BE} (at any fixed temperature). Transistors Q1 and Q2 are part of highly matched transistor pair, which share the silicon and so should be at the same junction temperature. This also means that they should have the same I_{SS}.

The V_{BE1} of Q1 will be as follows:-

$$V_{BE1} = \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log\left[\frac{V_{IN}}{R_S I_{SS}}\right]$$

While V_{BE2} the of Q2 will be:-

$$V_{BE2} = \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log \frac{I_{C2}}{I_{SS}}$$

The voltage at the output of the TLE2082 is $V_{BE2} - V_{BE1}$, and so subtracting V_{BE1} from V_{BE2} gives:-

$$V_{BE2} - V_{BE1} = \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log \frac{I_{C2}}{I_{SS}} - \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log\left[\frac{V_{IN}}{R_S I_{SS}}\right]$$

Factorising $$V_{BE2} - V_{BE1} = \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \left\{\log\left[\frac{I_{C2}}{I_{SS}}\right] - \log\left[\frac{V_{IN}}{R_S I_{SS}}\right]\right\}$$

Cross multiplying $$V_{BE2} - V_{BE1} = \frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log\left[\frac{R_S I_{C2}}{V_{IN}}\right]$$

Or $$V_{BE2} - V_{BE1} = -\frac{1}{\log e} \bullet \frac{kT}{q} \bullet \log\left[\frac{V_{IN}}{R_S I_{C2}}\right]$$

By using two similar transistors the effects of I_{SS} has been cancelled out, the effect of kT/q has not. The effect of it however can be cancelled by using a ptc (positive thermal co-efficient) resistor for R2.

At 25°C $$V_{BE2} - V_{BE1} = -0.059 \bullet \log\left[\frac{V_{IN}}{R_S I_{C2}}\right]$$

Setting R_S = 10 kΩ and I_{C2} = 100 µA, $R_S \bullet I_{C2}$ = 1 V. The output of op amp A1 would be $V_{BE2} - V_{BE1}$, but in order to achieve an output of 1 V per decade of input voltage, potential divider R_1 and R_2 is added. Placing the potential divider between the output and the base of the second transistor increases the gain and is also used to cancel out the temperature drift effects of kT/q, by R_2.

In order to achieve an output to input ratio of 1 V/decade a potential divider of approximately 1/16.9 is required, this is best achieved by using a 15.8 kΩ resistor for R_1 and a 1.0 kΩ for R_2.

The PTC resistor must be a temperature measurement and control type, and not a temperature sensitive switching type. One suitable resistor is a Tel labs type Q81, which has a temperature co-efficient of +0.3%/°C.

Feedback capacitors must be included around the op amps to ensure stability, as for each op amp the transistors are adding gain within their feedback loop. For added protection a diode could be added across transistor Q1 to protect it from being destroyed should a negative input be applied to the op amp's input.

The offset of the TLE2082 can be nulled out by an additional op amp, A3, which either adds/subtracts current to/from I_{C1}.

The TLE2082 is well suited to this application because of its very low noise, and its very low bias currents. The log amp can typically deal with currents varying from 1 nA to 10 mA, or over 7 decades. Amplifier A3 can be used to set the zero output voltage point. When dealing with the higher levels of current it is important that op amp A1 should not go into current limit, the TLE2082 can supply more than 30 mA and so there is not any possibility of this occurring.

4. CMOS Operational Amplifiers

4.1. CMOS Operational Amplifiers

Although originally considered to be too unstable for many linear functions, CMOS amplifiers are now well accepted as a real alternative to many bipolar, Bifet and even dielectrically isolated op amps.

Texas Instruments was the first company to release linear devices designed using the CMOS process, LinCMOS™, which was specifically developed for linear circuits. The first products were released in 1983, and LinCMOS™ and its next generations are still being used today to realise a whole range of linear functions - from op amps to A-D converters.

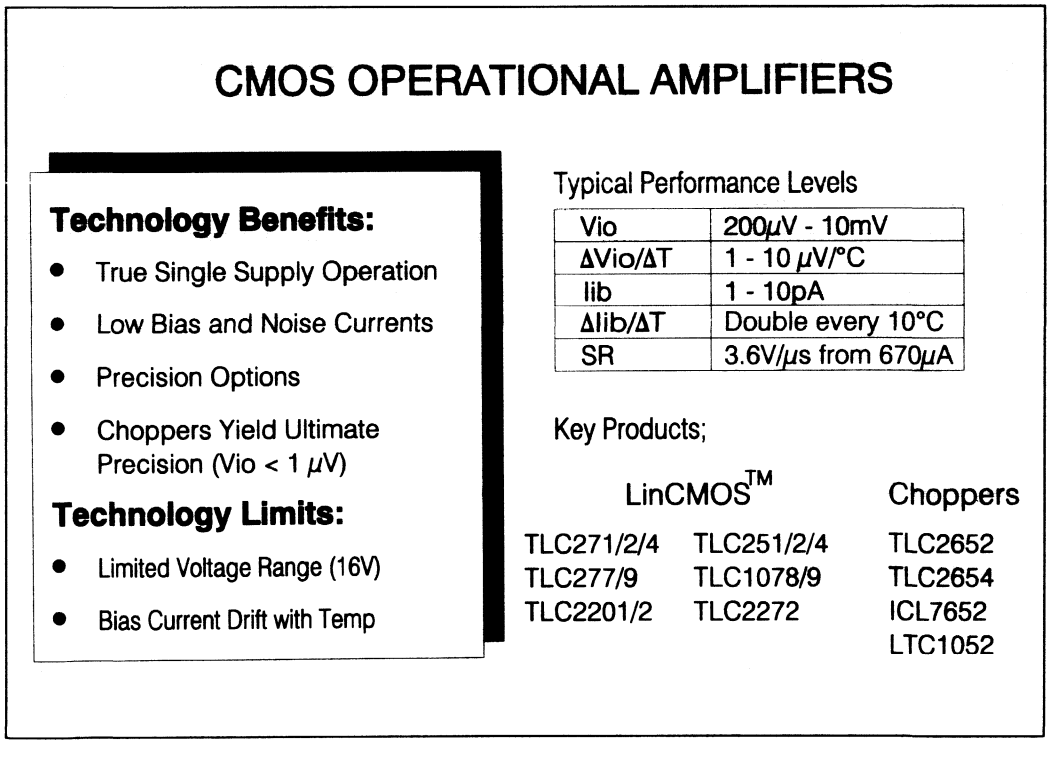


Figure 1.16 CMOS Operational Amplifiers

LinCMOS™ will be discussed later in the seminar, but below the various strengths and weaknesses of CMOS technologies are highlighted below.

4.1.1. CMOS Advantages

Single supply operation;

By far one of the most significant advantages of using a device designed using CMOS technology is their excellent single supply operation. By using PMOS on the input stage and an NMOS on the output stage it is possible to develop a device with an input common mode range that includes the negative rail and an output stage that swings all the way down to the negative supply - true single supply operation! This feature obviously makes the devices extremely popular in battery powered applications.

Low Voltage and low Supply current applications;

Texas Instruments has low bias op amps capable of operating with supply currents of less than 10μA and at supply voltages down to 1.4V. Single supply battery powered applications benefit further by using these parts.

High input impedance and low bias currents;

Like Bifet op amps, using MOS transistors on the input stage enables op amps with high input impedance and low offset and bias currents. Bias currents can be in the fA range but difficulty in testing, and various leakage currents mean that these levels of performance are rarely specified. A typical LinCMOS™ op amp has a bias current at 25°C of 100 fA. Over temperature however the bias currents will double for every 10°C increase in temperature.

ESD (Electrostatic Discharge) Protection;

Something which is perceived to be a problem but with devices designed using LinCMOS™ is not. All devices produced using LinCMOS™ are designed to withstand 2 kV ESD - something many bipolar designs cannot claim. Protection circuits found in LinCMOS™ devices are discussed in figure 14.

4.1.2. CMOS Disadvantages

Limited Voltage range;

Although ideal for low supply voltage applications, most CMOS parts will not operate with supply voltages greater than 16 or 18 Volts. This is a limitation in some wide supply, instrumentation applications.

Limited Offset Voltages;

The best CMOS devices can achieve offset voltages as low as 200 μV which is better than Bifet parts but does not compete with the best bipolar designs. Typical CMOS op amps will have an offset voltage specification of 2 mV - 10 mV. The stability of CMOS devices is however improved over Bifet designs.

Chopper stabilised op amps however, which are discussed in detail later, are designed using CMOS technology and achieve the ultimate in DC precision. Maximum offsets as low as 1 μV are realisable.

High Noise voltage;

Like Bifets, a MOS input causes devices to suffer from a high input noise voltage and high 1/f corner frequency, their input noise current is normally extremely low. The TLC2201 however, discussed in foil 20, actually features a combination of low voltage and current noise specifications.

4.1.3. Texas Instruments' CMOS amplifiers

TLC2201/2	ICL7652	TLC277/9	TLC271	TLC27L2/4
TLC2652/4	LTC1052	TLC27L7/9	TLC272/4	
TLC1078/9		TLC27M7/9	TLC27M2/4	

LinCMOS™ was Texas Instruments' first linear CMOS technology and the resulting products are now industry standards. It has since been upgraded with **Advanced LinCMOS™** which because of smaller geometries and more compact capacitors has enabled the true interface of digital and analogue structures - the most obvious result has been performance a/d converters. **LinBiCMOS™**, is the latest revision - it features the CMOS structures as found in Advanced LinCMOS™ but also has true bipolar transistors included. This technology is being extensively used as part of Texas Instruments' LinASIC™ program.

4.2. TLC27X Series - The Single Supply Op Amp

The first LinCMOS™ op amps were released in 1983 and there are now a number of families to chose from. Newer designs have been optimised for precision, low noise or low power and are discussed in detail later in the seminar. This figure summarises the various features of the original designs;

If we consider the part number of a standard LinCMOS™ op amp the whole family can be easily understood. A typical part number is....**TLC27L2AID.**

'TLC2' means the device is a LinCMOS™ op amp. Parts starting TLC3... are comparators. Standard amplifiers (beginning TLC27) operate with supply rails ranging from 3 to 16 Volts. The **TLC25X** version have been designed to operate with **1.4V supplies**.

'L' refers to the Bias version. The standard family of products are available in 3 Bias versions - each determines the supply current and corresponding AC performance of the amplifier. 'L' means low bias with low supply current and low slew rates. 'M' would mean medium bias and no letter equates to high Bias (see above figure).

'2'. There are single, dual and quad versions available and this number relates to the number of channels. Care must be taken however as the **TLC277** and **TLC279** (duals and quads) are also available. These devices are precision, zener zapped versions with low offsets down to 500 µV, and are also available in 3 bias options.

'A' means the device has been offset selected, with a maximum Vio of **5 mV**. Standard parts are specified with **10 mV** of offset and the 'B' selection has **2 mV** of offset. As stated above, real precision is available from the TLC277 and TLC279.

'I' means that the device is specified over the industrial temperature ranges. They are also available in commercial and military temperatures designated 'C' and 'M' respectively.

'D' . All CMOS op amps are available in a number of different packages, DIL, SO, Ceramic and chip carrier designated by P or N, D, JG or J and FN respectively.

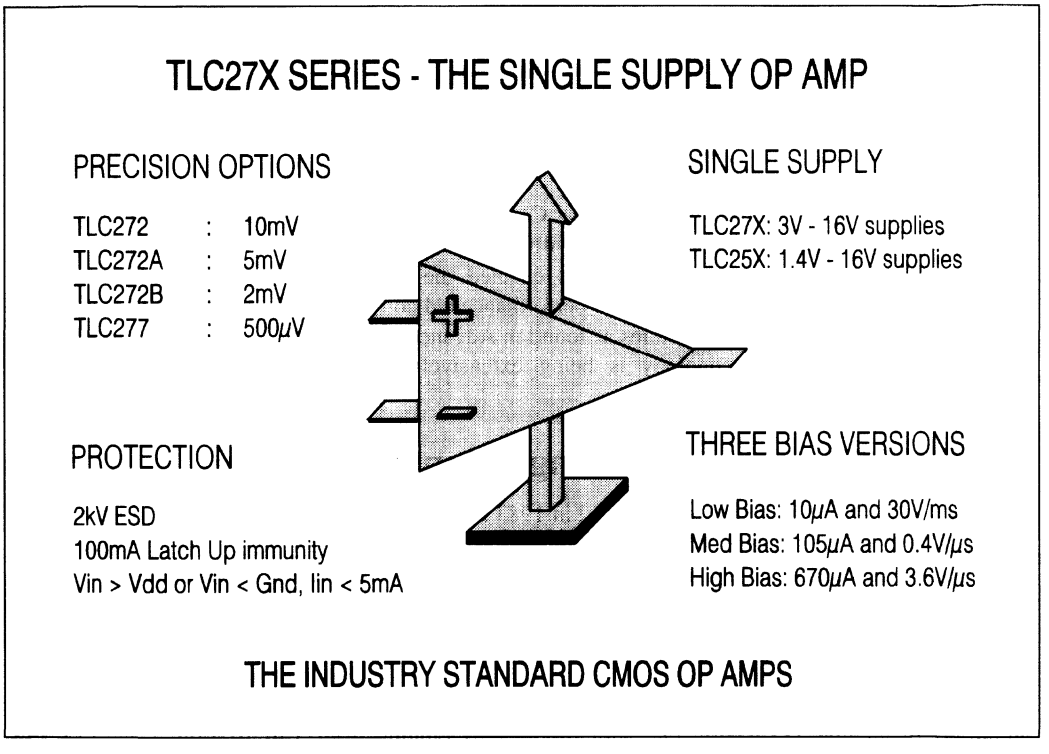


Figure 1.17 TLC27X Series

4.2.1. Common CMOS Problems Avoided

ESD - Electrostatic Discharge is one of the most common causes of damage to CMOS devices. To reduce failures due to this phenomenon, each pin on Texas Instruments LinCMOS^{TM} devices is protected by internal circuitry.

Standard ESD protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltage but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting resistors during normal operation after an ESD voltage has occurred. Although these currents are small, in the order of tens of nanoamps, CMOS amplifiers are usually specified to draw input currents as low as tens of picoamps.

To overcome this limitation, Texas Instruments design engineers developed a patented ESD protection circuit which can withstand several 2 kV ESD pulses while reducing or eliminating leakage currents that may be drawn through the input pins.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000V discharged from a 100 pF capacitor through a 1500 ohm resistor (human body model) and 200V from a 100 PF capacitor with no current limiting resistor (Charge device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

Latch Up - Latch-up occurs when an input or output voltage exceeds the supply rails, causing a parasitic SCR between the supply rails to turn on. When this occurs, the device supply current can increase from 20μA to many mA, which causes either functional or parasitic device failure. The only way to turn off this SCR is to remove the power to the device.

Voltages exceeding the supply rails can occur on I/O pins during many different stages of the manufacturing process. During board level testing (manual or bed-of-nails), stray voltages may be applied when contact is first made to the active circuit. ESD discharge from a person touching the end product may find its way to the I/O pin of the CMOS device and cause latch -up.

LinCMOS™ and Advanced LinCMOS™ products are designed to withstand - 100 mA I/O currents without latch-up. During wafer probe, every I/O pin is tested to this limit at 25°C with a very short duration pulse test that limits the amount of power and prevents damage to the device under test.

An additional feature of Texas Instruments' protection circuits is their ability to be able to withstand a continuous +/- 5 mA current on any I/O pin. If the input current is limited to less than 5 mA, then the voltage can be significantly higher than the supply voltages.

For more information about ESD, Latch-up and the various quality and test flows of LinCMOS™ and Advanced LinCMOS™ devices, please refer to the **LinCMOS™ Technology Highlights brochure.**

4.3. TLC1078/9 - True Micro-Power Op Amps

The TLC1078 and TLC1079 were developed as an extension to the existing LinCMOS™ family of op amps. They were designed and optimised to combine true micropower operation with excellent precision.

These devices will operate over the 1.4 V to 16V supply voltage range - power consumption is always low but it reduces with supply voltage and at 1.4V the device typically consumes 2μA of supply current per channel.

For precision operation the TLC1078 has a maximum offset voltage of 450 μV with extremely low drift of 1 μV/°C and 0.1 μV/month. Unlike bipolar devices which may appear to achieve better levels of performance, these devices continue to sustain these low offset voltages even when the supply voltage drops below the characterised value. Some bipolar designs experience an offset voltage increase of 5 fold as the supply voltage reaches it lower limits!

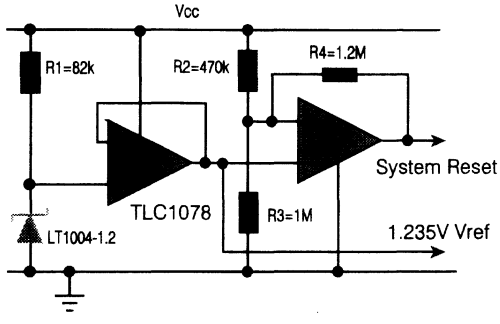
The other key parameters for DC precision designs are low bias currents and high open loop gain. Due it being a CMOS op amp, its bias currents are obviously low and introduce minimal DC errors. An added advantage is that they also cause negligible power dissipation in external resistors - a key factor in micro-power designs.

Although a relatively simple circuit, the application below highlights very well many of the factors to be considered when designing low power, precision applications.

TLC1078/9 - TRUE MICRO-POWER OP AMP

μPOWER WITH PRECISION

- ULTRA LOW POWER DISSIPATION
- LOW AND STABLE OFFSETS
  TLC1078(Dual); 450μV Max
  TLC1079(Quad); 850μV Max
  (Offset Maintained at Low Vcc)
- Vio DRIFT : 1μV/°C and 0.1μV/month
- LOW BIAS CURRENTS : 600fA
- EXCELLENT GAIN : 800,000



Turn On Voltage = 2.4V Turn Off Voltage = 1.68V

Power Consumption = 32.1μA at 3V
(Vref takes > 60%)

Figure 1.18 TLC1078/9 - True Micro-Power Op Amps

This circuit is targeted at low power, portable battery driven circuits and therefore the major requirement for this application is that power consumption should be kept at a minimum and that the circuit should operate at very low supply voltages. A dual op amp, the TLC1078, has been chosen to build a circuit which both supplies a precision reference and also generates a 'System Reset' signal (with hysterisis) when the power supply drops. The 1.235V reference can be used to supply other parts of the circuit (anything from A-D converters to comparators) and the Reset signal can be used to instigate battery-back-up or activate an external signal to show that the battery is running low.

The factors considered in this design were;

4.3.1. Low and Stable offsets;

Although not normally recognised as real precision amplifiers the op amp's chosen in this application are CMOS designs. Designed using the LinCMOS^{TM} technology, both amplifiers in the TLC1078 op amp have a maximum offset voltage of just 450 μV. A bipolar op amp, with a lower specified offset voltage could have been chosen, but the relative final precision of such a device may actually have been worse.

Many low power bipolar op amps suffer from a significant increase in offset voltage as the supply voltage is reduced. A device specified with 100 µV offset at 5V, is likely to have a much worse V_{IO} at lower supply voltages.

Low Bias Currents;

The second important factor to consider is the low input bias currents associated with CMOS designs. The DC error caused by bias currents flowing through external resistors is significantly higher for bipolar op amps than CMOS designs.

Bias currents are of particular importance when used in low power circuits. All resistors used in this application are large to reduce power dissipation, and therefore the DC error caused by bias currents flowing through these resistors is increased! There is therefore a trade-off between low power dissipation and absolute precision.

Low Vcc and Icc Operation;

The TLC1078 used in this application will operate from supply voltages as low as 1.4V and from supply currents less than 10µA. In this application the majority of current is consumed by the 'Low Power' reference. At 3V, the power consumption is 32.1µA, of which the reference consumes over 60%.

4.4. TLC2201/2 - Ultra Low Noise CMOS Op Amps

The TLC2201 and TLC2202 are probably the **WORLDS lowest noise** CMOS or JFET input operational amplifiers. Designed using Advanced LinCMOS™ technology, these precision op amps have proved extremely popular in a number of different applications.

Noise Performance - CMOS devices typically suffer from relatively high noise voltage and high 1/f frequency. Normally performing worse than Bifet op amps, they are typically not used in critical low noise applications. What all FET input devices benefit from however is a low noise current specification. Figure 21 explains why this is critical when interfacing to high impedance sources.

The TLC2201 and TLC2202 are unique because they combine low noise voltage (V_n) with extremely low noise current (I_n). A V_n specification of **8 nV/$\sqrt{Hz}$ (@ 1 kHz)** easily compares with some bipolar op amps, while I_n equal to **0.6 fA/$\sqrt{Hz}$**, matches the very best FET input amplifiers. The result is an op amp which can now be used in a wide range of low noise applications. It achieves outstanding performance when interfacing to even medium impedance sources and can replace discreet JFETs or matching transformers to achieved improved performance and lower costs.

The noise performance is specified with single(5V) or dual supplies (higher supply voltages are more typical) and its performance is guarantied for the 'A' and 'B' selections ('A' by sample test, 'B' by 100% test).

Precision - The TLC2201 is one of the worlds most precise CMOS op amps (non chopper stabilised). A maximum offset voltage of 200 µV combined with its obvious low offset and bias currents enables the device to be used in many precision applications.

TLC2201/2 - ULTRA LOW NOISE CMOS OP AMP

Lowest Noise CMOS op amp!!

- Low Noise Operation;
  Vn: 8 nV/$\sqrt{Hz}$ @ 1kHz
  In : 0.6fA/$\sqrt{Hz}$

  Noise is 100% tested on 'B' Selection

- Precision CMOS;
  Vio = 200 μV max for TLC2201
  500 μV max for TLC2202
  0.5 μv/°C drift

- Rail-to-Rail Output Swing

- Single and Dual Supply Operation

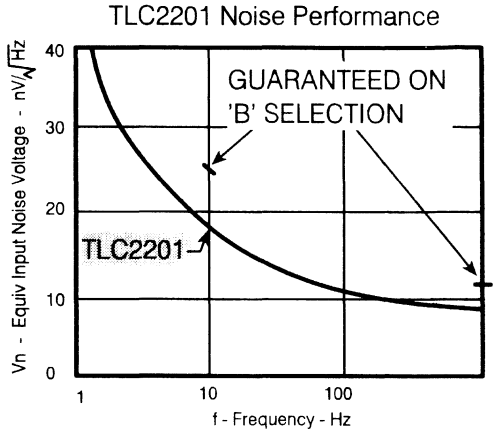


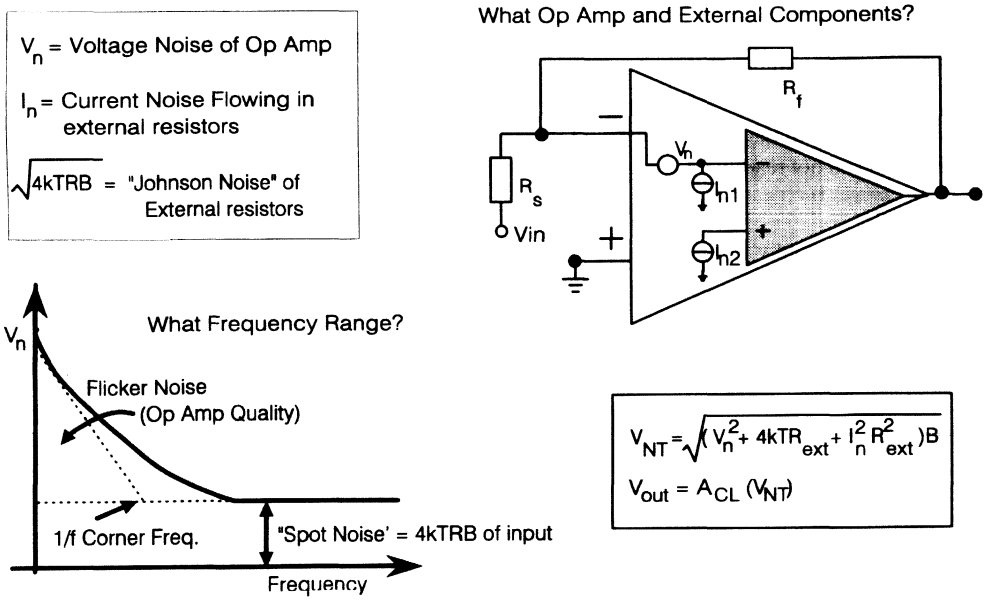
Figure 1.19 TLC2201/2 - Ultra Low Noise CMOS Op Amps

Rail to Rail Output Swing - Like other LinCMOS^{TM} op amps, the TLC2201 and TLC2202 are ideally suited to single supply applications - under normal conditions the output is guarantied to swing within 50 mV of the negative rail. A further benefit of these devices however is the ability of the output to actually swing to each rail - With +/- 5V supplies the output will swing to +/-4.7V. In single supply applications dynamic range is often crucial and the ability of these devices to provide an increased output signal significantly improves the performance of single supply circuits.

Applications - Both devices offer a number of benefits to a wide range of applications. Low noise enables the device to be used as an interface to high impedance sensors including piezoelectric transducers, pH meters and pin diodes. The devices are therefore ideal for test and measurement equipment. Rail to Rail output swing increases the performance and capability of single supply circuits, and when combined with its precision the device is ideal as an accurate signal conditioning interface in data acquisition circuits.

4.5. Noise Considerations

There are a number of factors to consider when developing a low noise circuit using operational amplifiers, these are discussed below:



Noise Considerations

4.5.1. Sources of noise

Johnson (or Thermal) Noise;

A resistor lying on a table will have a particular noise associated with it. Known as "Johnson Noise", this figure is not related to the quality of the resistor and its noise voltage is equal to;

$$Vn = \sqrt{4kTRB}$$

Where

k = Boltzmann's Constant

= 1.38 *10-23 J/K

T = Absolute temperature in Kelvin

= (298 @ 25°C)

R = Resistance value

B = Noise Bandwidth in Hz.

It is often useful to remember that a 100 kΩ resistor has a Johnson Noise equal to 40 nV rms over a 1 Hz bandwidth.

Johnson Noise is unpredictable but has a gaussian distribution, giving it a flat spectrum over frequency. It must also be remembered that this Johnson Noise is independent and extra to the errors caused by current flowing through the resistor.

In a low noise circuit the Johnson Noise of the external source resistor is often the limiting factor and it is one which can not readily be reduced. An alternative source may be the only solution!

Shot Noise;

Shot Noise(or schottky noise) is associated with the current flowing through a pn junction and is actually due to fluctuations in current. Shot noise becomes more dominant the lower the value of the actual current;

$$I_n = \sqrt{2qI_oB}$$

Where

q = Electron Charge

= $1.6 * 10^{-19}$ C

Io = DC operating Current

B = Noise Bandwidth in Hz

Like Johnson Noise, Shot Noise is unpredictable and is gaussian in distribution and is referred to as having a 'white' spectrum..

1/f or Flicker Noise;

Both operational amplifiers and resistors have noise characteristics different to what is expected from the Johnson Noise calculations. At low frequencies, noise is significantly increased, and follows a 1/f characteristic - i.e. the noise spectrum has an equal amount of power per decade of frequency. This noise, known as Flicker Noise, is very much dependent upon the quality of both the op amp and resistor. A Wire-wound resistor will have a lower noise than a carbon equivalent.

With operational amplifiers the amount of Flicker noise is very dependent upon the quality of the op amp and the level of care put into the design as well as the actual process being used. The point at which the flicker noise crosses the constant 'Spot Noise' of the op amp is known as the 'corner frequency'.

Popcorn Noise;

Popcorn Noise sounds like noise popping when played through a speaker. It is characterised by "hopping" between different noise levels, and can last from milliseconds to seconds. The source is not clearly understood but is reduced by cleaner processing. Good low noise processes should have no popcorn noise.

Summing Noise Sources

Noise Sources are random and therefore should be geometrically or RMS summed. The most well recognised formula for working out the total noise of an operational amplifier circuit which includes the different noise sources is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B} \quad \text{.....} \quad (1)$$

Where V_n = Voltage Noise of Op Amp

I_n = Current Noise of Op Amp

$4kTR_{ext}$ = Johnson Noise of external Resistors.

4.5.2. Noise Related to an Op Amp

There are typically two parameters specified in the datasheet of an operational amplifier, noise voltage and noise current;

Noise Voltage;

The noise voltage of a bipolar op amp is due to the Johnson noise of the base spreading resistor r_{bb} and the Shot noise of the collector current in the input transistors. There is also an error due to the flicker noise, associated with the input transistors base current flowing through the base resistors. At low frequencies the noise is dominated by the Flicker noise whilst at high frequencies, the Johnson noise is the major factor.

The noise voltage of a FET input amplifier is dominated by the Johnson noise of the channel resistance and is normally significantly higher than a bipolar design.

The noise voltage characteristics for both parts have a 1/f characteristic although the 'corner frequency' of FET input designs is typically much higher than for bipolar. It should also be noted that CMOS designs have a worse 1/f noise compared with Bifet op amps, but newer products developed using 'cleaner' CMOS technologies such as LinCMOS™ have greatly improved the noise performance and lowered the 1/f corner frequencies.

The 1/f region of the noise curve of an amplifier is particularly critical when designing precision circuits which operate at relatively low frequencies - very common in instrumentation equipment. An op amp with a low 1/f corner frequency is essential.

Current Noise;

For operational amplifiers with a bipolar input stage, the noise current is caused by Shot noise variations of the base current and flicker noise of r_{bb}. FET input amplifiers have a noise current specification caused by the shot noise associated with the gate leakage of the input FETs, this is significantly lower than for bipolar designs.

An op amp's noise current flows through the external resistors of an op amp generating an error source equal to $\sqrt{I_n^2 R_{ext}^2 B}$ - therefore the larger the external source resistors the larger the error due to noise current. Because the base current of a bipolar transistor is much higher than the leakage current of a FET transistor, the noise current of a CMOS or Bifet part is much lower than a bipolar design. FET input amplifiers are therefore normally used if a circuit has a large source resistance. As the bias

current of a FET input part doubles for every 10°C increase in temperature, the noise current, In, increases by $\sqrt{2}$ for every 10°C increase.

Equation (1) above, shows how these parameters are combined. The result from this equation is in fact an RMS term which is often preferred in its in its peak to peak form. If the RMS noise voltage is multiplied by 6.6, you have a 99.7% certainty that the peak to peak value will not exceed the result.

Further examination of equation (1) shows that there is a point at which the noise of a system is dominated by the external resistors. A term, of particular use when talking about bipolar op amps is the 'Equivalent Noise resistance', equal to V_n/I_n shows when the errors due to the noise current are than that due to the noise voltage

4.5.3. Noise Bandwidth

It can be seen from equation (1), that the Noise Bandwidth of the operational amplifier circuit is critical - the wider the frequency of operation the larger the amount of noise within that system. A low noise circuit must therefore have its noise bandwidth limited as much as is possible.

The Noise Bandwidth of an operational amplifier circuit is normally limited by using a filter network. It must be remembered however that the Noise Bandwidth is often very different to the RC Bandwidth of the filter which is limiting the noise. If a filter has a slow roll-off then the noise contribution by the signals with a higher frequency than the RC bandwidth can be significant. The Noise Bandwidth of a 1st order low pass filter (butterworth) is 1.57 x f_{3dB} of the filter. This is an increase of over 50%. A filter is of least 2 orders is normally recommended.

FILTER ORDER	NOISE BANDWIDTH
1	1.57 x f_{3dB}
2	1.11 x f_{3dB}
3	1.05 x f_{3dB}
4	1.03 x f_{3dB}
"Brick Wall"	1.00 x f_{3dB}

Noise on Output

Most noise calculations will work out the equivalent total noise on the input of the op amp. Like other errors this noise error is multiplied by the closed loop gain to give the equivalent noise on the output of the op amp.

4.6. Noise Vs Technology

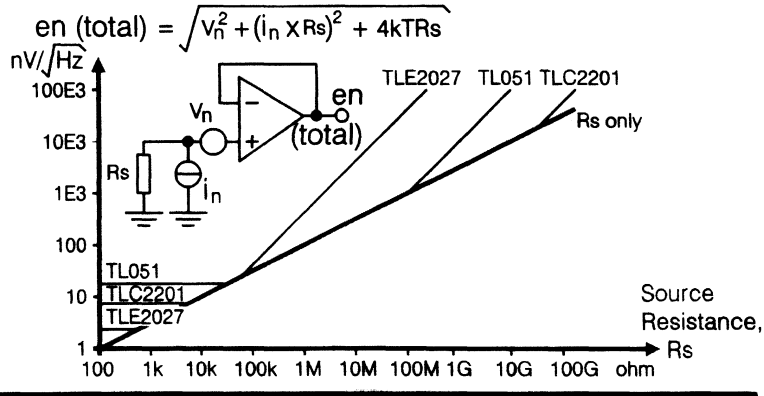
The previous figure discussed the relevance of noise voltage and noise current and how depending upon the source impedance each or both may be of importance. The graph and table in the figure above compares the overall noise performance of low noise op amps from each major technology. The formula to remember is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B}$$

V_n = Noise Voltage of Op Amp

I_n = Noise Current of Op Amp

$4kTR_{ext}$ = Noise of Resistors.



PROCESS	BIPOLAR	EXCALIBUR	BIFET	LinCMOS		
PARAMETER	NE5534	TLE2027	TL051	TLC1078	TLC2201	UNIT
Noise Voltage	3.5	2.5	18	68	8	$nV/\sqrt{Hz}$
Noise Current	400	400	10	0.5	0.6	$fA/\sqrt{Hz}$
1/f Corner	100	3	100	30	50	Hz

Noise Vs Technology

This figure shows that bipolar amplifiers are the best for a that, providing the source resistance is small, low noise voltage. Amplifiers like the TLE2027 have extremely low noise voltage specifications which means that, providing the source resistance is small, they achieve the best overall noise performance.

As the size of the external resistors increases, the Johnson noise of these components begin to dominate the total noise equation. Not surprisingly, the lower the value of the op amps noise voltage, the smaller the resistor needs to be before it begins to prevail - resistor size can prove a severe limitation when designing low noise circuits with low noise op amps.

As the source impedance increases, there comes a point when the noise current, In, flowing through these resistors dominates the total noise equation. Because bipolar resistors have a significantly higher noise current than FET input amplifiers, this error term can quickly cause the largest error. Low noise CMOS designs like the TLC2201 have such a low noise current specification, combined with a

relatively low noise voltage, that it is often the best choice even with medium sized external source impedances.

The other specification highlighted by this figure is the 1/f corner frequency of the op amp. Low noise bipolar designs will normally have much lower specifications than FET input designs (3 Hz for the TLE2027), although again, the TLC2201 has a very good specification relative to other FET input designs. It is worth noting that the NE5534 has a high 1/f corner frequency and yet it is still recognised as a low noise part - 1/f should not necessarily be used to compare the performance of different amplifiers.

4.7. Low Noise PIN Diode Interface

When interfacing to a wide variety of sensors the key factors in deciding which op amp will be used in the application are high input impedance, low input offset voltages and low noise voltages. A device perfect for applications requiring these specifications is the **TLC2201**.

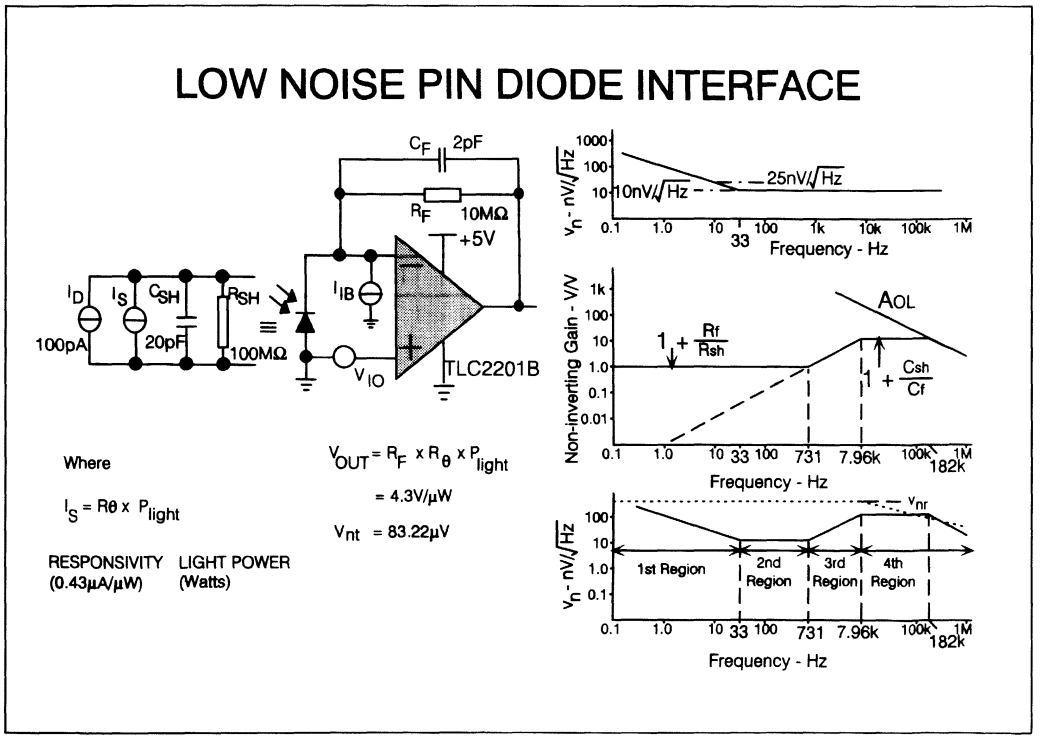


Figure 1.20 Low Noise PIN Diode Interface

No application shows the need for such parameters more clearly than when interfacing to a PIN photo-diode. Once again as in most applications requiring high input impedances it is the bias currents which are of importance, as feedback will multiply the op amp's input impedance by the circuit's loop-gain.

When using a PIN diode a small `dark' current will flow through it. This dark current is the bias current of the PIN diode. In parallel with the dark current is the current which is due to the light shining onto the device. It is the dark current along with the current noise which decides the error floor of the system. So if the dynamic range is not to be severely degraded the input bias currents of the op amp should be smaller than the dark current of the PIN diode. A typical PIN diode such as hp's 5082-4204 has maximum dark current of 100 pA (at zero voltage bias and at 25°C). The TLC2201 with a maximum bias current of 20 pA (calculated from the maximum bias current specifications over temperature) at 25°C provides a good safety margin.

The PIN diode is a light power to current converter and as such needs to interface to a trans-impedance amplifier. The result is that in order to get the required gain the feedback resistor of the op amp will normally have to be large. This feedback resistor will form a pole with the shunt capacitance of the diode and the op amp's input capacitance, which can lead to instability. Although this effect may well be reduced by the parasitic board capacitance which is in effect in parallel with the feedback resistor. This `feedback' capacitor can be increased to reduce the circuit's wideband noise, but this will reduce the application's bandwidth. Hence the required gain decides the value of R_f and the required signal bandwidth decides C_f. As well as converting the signal current to a voltage, the large feedback resistor adds to the offset voltage of the op amp by multiplying the bias currents of the op amp and the dark current of the PIN diode by its value.

The equivalent model of a PIN diode contains a shunt resistance, R_{sh}, which coupled to the feedback resistor gives the op amp a non-inverting gain of $1+R_f/R_{sh}$ (which frequently exceeds unity). It is therefore very important to use an op amp with low offset voltages and drift. The PIN diode's shunt capacitor also provides a limit to the range of frequencies over which the diode can be operated. Like all semiconductor barrier capacitances it is very voltage dependent, and can be reduced by placing a negative voltage across the diode.

The overall low frequency output voltage will therefore consist of the following factors:-

$$Vo = R_f * R_\phi * P_{light} + R_f * I_D + V_{IO} * \left(1 + \frac{R_f}{R_{sh}}\right) + R_f * I_{IB}$$

where R_ϕ is the responsitivity of the diode to light power (in amperes per watt), and P_{light} is the amount of light falling onto the diode's sensitive area (in watts).

The temperature effects of the PIN diode dominates any drift effects of the op amp's V_{IO}. R_{sh} will tend to halve every 10°C, just as the bias currents will tend to increase. The 0.5 µV/°C (typical) drift of the TLC2201 will be swamped by the change in gain due to R_{sh}.

As with all high impedance applications, the input stage is very susceptible to interference and leakage from the board. Any current injection into the input can be converted into millivolts of offset error. For this reason, it is standard practice for guard rings to be placed around the inputs of the op amp, reducing the influence of interference around the board. To decrease leakage of the board a Teflon based board will normally give the best performance.

In addition to offset errors, which are DC, noise errors will be introduced due to the PIN diode's noise and the op amp's noise.

The noise current will be the shot noise due to the dark current of the PIN diode and the bias current of the op amp. The noise current of the TLC2201 is 2.53 $fA/\sqrt{Hz}$ while the dark current of the PIN diode

would generate 5.66 fA/$\sqrt{Hz}$. The feedback resistor will generate noise due to the noise currents of the PIN diode and the op amp and also its own thermal noise. A 10 MΩ resistor generates 62 nV/$\sqrt{Hz}$ (due to shot noise of the PIN diode and op amp) and 406 nV/$\sqrt{Hz}$ (due to thermal noise). At these values the noise voltage of the TLC2201 (guaranteed to 25 nV/$\sqrt{Hz}$ at 10 Hz) would seem to be negligible, but the shot noise and thermal noise appear directly on the output of the op amp while the op amp's noise voltage will be multiplied by the op amp's gain. The op amp's gain will increase above the low frequency gain to 1 + C_{sh}/C_f. This gain will only be band-limited by the op amp's unity gain bandwidth. The non-inverting gain can rapidly increase over temperature (due to the large variance in R_{sh}, at a faster rate than the current noise, so a low noise voltage device is the best solution.

The non-inverting gain of the TLC2201 is:-

$$G_{cl} = 1 + \left(\frac{R_f}{1 + s * R_f * C_f}\right) * \left(\frac{1 + s * R_{sh} * C_{sh}}{R_{sh}}\right)$$

At low frequencies the R_f/R_{sh} ratio will dominate, and at higher frequencies the C_{sh}/C_f ratio will decide the noise and ac. gain. The poles of the circuit will be at:-

$$f_1 = \frac{1}{2\pi}\left(\frac{1}{C_{sh} + C_f}\right) * \left(\frac{R_{sh} + R_f}{R_{sh} * R_f}\right)$$

$$f_2 = \frac{1}{2\pi * R_f * C_f}$$

With R_{sh} = 100 MΩ, R_f =10 MΩ, C_{sh} = 20 pF and C_f = 2 pF the poles are at f_1 = 731 Hz and f_2 = 7.96 kHz. f_2 will also be when the trans-impedance gain of the TLC2201 starts to roll off.

At low frequencies the noise voltage of the TLC2201 will be amplified by 1.1 but at the higher frequencies it will be amplified by 10. This splits the noise curve into three distinct parts; the low frequency gain, transition gain and the high frequency gain. At higher frequencies the gain bandwidth product will reduce the gain. A further complication to the noise analysis is the flicker effect of the op amp's noise voltage, and so making 4 regions to the curve.

The first region is from virtually dc to the 1/f corner frequency of the TLC2201B which is of the order of 33 Hz. Over this region the noise voltage of the TLC2201 follows this approximate equation:-

$$v_n^2 = \left(\frac{v_{n(10)}^2 - v_{n(1k)}^2}{f} * 10\right) = \frac{4810 * 10^{-18}}{f}$$

Where $v_{n(10)}$ is the noise voltage specification at 10 Hz, $v_{n(1k)}$ is the specification at 1 kHz.

Calculating the noise over the region of 0.01 Hz to 33 Hz (ignoring the noise below 0.01 Hz) and adapting that equation yields

$$V_{n1}^2 = 4810 * 10^{-18} * \left(1 + \frac{R_f}{R_{sh}}\right)^2 * \ln\left(\frac{f_c}{f_a}\right)$$

$$V_{n1} = 69.35 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{\ln \frac{100}{0.01}} \quad \text{nV}$$

$$= 231.5 \text{ nV}.$$

The second region will cover the frequency range 33 Hz to 731 Hz. Over this frequency range the noise voltage is `white' and so has equal power per unit frequency and so the noise included over this range is calculated as follows:-

$$V_{n2} = v_{nwhite} * \left(1 + \frac{R_f}{R_{sh}}\right) * \sqrt{f_1 - f_c}$$

$$= 12 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{731 - 33} \quad \text{nV}$$

$$= 348.7 \text{ nV}$$

The third region is where the resistances are being shunted out by their parallel capacitances, here the gain is increasing by 20 decibels per decade. By extrapolating this curve down to the 1 Hz point the noise produced can be considered as increasing with frequency, simplifying the calculation. The equation of this line is:-

$$v_{n(1Hz)} = \left(1 + \frac{Rf}{Rsh}\right) * \left(\frac{v_{n(1kHz)}}{f_1}\right)$$

The noise content within the f_1 to f_2 band will be the area under this curve, the actual integration will be of the noise voltage squared. Therefore the noise content over this region results in the following equation:-

$$V_{n3} = \left(1 + \frac{R_f}{R_{sh}}\right) * \left(\frac{v_{n(1kHz)}}{f_1}\right) * \sqrt{\frac{f_2^3}{3} - \frac{f_1^3}{3}}$$

$$= 1.1 * \frac{12}{731} * \sqrt{\frac{(7.96*10^3)^3}{3} - \frac{731^3}{3}}$$

$$= 7.40 \ \mu\text{V}$$

Over the fourth region the noise is flat, but the gain then starts to follow the open loop characteristic of the op amp. This introduces a bandwidth limit of:-

$$BW = \frac{B_1}{1 + \frac{C_{sh}}{C_f}} - f_2$$

BW will be multiplied by $\pi/2$ to achieve the noise bandwidth, hence the noise voltage contained in the fourth region has this characteristic:-

$$Vn4 = v_{n(1kHz)} * \left(1 + \frac{C_{sh}}{C_f}\right) * \sqrt{\frac{\pi}{2} * BW}$$

$$= 12 * \left(1 + \frac{20}{2}\right) * \sqrt{\frac{\pi}{2} * 174 * 10^3}$$

$$= 69.0\ \mu V$$

In addition to the noise voltage from the amplifier, there will be the noise voltage due to the thermal noise of the feedback impedance and to the noise voltage generated by noise current through the feedback impedance.

Only the real part of the feedback impedance produces noise and just as the signal gain rolled off at f_2 so will the thermal noise. The thermal noise will therefore follow this characteristic:-

$$V_{nr} = \sqrt{4kTR_f} * \sqrt{f_2 * \frac{\pi}{2}}$$

$$= 45.4\ \mu V$$

The noise current will generate a noise voltage equal to:-

$$V_{nc} = i_n * Re\left(\frac{R_f}{1 + s * R_f * C_f}\right)$$

$$= \sqrt{5.66^2 + 2.53^2} * 10\text{-}15 * R_f * \sqrt{f_2 * \frac{\pi}{2}}$$

$$= 6.93\ \mu V$$

The total noise voltage will be the RMS sum of all noise voltages:-

$$V_{nt} = \sqrt{V_{n1}^2 + V_{n2}^2 + V_{n3}^2 + V_{n4}^2 + V_{nr}^2 + V_{nc}^2}$$

$$= \sqrt{0.231^2 + 0.349^2 + 7.40^2 + 69.0^2 + 45.4^2 + 6.93^2}$$

$$= 83.22\ \mu V$$

Comparing each of the noise voltages over each region, the overall output noise voltage is dominated by the thermal noise of R_f and the out of frequency of interest bandwidth noise voltage of the op amp.

The signal to noise ratio relative to R_f is $\sqrt{R_f}$, so as R_f increases the output increases, the thermal noise increases but at a much reduced rate.

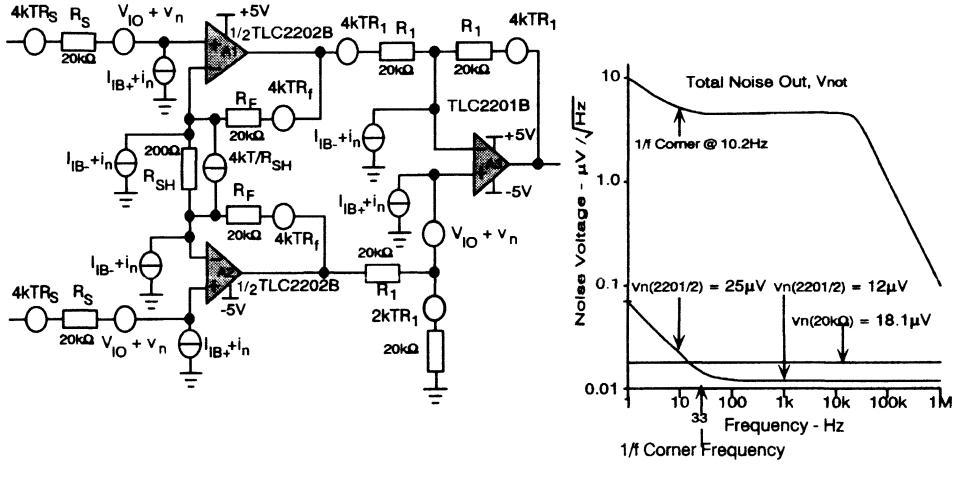
The noise of the op amp in region 4 can be reduced by increasing C_f, but this reduces the bandwidth of the application, and C_f will normally have been chosen to meet the application's requirements. A better way of reducing this high frequency noise is to reduce the op amp's high frequency gain by reducing

the value of C_{sh}. This can be done by applying a negative voltage across the diode. The effect of this is to raise the frequency of f_1 whilst lowering the high frequency gain of the op amp.

In the application shown the common mode range of the TLC2201 is being exploited in a single rail circuit making the application of a negative voltage across the diode impossible.

Another point to note is that the speed of this application is limited by C_f and not the op amp, if a faster application was required the trans-impedance gain would need to be reduced, but this would also reduce the signal to noise ratio of the application.

4.8. High Precision Low Noise Amplifier



High Precision Low Noise Amplifier

When designing low noise systems the voltage noise of the amplifier is not the only important parameter. The wide variety of transducers, and their resistances, can often make the noise voltage of the op amp negligible when compared to the Johnson noise of these resistances. With very high impedance transducers the noise current of the amplifier dominates the total circuit noise.

In most applications involving the **TLC2201B** and **TLC2202B** operational amplifiers the thermal noise of the source and/or feedback resistors will be the most important. This is due the TLC2201/2 having a maximum noise voltage of only 12 nV/$\sqrt{Hz}$ and a noise current of 2.53 fA/$\sqrt{Hz}$ (@25°C), giving it

an effective noise resistance (ratio of noise voltage to noise current) of above 4 MΩ. This means that only when dealing with impedances above 4 MΩ is the effect of the noise current of the TLC2201 going to be larger than its noise voltage. The offset error that this impedance would create would be 80 μV.

Instrumentation Amplifier

The 3 op amp instrumentation amplifier is a versatile configuration and can be used to yield the best performance from an op amp; in particular the TLC2201 with its high input impedance, good common-mode rejection ratio as well as its excellent input and output swings.

As in most low noise systems the input stage will have the largest effect on the signal to noise ratio. Using the TLC2202 in the input stage makes use of its very low noise currents and noise voltages as well as its very low offset voltage. The common-mode range down to the negative rail adds further versatility to the application whilst maintaining the accuracy required.

When working out the noise of a system it is best to relate each stage's noise to its input. This will normally make analysis easier, as both the input signal and the input referred noise will be multiplied by the op amp's non-inverting gain, $1+ R_f/R_{sh}$, (signals via the inverting input will be multiplied by $-R_f/R_{sh}$). The instrumentation amplifier configuration adds some further complexity to the analysis; with the input stage sharing a resistor, R_{sh}, between its two op amps' inverting input terminals. The use of R_{sh} is two-fold; A, R_{sh} provides the instrumentation amplifier with its good common-mode rejection characteristics, and B, R_{sh} sets the gain at $1+2R_f/R_{sh}$. With the input stage sharing R_{sh} between the two op amps it is easier to consider the thermal noise of R_{sh} to be in the form of a current ($4kT/R_{sh}$), which adds to the noise current of each op amp's inverting input.

The sources of noise for both input stage op amps will be the same. The non-inverting input will exhibit the noise voltage, v_n, of the op amp itself, in addition will be the thermal noise of the source resistor, $4kTR_S$, and the noise generated by the noise current, i_n, through R_S. These voltages are uncorrelated and will therefore RMS sum together. Due to the virtual short across the op amps' inputs (the very high open loop gain forces the two inputs together) the noise voltage at the non-inverting input will appear at the inverting input. This means that the total noise on the non-inverting input will be multiplied by the inverting gain of the opposing op amp in the input stage. So the noise generated on the non-inverting input, v_{ni+}, of each op amp will be:-

$$v_{ni+} = \sqrt{v_n^2 + 4kTR_S + i_n^2R_S^2}$$

The noise current on the inverting input will flow through the feedback resistor, R_f, creating a noise voltage at each op amp's output, which sums together with the thermal noise voltage of R_f. The noise current on the inverting input will be the noise current of the device plus the thermal noise current of R_{sh}. As this noise voltage is at the output of the op amp (just as the bias current error is added to the output of the op amp), referring it to the non-inverting input entails dividing it by the non-inverting gain. The resultant is the noise generated by a resistance equivalent to R_{sh} in parallel with R_f. This extra source generates further non-inverting input referred noise. However it will not appear at the inverting input, as the noise is actually being generated at the output.

Therefore the total noise voltage referred to the input, $v_{nri(1)}$, of amplifier A1 will be the noise generated at the non-inverting input summed with the noise due to the parallel combination of feedback resistor, R_f, and shunt resistor, R_{sh}. Therefore:-

$$v_{nri(1)} = \sqrt{v_{ni+(1)}^2 + i_{n(1)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)}$$

and the input referred voltage, $v_{nri(2)}$, of amplifier A2 will be:-

$$v_{nri(2)} = \sqrt{v_{ni+(2)}^2 + i_{n(2)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)}$$

The third amplifier will have a similar equation except that R_S will be replaced with $\frac{1}{2}R_1$ and $R_{sh}R_f/(R_{sh}+R_f)$ will be replaced with $\frac{1}{2} R_1$, yielding:

$$v_{nri(3)} = \sqrt{v_{n(3)}^2 + 2*4kT(\frac{1}{2} R_1) + 2 * i_n^2*(\frac{1}{2} R_1)^2}$$

The output of A1 (*and for A2*) will be $v_{nri(1)}$ ($v_{nri(2)}$) multiplied by the non-inverting gains RMS summed with $v_{ni+(2)}$ ($v_{ni+(1)}$) multiplied by its inverting gain. Assuming all op amps have the same worst case noise voltages and currents, the output noise voltage, $V_{no(1)}$ of A1 will be:-

$$V_{no(1)} = \sqrt{\left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + \left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2}$$

Op amp A2 will have a similar output noise voltage. The third op amp A3 will multiply the noise voltages from A1 and A2 by its inverting gain. It will RMS sum these together with its own noise voltage (which is multiplied by its own non-inverting gain), yielding a total output noise voltage, V_{not}, of:-

$$V_{not} = \sqrt{2 * \left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + 2 * \left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2 + 2 * v_{nri(3)}^2}$$

To maximise noise rejection, the gain of the first stage will normally be large while the gain of the last stage will be small (frequently, as here, unity to minimise any common-mode errors), and so reducing the effect of the final stage's noise. Using bipolar input op amps in the final stage will have a greater effect on the noise level due to their much larger noise currents. These larger noise currents place a compromise on the limit on the range of values for A3's source resistors, smaller source resistors generate less noise voltages, but load the input stage op amps' outputs introducing distortion.

With R_f=20 kΩ, R_{sh}=200 Ω, R_1=20 kΩ, R_s=20 kΩ the non-inverting gain of the input stage will be 101 and the inverting gain will be 100. These values coupled with the TLC2201B/2B's maximum noise voltage of 12 nV/$\sqrt{Hz}$ (guaranteed at 1 kHz) and noise current of 2.53 fA/$\sqrt{Hz}$ (calculated for 1 kHz) the following values are achieved.

For A1 and A2

$$V_{ni+} = 21.7 \text{ nV}/\sqrt{Hz}$$

$$V_{nri} = 21.8 \text{ nV}/\sqrt{Hz}$$

$$V_{no} = 3.10\ \mu V/\sqrt{Hz}$$

and for A3 $V_{nri} = 21.7\ nV/\sqrt{Hz}$

The resulting output noise voltage, V_{not}, spectral density for the TLC2201/2 instrumentation amplifier will be:-

$$V_{not} = 4.39\ \mu V/\sqrt{Hz}.$$

Referring this value to the input (dividing by the signal gain = 201) implies an input referred noise voltage of 21.8 $nV/\sqrt{Hz}$. This value is dominated by the thermal noise of the source resistor, with a low noise bipolar op amp the noise would be dominated by the noise current of the device. So when interfacing to high impedances the TLC2201/2 provides a very low noise and a highly accurate solution.

4.9. Resolve Displacement with 12 Bit

4.9.1. Measure Position with an LVDT

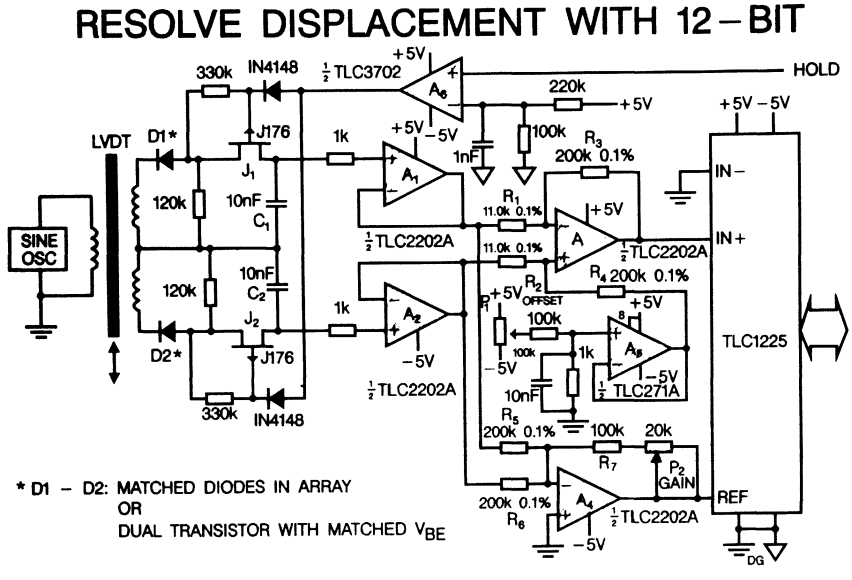
The field of robotics represents an almost limitless arena for high resolution position sensing in mechanical systems. For that purpose, a transducer - the Linear Variable Differential Transformer (LVDT) is often employed. When combined with precision conditioning TLC2202 op amp circuitry and a 12-bit plus sign TLC1225 a/d converter, high resolution measurements of displacement are possible from ±5V supplies.

An LVDT is a transformer with a mechanical moveable core. The primary is driven by a sine wave, usually amplitude stabilised. Sine drive eliminates error inducing harmonics in the transformer. The two secondary windings are connected in opposed phase. When the core is positioned in the magnetic centre of the transformer, the secondary outputs cancel and there is no output. Moving the core away from the centre position unbalances the flux ratio between the secondary windings, developing an output.

Signal conditioning circuits for LVDT outputs involve rectification and smoothing to convert the AC signal into a DC signal proportional to position. Rectification circuits vary from simple half wave rectifiers to complex synchronous demodulators. After filtering or smoothing, the DC signal can then be simply digitised by an a/d converter.

Application Circuit Features

The LVDT in this application has its centre between the two secondary windings grounded. The amplitudes of the secondary coils' output signals are directly proportional to the core position and are also each other's complement. As the core moves, one output rises while the other falls. Despite using simple detector diodes, D_1 and D_2, to rectify the AC signals from the transducer, the circuit obtains many high performance features.



Resolve Displacement with 12 Bit

The application incorporates a sample and hold circuit that keep the detectors output stationary during a conversion. The rectified signal is sampled on the hold capacitors, C_1 and C_2, and held constant while the a/d conversion takes place. Low leakage JFET switches, J_1 and J_2, in addition to CMOS inputs on the TLC2202 op amps, A_1 and A_2, prevent discharging and give a low droop rate. The differential, rectified and held LVDT output is then amplified by a differential amplifier, formed by the TLC2202 CMOS op amps, A_1, A_2 and A_3.

Summing the outputs of the two secondary windings by A_4, and using this signal as the converter's reference has two very definite advantages. It helps eliminate any need for precision stabilisation of the oscillator's amplitude. It also obviates compensating for temperature dependent gain changes in the transformer. Using this approach ensures that such common mode signals have no effect on the digitised output of the a-d converter.

Why Use the TLC2202 Advanced LinCMOS Op Amp?

The TLC2202 is an ideal op amp for precision applications operating from low supply voltages and requiring rail-to-rail output swing. Particularly for A_1 and A_2 in this application:

- A very low input bias current is essential to prevent discharging of the hold capacitors C_1 and C_2. TLC2202's CMOS inputs ensure a maximum input bias current of 100 pA over temperature.
- A common mode input range and output swing close to the negative supply are required. TLC2202 fully support these needs and has even a common mode input range to the negative rail.
- The input offset voltage must be low and stable enough to allow reliable trimming of the system offset to 12 bits accuracy. The 500 μς maximum offset of the TLC2202 is just acceptable.
- As a high common mode voltage is present on the inputs of A_1 and A_2, a good common mode rejection is necessary to prevent excess offset and offset drift. The minimum 85 dB over temperature adds little additional offset error and insignificant offset drift over common mode voltage variations.

Particularly for A_3 and A_4 in this application:

- Low input offset and rail-to-rail output swing. TLC2202's outputs swing very close to both supply rails provided that it is not loaded heavily.

4.9.2. Design Details

Transducer

The chosen component design assumes a LVDT with a maximum differential linear output voltage of ±250 mV peak. The outputs of the two secondary windings are assumed to be centred around 4V peak, which make up the common mode voltage. This leaves some room for variations in the sine wave amplitude due to oscillator drift and transformer transfer ratio changes with temperature, which the circuit compensates for as previously described.

Rectifier plus Sample and Hold Circuit

It is essential that the two rectifier diodes D_1 and D_2 have identical voltage drops and that their drops track with temperature. Two matched diodes in an array should be used. Alternatively, a double transistor with precision matched V_{BE} characteristics could be used as rectifying diodes by connecting the base and collector of each transistor. Be aware that reverse bias protection diodes in some double transistors prevent this use. A rectification resulting in a negative output voltage was chosen as the common mode range of the succeeding TLC2202 op amps have a wider negative than positive common mode range.

P-channel JFET switches J_1 and J_2 were chosen to allow switching with the available ±5V supplies (the source signals can be close to -5V, so n-channel JFETs would require a minimum turn-off voltage of $V_{GS(OFF)}$ - 5V, corresponding to -8 to -10V for most devices). The 330 κΩ gate-source resistors keep the gate-source voltages equal to zero volts in the switches on-state condition. In off-state, the gates are brought close to +5V by the switch control comparator, A6, which interfaces directly to logic signals. It is possible to control p-channel JFETs directly from logic levels but the used TLC3702 LinCMOS comparator provides better isolation from digital glitch noise.

The values of C_1 and C_2 were chosen to provide a low droop rate during the hold period, where leakage from the inputs of A_1 and A_2 plus the JFETs discharge the capacitors. The droop rate, dV/dt, can be calculated from:

$$\frac{dV}{dt} = \frac{I_{leakage}}{C};$$

Differential Amplifier

A standard instrumentation three op amp configuration is used for the differential amplifier. The purpose of the first two amplifiers, A_1 and A_2, is to buffer the voltages hold on C_1 and C_2. The third amplifier, A_3, acts as a differential amplifier providing the common mode suppression. The gain setting resistors, R_1, R_2, R_3 and R_4, used, must be well matched to achieve good common mode rejection - preferably better than 0.1%, to give more than 60 dB rejection. The gain has been accommodated to give full scale for a ±250 mV peak transducer signal. To remove transducer offset plus op amp offsets an adjustment is included. A single TLC271A LinCMOS op amp, A5, buffers the potential divider circuit around P_1. Stability of this adjustment rely on supply rail drift tracking within 1%.

Reference Amplifier

The sum of the two secondary outputs is used to generate a ratiometric reference voltage. Op amp A_4 sums the two signals through R_5 and R_6. Precision tracking of these resistors is required to ensure a reference input voltage, REF, whose level depends only on the sum of the two secondary voltages. The potentiometer, P2, sets the full scale range, which of course most be equal to or higher than the IN+ voltage to the a/d converter. Any changes in the sine oscillators amplitude, transformer transfer ratio over temperature or other common mode errors are cancelled with this arrangement. The voltage levels set at the IN+ and REF pins should allow for some room for such common mode drift.

A-D Converter

TLC1225 is a self-calibrating 12-bit plus sign bipolar or 12-bit unipolar a/d converter with 10 ms conversion time. In unipolar configuration, only a single +5V supply is required. Bipolar mode, as used in this application, needs however dual supply rails but provides a ±5V input range. The differential input voltage is converted ratiometric to the reference input and converted to a parallel word, which interfaces directly to a 16-bit data bus.

Software controlled self-calibration allows calibration of the a/d converter at power up, before every conversion cycle or whenever appropriate. This feature ensures long term stability, preventing frequent re-calibration of the application and avoid expensive initial trimming at the factory.

4.10. Measure Piezo AC - Signals with Charge Amplifiers

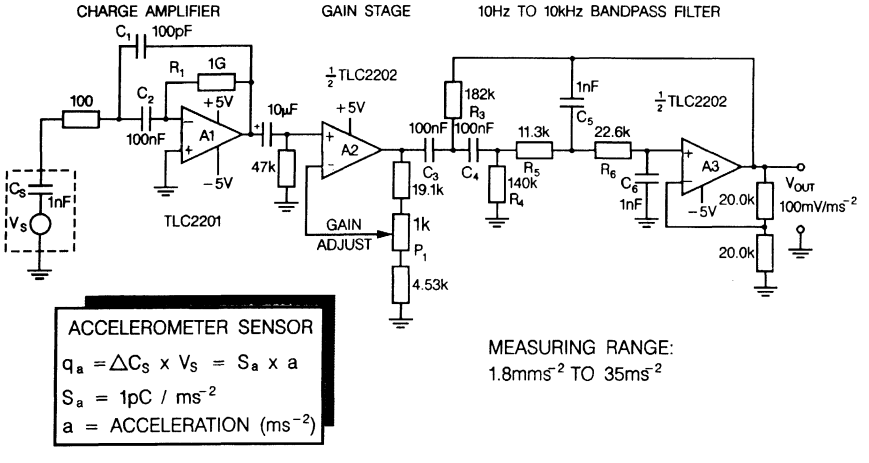
4.10.1. Piezo Transducer Interfaces

When interfacing op amps to piezo transducers, two basic modes are employed; Voltage mode or Charge mode. Both principles require an op amp with very high input impedance and low bias current, which limits the choice to JFET or CMOS input op amps. The dynamic range of such interfaces to piezo transducers that exhibits AC signals, is usually limited by the noise produced by the op amp. The TLC2201 and TLC2202 are Advanced LinCMOS op amps that challenge the input noise of the very best JFET input op amps and are simultaneously capable of operation from low supply voltages.

Voltage mode operation requires that the op amp is placed very close to the sensor as parasitic load capacitance on the sensor output will change its sensitivity. A cable between the sensor and the op amp will not only attenuate the sensor's output - but variations in the cable capacitance due to mechanical influence easily modulates the desired signal. When voltage mode configuration is used, the amplifier is usually encapsulated together with the sensor such as in electric microphones.

MEASURE PIEZO AC – SIGNALS WITH CHARGE AMPLIFIERS

ACCELEROMETER AMPLIFIER



Measure Piezo AC - Signals with Charge Amplifiers

Charge mode operation is widely used, primarily because the influence from any shunt capacitance across the sensor is eliminated. Consequently, the length of a connected cable will not influence the sensitivity but affect only the maximum bandwidth of the measuring system.

Accelerometer Application

The illustrated application converts an acceleration input, a, measured by a piezo electric acceleration sensor and conditioned by an accelerometer amplifier, to an output voltage, V_{out}, proportional with the sensed acceleration. The circuit provides a wide dynamic range thanks to the very low input noise and rail-to-rail output swing of the Advanced LinCMOS op amps, TLC2201 and TLC2202 used. Additionally, the entire circuit operates from ±5V supplies, ensuring overall low power consumption.

The accelerometer amplifier consist of three sections, a charge amplifier that converts the sensor output charge to a voltage, a gain stage and a 10 Hz to 10 kHz bandpass filter, which limit the amplifier's noise bandwidth.

If an accelerometer sensor with a sensitivity of 1 pC/ms^{-2} is employed, a maximum full scale rms acceleration of 35 ms^{-2}, or approximately 36g can be measured. The lowest acceleration that can be detected is determined by the charge amplifier's noise. Assuming typical system noise with a minimum of 5 dB S/N ratio, vibration or acceleration levels down to 1.7 mms^{-2} corresponding to 0.17 mg are theoretical measurable.

Sensor

The equivalent electrical model of a piezo electric acceleration sensor can be thought of as a voltage source, V_S, in series with a small sensor capacitor, C_S. Variations in capacitance due to physical deformation will cause charge, q_a, to be dumped into the charge amplifiers summing junction. Characteristic parameters for such a sensor are the sensitivity, S_a, and the sensor capacitance, C_S.Their relationship to the produced charge, q_a, is given by:

$$q_a = \Delta C_S * V_S = S_a * a \; ; \quad \text{where a = acceleration ;}$$

The sensor (B&K type 4384) used in this application has the following typical parameter values: S_a = 1 pC/ms^{-2} and C_S = 1 nF.

Charge Amplifier

The purpose of the charge amplifier is to transform the high output impedance of the acceleration sensor and amplify its relatively weak signal. A basic charge amplifier consist of a high gain operational amplifier with a feedback capacitor. When charge is dumped into the amplifier's summing junction from the sensor, the amplifier manipulate its output voltage to maintain the charge in the feedback capacitor equal to the charge dumped into the input, so that the voltage in the summing junction tends to be at null. For the actual application, A_1 is acting as charge amplifier and C_1 is the feedback capacitor. Ignoring the effect from R_1, C_2 and the 100Ω input resistor, the transfer function from acceleration input to A_1's output voltage, E_{o1} becomes:

$$E_{o1} = -\frac{q_a}{C_1} = -\frac{S_a}{C_1} * a \Leftrightarrow \frac{E_{o1}}{a} = -\frac{S_a}{C_1} ; \quad (1)$$

By insertion of actual component and parameter values, (1) becomes:

$$\frac{E_{o1}}{a} = -\frac{1\ pC/ms^{-2}}{100\ pF} = -10\ mV/ms^{-2} ; \quad (2)$$

If higher vibration or acceleration levels than 36g have to be measured, C_1 can be increased to reduce the gain of the charge amplifier.

A large feedback resistor, R_1, provides a leakage path for A_1's input bias current and prevents the op amp's output from being driven into saturation. As R_1 together with C_1 forms a highpass filter with a 3dB frequency, $f_O = 1/(2\pi R_1 C_1)$ = 1.59 Hz; the value of R_1 needs to be vary large if low frequencies are of interest. The exceptional large value of 1 GΩ is chosen because the effect of its thermal noise decreases as R_1 increases. This is discussed in the noise evaluation section. An upper limit of R_1 is given by the offset produced when A_1's input bias current passes through it. With TLC2201's 100 pA

maximum input bias current over temperature, a worst case offset of (1 GΩ * 100 pA) = 100 mV is generated. However, as the maximum signal output from A_1 is only 500 mV peak, no limitations on the op amp's output swing follows. To prevent swing limitations on the succeeding gain stage, the charge amplifier's output is AC coupled.

To avoid A_1's input bias current from contributing to the charging of C_1, a DC blocking capacitor C_2 is placed between the very high impedance AC summing junction and the op amp's inverting input terminal. The effect of C_2 on the transfer function can be ignored with the value chosen. A 100Ω resistor in series with the charge amplifier's input provides some protection, when the sensor is disconnected. A lowpass filter is formed together with C_1 but at frequencies beyond interest. Thermal noise from 100Ω will not affect the overall accelerometer amplifier's noise performance.

Charge amplifiers very high input impedance require carefully layout, PCB cleaning and guarding. The summing junction would benefit from Teflon stands. Both capacitors should be of a low leakage type such as polypropylene, polystyrene or Teflon.

Gain Stage

A simple non-inverting gain stage is implemented by one half of a low noise TLC2202 op amp to boost the charge amplifier's output voltage five fold. Additionally, the gain stage around A_2 allow for ±10% gain adjustment with P_1 to accommodate variations in the sensitivity of the sensor. The gain should be adjusted to yield an overall accelerometer amplifier output voltage, V_{out}, of 100 mV/ms^{-2}. Thermal noise from the potential voltage divider, does not contribute to the total system noise.

TLC2202's output stage features near rail-to-rail output swing with the load impedance provided.

Filter

Following the gain stage is a 10 Hz to 10 kHz bandpass filter, implemented around the second half of TLC2202. The purpose of this filter is to remove low frequency excess noise and limit the upper noise bandwidth. In fact, the bandpass filter consists of a combined 2nd order 10 Hz highpass and 2nd order 10 kHz lowpass filters with Butterworth characteristics. Design of this filter section assumes no mutual interaction between the two filter sections. This is only possible because the cut off frequencies are so far apart and that an impedance level has be chosen to minimise interaction.

Design details of the filter are trivial and only covered briefly. Assumptions: $\omega_{oHP} = 1/(2\pi * 10\ Hz)$, $\omega_{oLP} = 1/(2\pi * 10\ kHz)$, a midband gain of two and a 2nd order maximum flat or Butterworth Q factor, $Q = 1/\sqrt{2}$. The transfer function, H(s), can then be shown to be given by:

$$H(s) = \frac{s^2}{s^2 + \left(\frac{1}{R_4C_3} + \frac{1}{R_4C_4} - \frac{1}{R_3C_3}\right)s + \frac{1}{R_3R_4C_3C_4}} * \frac{\frac{1}{R_5R_6C_5C_6}}{s^2 + \left(\frac{1}{R_5C_5} + \frac{1}{R_6C_5} - \frac{1}{R_6C_6}\right)s + \frac{1}{R_5R_6C_5C_6}}; \quad (3)$$

$$H(s) = \frac{s^2}{s^2 + \frac{\omega_{oHP}}{Q} s + \omega_{oHP}^2} * \frac{\omega_{oLP}^2}{s^2 + \frac{\omega_{oLP}}{Q} s + \omega_{oLP}^2} \quad ; \quad (4)$$

Comparing (3) and (4) yields the following design equations and component values:

Highpass: Choose $C_3 = C_4 = C = 100\,nF$;

$$R_3 = \frac{\frac{1}{Q} + \sqrt{\frac{1}{Q^2} + 8}}{4\omega_{oHP} C} = 182.1k\Omega \cong 182k\Omega \text{ (E96 value)};$$

$$R_4 = \frac{4}{\omega_{oHP} C} \frac{1}{\sqrt{\frac{1}{Q^2} + 8} + \frac{1}{Q}} = 139.1k\Omega \cong 140k\Omega \text{ (E96 value)};$$

Lowpass: Choose $C_5 = C_6 = C = 1\,nF$;

$$R_6 = \frac{1}{Q\,\omega_{oLP} C} = 22.51k\Omega \cong 22.6k\Omega \text{ (E96 value)}$$

$$R_5 = \frac{1}{R_6 C^2 \omega_{oLP}^2} = 11.25k\Omega \cong 11.3k\Omega \text{ (E96 value)};$$

Why use Advanced LinCMOS TLC2201 and TLC2202 Op Amps?

The charge amplifier requires a CMOS or JFET input op amp with very low input voltage and noise current. In addition, the input bias current should be as low as possible to avoid excess offset that limits the dynamic range.

For the gain stage and filter section, a relatively low voltage and current input noise is still required. But more important is the low distortion rail-to-rail output swing providing output voltage levels, that easily interface to a connected sample & hold plus a/d converter circuitry.

If these essential needs are added to the demand for low cost, low power and low supply operation (±5V), the TLC2201 and TLC2202 are about the only op amps available meeting these requirements.

4.10.2. Noise Considerations

If a multi-stage amplifier is constructed such, that the input noise of the first stage multiplied with its gain is larger that the input noise of the succeeding stage etc., the first stage will dominate the noise of the total multi-stage amplifier. Following this principle, the charge amplifier's gain has been chosen to produce an output noise, E_n, significantly higher than the input noise of the gain stage. Consequently, the noise evaluation is focused on the noise produced by the charge amplifier in the bandwidth limited by the filter section. Wideband noise generated by A_3, (which is only limited by its falling open loop gain), is low and can be ignored.

Three sources dominates the output noise from the charge amplifier:

- $\mathbf{e_n}$, input noise voltage density from A_1, TLC2201; (e_n = 8 nV/$\sqrt{Hz}$ typical)
- $\mathbf{I_n}$, input noise current density from A_1, TLC2201 ; (i_n = 0.6 fA/$\sqrt{Hz}$)
- $\mathbf{R_1}$, thermal noise density generated by R_1 (1 GΩ), and equal to $\sqrt{4kTR_1}$;

Where k = 1.38 * 10^{-23} J/K (Boltzmann's constant; and T = 298 K (absolute temperature @ 25°C).

Assuming that the charge amplifier's input is shorted by the sensor's characteristic capacitance, C_S, and that C_2 and the 100Ω input resistor does not influence the noise, the charge amplifiers output noise density, $E_n(s)$, is given by:

$$E_n^2(s) = \left(1 + \frac{R_1 \parallel \frac{1}{C_1 s}}{\frac{1}{C_S s}}\right)^2 * \left(e_n^2 + i_n^2\left(R_1 \parallel \frac{1}{C_1 s} \parallel \frac{1}{C_S s}\right)^2 + 4kTR_1\left(\frac{\frac{1}{C_1 s} \parallel \frac{1}{C_S s}}{R_1 + \frac{1}{C_1 s} \parallel \frac{1}{C_S s}}\right)^2\right)$$

$$E_n^2(s) = e_n^2\left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1\, s + 1}\right)^2 + i_n^2 R_1^2\left(\frac{1}{R_1 C_1\, s + 1}\right)^2 + 4kT\, R_1\left(\frac{1}{R_1 C_1\, s + 1}\right)^2$$

The total rms noise measured on the charge amplifiers output can now be calculated from:

$$E_n(rms) = \sqrt{\int_{-\infty}^{\infty} |E_n(j2\pi f)|^2\, d(f)} \qquad s = j\omega = j2\pi f$$

To simplify this task, we will analyse the three components of $E_n^2(s)$, and determine which dominate in the frequency band of interest.

$$E_n^2(s) = E_{e_n}^2(s) + E_{i_n}^2(s) + E_{R_1}^2(s); \quad s = j\omega = j2\pi f \Rightarrow$$

$$|E_n(j2\pi f)|^2 = |E_{e_n}(j2\pi f)|^2 + |E_{i_n}(j2\pi f)|^2 + |E_{R_1}(j2\pi f)|^2;$$

$\mathbf{e_n}$ generated noise: $E_{e_n}(s) = e_n\left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1\, s + 1}\right)$;

$$|E_{e_n}(j2\pi f)| = e_n \sqrt{\frac{1 + \left(\frac{f}{f_{zero}}\right)^2}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Zero frequency: $f_{zero} = \frac{1}{2\pi R_1 (C_1 + C_S)} = 0.14$ Hz

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59$ Hz

Noise; $f << f_{zero}$: $e_n = 8\ nV/\sqrt{Hz}$ (typical)

Noise; $f >> f_{pole}$: $e_n\left(1 + \frac{C_S}{C_1}\right) = 88 nV/\sqrt{Hz}$ (typical)

i_n generated noise: $E_{e_i}(s) = i_n R_1 \left(\frac{1}{R_1 C_1 s + 1}\right)$;

$$|E_{e_i}(j2\pi f)| = i_n R_1 \sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59$ Hz

Noise; $f << f_{pole}$: $i_n R_1 = 600\ nV/\sqrt{Hz}$ (typical)

R_1 generated noise: $E_{R_1}(s) = \sqrt{4kTR_1}\left(\frac{1}{R_1 C_1 s + 1}\right)$;

$$|E_{R_1}(j2\pi f)| = \sqrt{4kT R_1} \sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59$ Hz;

Noise; $f << f_{pole}$: $\sqrt{4kTR_1} = 4.1\ \mu V/\sqrt{Hz}$;

Clearly, the current and thermal generated noise dominates at very low frequencies. The amplitude of the current generated noise, $|E_{in}(j2\pi f)|$, is reduced by -20 dB/decade above f_{pole}. Consequently, it has shrunken to the same level as the amplitude of the voltage generated noise, $|E_{en}(j2\pi f)|$, at:

$$\frac{i_n R_1}{e_n \frac{C_1 + C_s}{C_1}} \frac{1}{2\pi R_1 C_1} = \frac{i_n}{2\pi e_n (C_1 + C_S)} = \frac{600nV}{88nV} * 1.59\ Hz = 10.8\ Hz\ ;$$

Current generated noise has therefore no effect on the total noise in the 10 Hz to 10 kHz frequency band at 25°C. Note that the 10.8 Hz frequency remains constant with changes in R_1.

Similarly, the amplitude of the thermal generated noise, $|E_{R1}(j2\pi f)|$, equals the amplitude of the voltage generated noise, $|E_{en}(j2\pi f)|$, at:

$$\frac{\sqrt{4kTR_1}}{e_n \frac{C_1 + C_s}{C_1}} \frac{1}{2\pi R_1 C_1} = \sqrt{\frac{4kT}{R_1}} \frac{1}{2\pi e_n (C_1 + C_S)} = \frac{4.1\ \mu V}{88\ nV} * 1.59\ Hz = 74\ Hz\ ;$$

Consequently, thermal generated noise as well as current generated noise has little or insignificant effect on the total noise in the 10 Hz to 10 kHz frequency band. Note that the 74 Hz frequency decreases proportionally with increasing value of $\sqrt{R_1}$. The interesting point about R_1 is, that the current generated noise in the frequency range considered is unaffected and that a higher value reduces the thermal noise!

The conducted noise analysis clearly shows, that the charge amplifier's output noise density in the frequency range of interest is totally dominated by the noise voltage, $|E_{en}(j2\pi f)|$, generated by the TLC2201 op amp's input noise voltage, e_n. Calculating the total rms noise, $|E_n(rms)|$, on the output of the charge amplifier now becomes a simple task, as $|E_{en}(j2\pi f)|$ is constant from 10 Hz to 10 kHz. Integration of the noise density over the frequency band of interest can now be accomplished with a simple multiplication, yielding:

$$|E_n(rms)| = \sqrt{|E'_{e_n}(j2\pi f)|^2 * \text{Noise Bandwidth}}\ ;$$

Where $|E'_{e_n}(j2\pi f)|$ is equal to $|E_{e_n}(j2\pi f)|$ for $10Hz < f < 10\ kHz$. Inserting numbers gives:

$$|E_n(rms)| = \sqrt{|88\ nV/\sqrt{Hz}|^2 * (10\ kHz - 10\ Hz) * 1.11}$$

$$= 9.27\ \mu V\ rms;$$

Re-arranging the transfer function (1) for the charge amplifier can now be used to determine the corresponding input accelerations, a_n:

$$a_n = \frac{E_n(rms)}{S_a} C_1$$

$$= 0.927\ mms^{-2}\ ;$$

Assuming a minimum 5 dB S/N ratio, the typical lowest theoretical acceleration, a_{min} that can be measured is given by:

$$a_{min} = 0.927\ mms^{-2} * 10^{\frac{5\ dB}{20}}$$

$$= 1.65\ mms^{-2} \cong \mathbf{0.17\ mg\ acceleration}$$

However, these figures are reduced somewhat if a worst case calculation is performed. The major additional noise comes from:

- Worst case TLC2201A noise voltage is 50% higher and equal to 12 $nV/\sqrt{Hz}$, which raises the flat noise floor.
- Worst case TLC2201 noise current over temperature is much higher than the typical 0.6 fA @ 25°C, as it tends to double for every 10°C temperature increase. This temperature dependent effect results in an increasing low frequency noise with increasing temperature.
- Thermal noise from the feedback resistor increases with the square root of the temperature again adding to the low frequency noise.
- Noise sources from the succeeding gain op amp and filter contribute slightly to the total noise with the component values and gain chosen.

4.11. When is an Op Amp Single or Dual Supply?

There are a number of fundamental differences between operational amplifiers that have been developed for either single or dual supply applications. Many design problems are caused by an engineer using an op amp with the wrong configuration of power supplies. By understanding a few basic ground rules, often technology related, it is possible to ensure an op amp is always used correctly.

Transistor Type on Input

A single supply op amp should have a Common Mode input voltage range that includes the negative supply rail (usually ground) and have an output that also swings very close to this rail.

A Common Mode input range that includes the negative rail can be achieved by using the following transistor types on the op amp's input; PNPs, 'P-Channel' Mossiest or 'N-Channel' JFETs. Bipolar op amps can easily be designed with PNPs on the input and therefore single supply performance can be easily achieved from bipolar technologies. CMOS devices make good single supply op amps because they use PMOS transistors on the input stage, but Bifets have a problem! 'N-Channel' JFETs exhibit very poor stability and high leakage with high drain-gate voltages, and today are rarely used in the input stage of an op amp. Bifets then, use 'P-Channel' JFETs on the input and are therefore not developed for single supply applications.

Bifets and bipolar op amps with NPN input stages do however have their benefits. They now have a Common Mode input range that can include, (and in the case of the TLE2061 family actually exceeds) the positive rail. This is useful in various 'High-Side Monitoring applications' such as power supply circuits. NPNs also have the advantage of enabling op amps with lower noise and increased gain and precision.

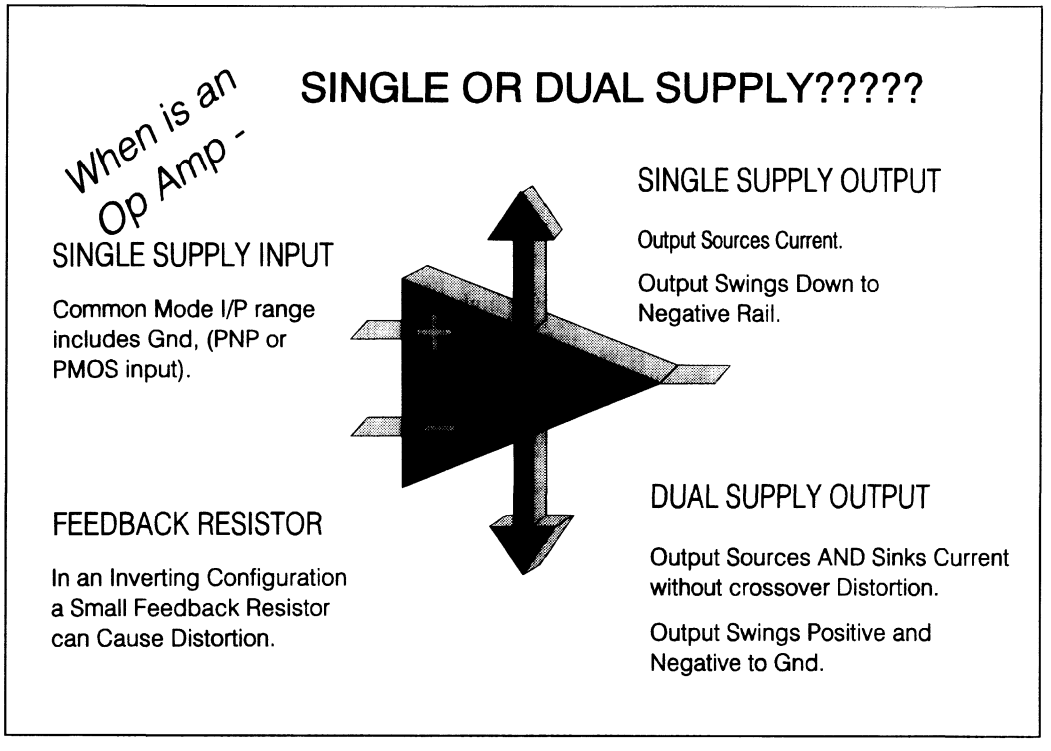


Figure 1.21 When is an Op Amp Single or Dual Supply?

Output Stage Design

The second requirement for a single supply op amp is that the output must swing very close to the negative rail. In the case of CMOS designs this is easily achieved by using NMOS transistors on the output - developing an output that swings to within a few microvolts of the ground is relatively simple. In this type of circuit the output has been designed to predominantly source current.

Bifet and bipolar op amps can effectively use the same type of bipolar output stage but developing an output that swings down to the negative rail using these technologies is not so simple. In op amps such as the LM324, the output has been designed specifically to source current, and for use in single supply applications. The typical requirement, however, for the majority of amplifiers designed using bipolar or Bifet technologies is that they are able to both **Sink and Source current** - i.e. they are capable of driving a load that is connected to the mid point of their supplies without crossover distortion. This feature, when combined with the capability of the output to swing all the way to the negative rail makes the design of an output stage very complicated. Clever design techniques are therefore needed to realise true single supply bipolar op amps. Devices such as the TLE2141 and LT1013 are examples of products that perform well in both situations - they have an output that swings to the negative rail but they can also sink and source current.

Other newer bipolar op amps are also often termed single supply amplifiers - their common mode input range includes ground and their output swings very close to, if not all the way to the negative rail. An example is the TLE2021 family, these designs are ideally suited to many single supply applications and are very different to products which have been optimised for dual supply applications only.

Newer CMOS designs are also being developed for use with both single and dual supply rails. Op amps such as the TLC2201, TLC2652 and TLC2654 are excellent with a single supply, and their output will swing all the way down to the negative rail. With dual supplies their output will happily sink and source current, and will swing to within a few hundred millivolts of each rail without causing distortion.

Figure 22 shows what errors can occur if an op amp, designed for single supply circuits, is used in a dual supply configuration.

4.12. Single Supply Considerations

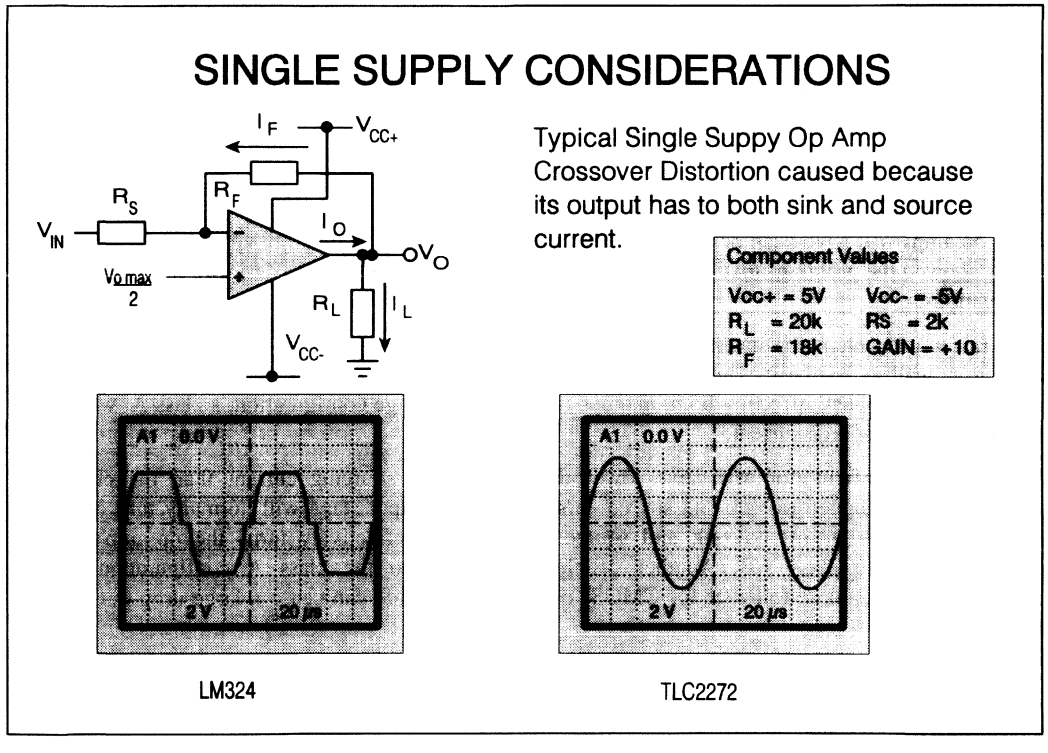


Figure 1.22 Single Supply Considerations

Figure 21 effectively put single supply op amps into two categories;

1) Those whose output can source current only

2) Those that can both sink and source current and have been designed to drive a load which is connected to the mid point of the supplies.

If a single supply op amp, such as the LM324, is used in an application where it needs to both sink and source current then the output signal may be heavily distorted. The device has not been designed to make the cross-over from sinking to sourcing current smoothly, and therefore distortion is very apparent - see photo on left. This problem is also made worse because the load being driven in this application is not easily handled by this device. If the load resistor is increased then the amount of distortion will reduce. Remember that the feedback resistor is seen as a load and that to reduce distortion it should be kept large.

The waveform on the right shows the TLC2201(a high performance CMOS op amp), used in the same circuit as the LM324. This device outperforms the LM324 in several ways;

1. The device is designed to sink and source current and also has the ability to work like other CMOS parts in single supply applications
2. The TLC2201 can drive heavier loads than the LM324 - the equivalent load here is 10 kΩ and the LM324 is beginning to suffer.
3. The TLC2201 has a much wider output swing. With +/-5 V supplies the output will swing to +/- 4.7 V - true single supply operation.

4.13. TLC2272 Rail to Rail Op Amp

Most op amps will have been designed to work in either single rail or dual rail applications. The figure above showed the problems that can be seen when using an op amp that was designed for single supply applications.

This raises a problem for inverting amplifier configurations where the op amp might have to sink current as well as source it. This is what affected the LM324 and can affect the TLC27X family of op amps. The problem affecting both op amps is their output stage configuration, a class A, which are designed only to source current.

The class A configuration will give lower distortion when sourcing current than the class AB configuration, designed to sink and source current, but the output stage will normally turn off for a short period when trying to sink and source current. This effectively turns the op amp's output configuration into class AB. Another problem attributed to the class A configuration is the emitter-follower (source-follower for CMOS) output stage, which can cause a large drop-out voltage from the supply.

This can be seen in the TLC27X family by their typical output swing of 0 V to V_{DD}-1 V. The new generation of general purpose LinCMOS op amps, TLC2272, have overcome these problems by using a push-pull output stage.

The push-pull output stage enables the TLC2272 to swing within millivolts of both rails while sinking and sourcing current. This capability enables the device to work in both single supply applications (operating in class A) and dual supply applications (operating in class AB). This is very important when providing signal conditioning for A-D converters, normal single supply op amps have their outputs clipped 1 V from the positive supply, which reduces the dynamic range of the A-D converter by 20%.

TLC2272 DUAL RAIL-RAIL CMOS OP AMP

SPECIFIED FOR SINGLE AND DUAL SUPPLY OPERATION!

- Output Swing Includes Both Supply Rails
- Common Mode Input Voltage Range Includes Negative Rail
- Low Input Offset Errors
  ...VIO = 950 μV @ 25°C
  ...IIB = 1 pA @ 25°C
- LOW NOISE
  ...Vn = 9 nV/√Hz @ 25°C
  ...In = 2.8 fA/√Hz @ 25°C

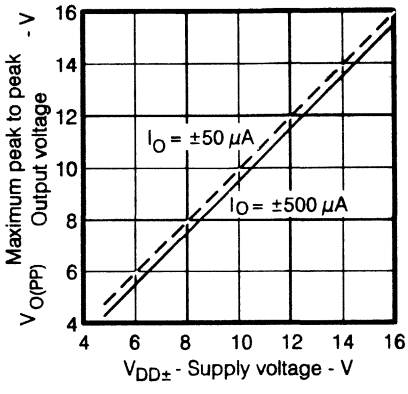


Figure 1.23 TLC2272 Rail to Rail Op Amp

The wide output swing and low input offset errors, V_{IO} < 1 mV and I_{IB} = 1 pA (Typ), make it suitable for high impedance transducer interfacing. Its capability for use in these applications is enhanced by its low noise specifications.

All these features make it one huge advance over other general purpose CMOS amplifiers.

4.14. TLC2272 Single Supply Sensor Interface

The increase in use of electronics in the automotive industry has brought about the need for single supply op amps, capable of operating from a +5V supply. The TLC2272 was designed for these applications, using a PMOS input stage gives the common-mode range down ground, while a push-pull CMOS output stage gives it an output swing includes both rails.

This application below utilises all these features, interfacing to a piezoelectric pressure sensor used to sense knocking in an internal combustion engine. The first op amp is in a non-inverting configuration, making use of its high input impedance and its common-mode range down to the negative rail.

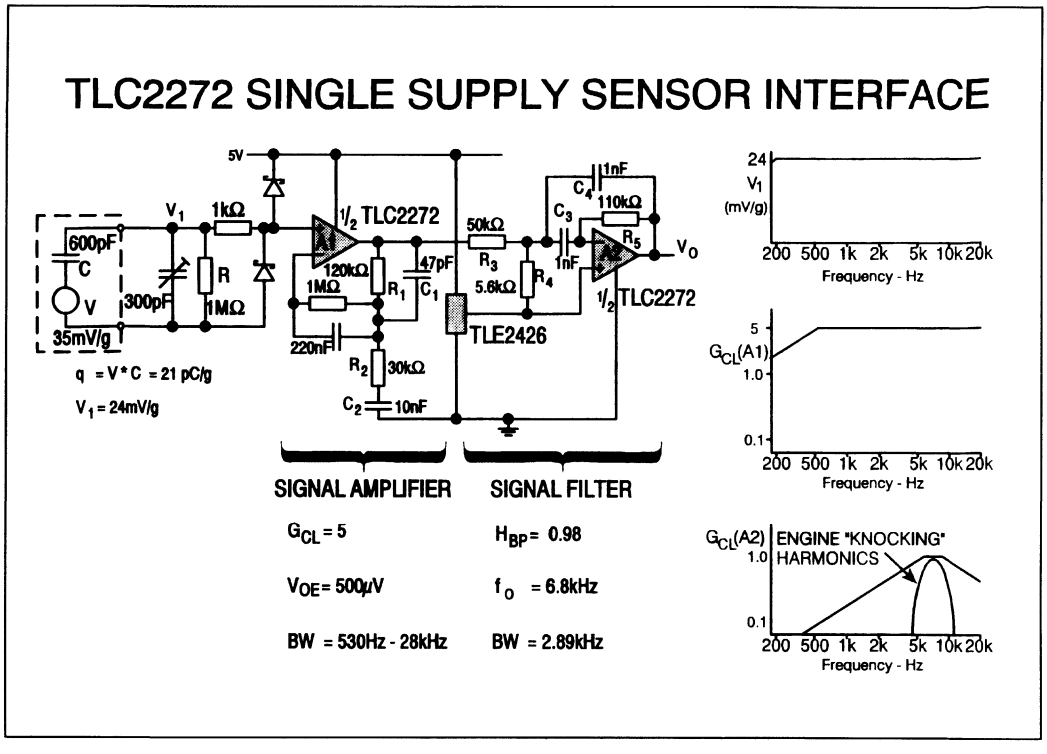


Figure 1.24 TLC2272 Single Supply Sensor Interface

The piezoelectric sensor is an ac sensor and can be modelled by a voltage source in series with a capacitor. The sensor can be considered as working in two modes one as a sensors which produces charge or as a sensor which produces ac voltages. In this application the TLC2272 is amplifying the voltage produced by the sensor.

Interfacing to the sensor is a 1 MΩ resistor and a calibrating capacitor, this capacitor can be used to alter the high pass cut-off frequency of the sensor as well as affecting its gain. The shunt resistor is included to provide both a current path for any bias currents of the op amp and to provide a current path for any current flowing out of the sensor. In order not to load the sensor this shunt resistor needs to have a large resistance, and for this reason the TLC27M7 is ideal. No bipolar op amp has a high enough input impedance and more importantly low enough bias currents to be able to interface with these resistances.

The first op-amp, acting as the sensor interface, doubles as a wideband filter amplifying the input signal plus filtering out signals which are not of interest. The second op amp in the TLC2272 is connected in a Delyiannis-Friend configuration producing a bandpass filter, which is used to filter out all other signals.

The advantages of this circuit is that all the filter's key parameters can be designed and decided sequentially, simplifying the design process. The input resistors act as attenuators bringing the gain of

this filter to unity. The centre frequency of the circuit is determined by the feedback resistor, R_5 , and the Thevenin equivalent of the input attenuating resistors, R_{TH}.

$$\omega_o = \frac{1}{C * \sqrt{R_5 R_{TH}}}$$

and

$$R_{TH} = \frac{R_3 * R_4}{R_3 + R_4}$$

The quality factor, Q, (a measure the reactance to resistance ratio at the natural frequency of the filter, roughly speaking it is a measure of how steep the initial roll-off is) of the filter depends solely on the ratio of the feedback resistor to the Thevenin equivalent of the input resistors.

$$Q = \frac{1}{2}\sqrt{\frac{R_5}{R_{TH}}}$$

When engine knock starts to occur the sensor will generate a range of signals, whose frequency is not present when the engine is running properly, which the second op amp is used to exclusively amplify. The characteristic knock frequency of the engine will change depending on the size of the cylinders and the cylinder block's material. To meet all these changes in frequency a wideband sensor and a versatile op amp are required; most of these sensors have bandwidths into the tens of kilohertz, meaning that one form of sensor should suit almost all applications. The TLC2272 with a unity gain bandwidth of 2 MHz and an input offset voltage of 950 µV provides the accuracy and speed required by the system, without using capacitive coupling.

The rail-rail output swing also increases the system's dynamic range by enabling the TLC2272 drive A-D converters to their full input range. This is helped by the TLE2426 virtual ground, which enables the TLC2272 to drive symmetrical loads. This example typifies a usual LinCMOS™ op amp application requiring low bias currents and low quiescent currents whilst providing accurate signal conditioning.

4.15. TLC2652 Chopper Stabilised op Amp

Chopper stabilised operational amplifiers have been available for many years but when they were first released there was much resistance, by design engineers, to using them. It was felt they were too noisy as an op amp and also generated too much extra noise within a circuit. Recently however, engineers have started to appreciate the outstanding levels of performance that can be achieved by using a 'chopper'. It was realised that the so called noise problems were not such a real issue and that the performance and relative low cost of newer products was just too good to miss!

The ideal precision op amp would require; ultra low offset voltages with negligible drift, bias and offset currents as low as those achieved by FET input amplifiers plus open loop gains, PSRR and CMRR would be high and noise would have to be at a minimum. Chopper stabilised op amps *very nearly* achieve the required level of performance to be the ideal precision amplifiers! If bandwidth is limited to reduce noise errors, then the precision of a circuit is determined more by external components and parameters (board layout, temperature gradients etc.) than the op amp itself.

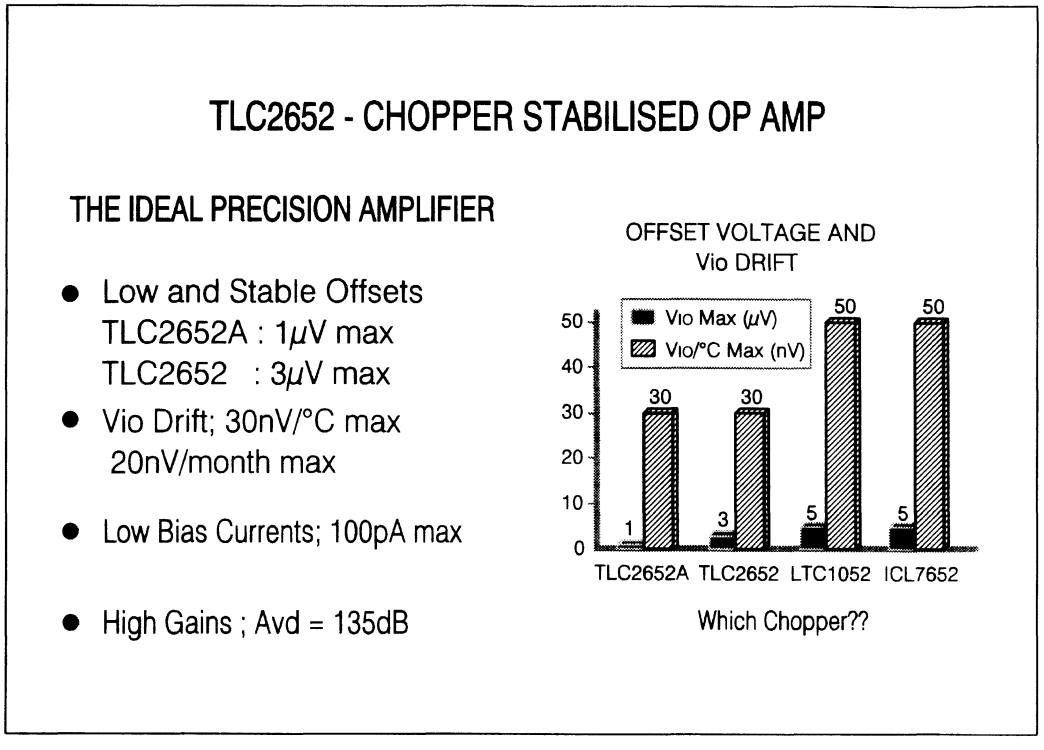


Figure 1.25 TLC2652 Chopper Stabilised op Amp

Newer designs in particular are getting closer still to the ideal. The latest choppers released by Texas Instruments are the **TLC2652/A and TLC2654/A** - both are **world leaders.**

The **TLC2652**, shown above, is a chopper stabilised op amp optimised for precision. The 'A' selection part has a **maximum offset voltage of just 1 μV** and maximum drift specifications of **30 nV/°C and 20 nV/month**. Short and long term errors due to offset voltage are rarely a problem! The device is also CMOS so its bias currents are low causing minimal errors due to currents flowing in external resistors. A further benefit of chopper design techniques (see Figure 26) , is that they also benefit from extremely high gains, Avd is 135 dB, and both the Power Supply and Common Mode Rejection Ratios are 120 dB. The device easily meets the requirements of an 18 bit system.

If there is a limitation to choppers then it occurs in three areas: Noise voltage is typically high (although 1/f noise is practically removed) in most designs (see TLC2654, Figure 26, for something new!) and so care must be taken to limit the circuits bandwidth of operation. It should be noted however that with very low bandwidths, <0.25 Hz, the noise from a chopper is often less than the noise of a bipolar op amp (this is because of their almost zero 1/f frequency). Secondly, because the devices are fabricated using CMOS technology then supply voltages are most commonly limited to +/- 8V. Thirdly, they are often just too good! Errors are typically introduced due to external factors (see 4.19), and these must be carefully considered when depending upon the precision available from these parts.

If you are looking for a device that achieves outstanding levels of precision the TLC2652A should be seriously considered.

4.16. TLC2654 - Lowest Noise Chopper Op Amp

One large drawback of chopper stabilised op amp has been their relatively high input noise voltage - at low frequencies the noise voltage of a typical chopper may be 100 nV/$\sqrt{Hz}$, significantly higher than most amplifiers. In practice this means that the circuit bandwidth needs to be limited to ensure that dc errors are dominated by the offset voltage of the amplifier and not by the low frequency noise of the op amp. When using the TLC2652A with an offset voltage of 1 µV the circuit bandwidth needs to be limited to 1 Hz.

TLC2654 - LOW NOISE CHOPPER OP AMP

By Increasing the Chopping Frequency to 10kHz, Noise for the TLC2654 has been Significantly Reduced. Resulting in:

Increased Usable Bandwidth

Reduced Intermodulation Effects

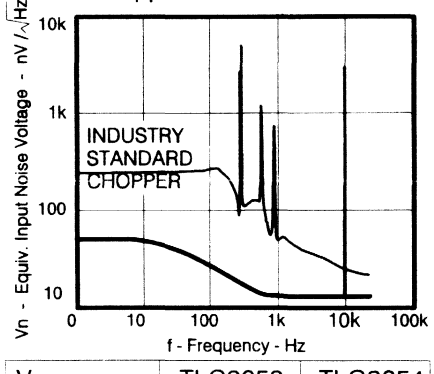
Precision Maintained:

Vio..... TLC2654A = 10µV max
TLC2654 = 20µV max

Vio Drift... 0.3µV/°C max
0.02µV/month max

(Still 4 years for 1µV of Vio Drift!!)

Chopper Noise Performance



Vnpp	TLC2652	TLC2654
DC to 1Hz	0.8 µV	0.5 µV
DC to 10Hz	2.8 µV	1.5 µV

Figure 1.26 TLC2654 - Lowest Noise Chopper Op Amp

This places severe ac limitations on the circuit, the 10-90% rise time of any single pole filter is $0.35/f_{3dB}$, where f_{3dB} is the 3dB bandwidth of the filter. Limiting the bandwidth of the TLC2652A places 10-90% rise time of 3.5s onto the system, settling to 10 bits of accuracy can take considerably longer. In some high precision systems this may not be a problem but it others in can place too large a time limit on data accessing and gathering.

Realising that this can cause problems in a lot of applications Texas Instruments has put significant effort into developing a chopper with much lower noise - the TLC2654 was the result. By increasing

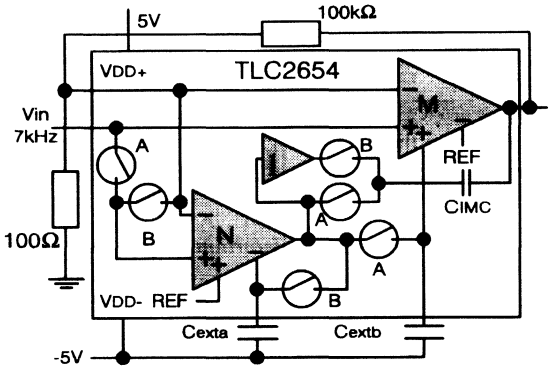
the chopping frequency from 450 Hz (for TLC2652 and other standard choppers) to 10 kHz it was possible to reduce the total noise of the amplifier by a half. This has been tried in the past but has always proved unsuccessful due to the resulting large increase in offset voltage and drift. Patented techniques used in the TLC2654 however enabled offsets voltage shifts to stay at a minimum, while improving the noise specifications - 10 µV is the maximum for the TLC2654A. Drift is also low at 0.05 µV/°C and 0.06 µV/month. It is not surprising that the TLC2654 won the "Product of the Year" Award from the US magazine Electronics.

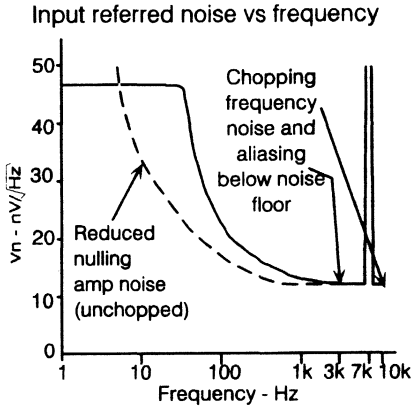
In practice, choppers are often used as much for their low drift as for their absolute offset. By using the TLC2654 precision can be maintained and the usable bandwidth of the device can be increased. In practice this means that precision measurement applications, like weigh scales, can be designed with much improved response times.

4.17. High Performance Low Noise Choppers

Chopper op amps such as the **TLC2652** and **TLC2654** offer the very highest precision in terms of offset voltages and drifts. In addition to this they also offer very low noise spectral densities at frequencies below 1 Hz.

The low offset voltage and drift is attained by continually measuring the offset of the main and nulling amplifier and using this to cancel out the offset voltages. This is done by a form of sampling, which can add noise to the system in a number of ways, and it this noise has limited the acceptance to choppers. This figure discusses the relative effects of the noise introduced by chopper op amps, and how they may be able to improve system performance.





- Choppers offer the Ultimate in Precision in Low Frequency Applications
- Chopping and aliasing errors are Reduced to be below Noise Floor
- T.I.'s Choppers offer better Noise and Offset Accuracy

High Performance Low Noise Choppers

4.17.1. Flicker Noise reduction

A chopper op amp sees its offset voltage and input noise voltage as very similar errors, which enables it to remove both the offset voltage and the low frequency noise voltage. At very low frequencies the noise voltage is dominated by flicker noise (having a 1/f characteristic), and it is this noise that the chopper sees as an offset, and is able to remove producing a flat spectrum. It should be noted, however, that the level of the noise at 50 Hz has an amplitude higher than low noise op amps, but because of the removal of flicker noise at frequencies below 1Hz the noise level is in fact below most of the lowest noise op amps.

At very low frequencies, combination of the very small low frequency noise and the very low offset couple together to produce the highest accuracy solutions to high precision DC. applications.

By continually nulling out the offset voltage of the op amp, noise produced from internal references are rectified and averaged out to produce a systematic offset which the chopper cannot null out. Texas Instruments' choppers use a special technique where the references' noise are not rectified and this reduces not only the systematic offset but also the wideband noise, shown on the figure. This reduced wideband noise enables Texas Instruments' choppers to reach noise levels that were previously unattainable by integrated circuit choppers. Another advantage of the techniques used within Texas Instruments' choppers is that because the systematic offset voltage has been reduced, they are able to

chop at much higher frequencies, giving much lower noise voltages. Choppers in the past were limited to chopping frequencies below 500 Hz. The figure above shows the performance of the TLC2654, chopping at 10 kHz, creates noise levels below 50 nV/$\sqrt{Hz}$, whereas chopping at 450 Hz would generate noise levels well above 100 nV/$\sqrt{Hz}$

4.17.2. Sampling and discrete time effects

As stated earlier, choppers are in effect sampling devices and this results in their spectra containing harmonics of the chopping frequency. The amplitude of these harmonics are normally in the nanovolt region, as shown in the spectrum analysis, and so normally the energy contained in them can be neglected.

Another cause of concern related to choppers is ***inter-modulation distortion***. During the chopping procedure the device is sampling and this can cause folding back of high frequency signals down to lower frequency signals. This is normally known as aliasing and can add errors into the frequency range of interest, thus reducing the dynamic range of the op amp. With the TLC2652 and TLC2654 any aliased signals will normally be attenuated to the order of the noise floor. This effect is also shown on the spectrum analyser plot. This is just one form of inter-modulation distortion and as all active devices are non-linear some inter-modulation distortion will be created. At best this distortion will be harmonics of the input signals, but poor performance devices can cause summation and subtraction of these harmonics. The latter effect is much more important in high end audio systems.

The chopper induced intermodulation distortion effects are removed by a special `intermodulation compensation network'. All choppers employ a form of "intermodulation compensation network", and its basic function is to reduce the ac. gain of the nulling amplifier during the amplifying phase. Without this network aliasing between the input signal and the chopping frequency would occur.

During the amplifying phase an intermodulation compensation capacitor, C_{IMC}, is connected from the output of the nulling amplifier to the output of the main amplifier, so reducing the gain of the path through the nulling amplifier. During the nulling phase C_{IMC} is removed from the nulling amplifier's output and connected to another voltage source. This isolates the nulling amplifier from the main amplifier's output. When C_{IMC} is switched back, the change in voltage across it introduces charge and creates transients onto the main amplifier's input. C_{extb} integrates this injected charge, increasing the offset of the whole op amp. As the chopping frequency increases, minimising aliasing, more charge is injected increasing the offset created.

To reduce this problem, Texas Instruments has implemented a technique which minimises the voltage change across C_{IMC}. Driving C_{IMC}, during the nulling phase, with a buffered signal from the nulling amplifier reduces the change in voltage. This minimises any change in charge across C_{IMC} when it is switched back. Hence Texas Instruments' choppers have lower offset voltages and are capable of chopping at higher frequencies which produces less low frequency noise and also gives the added benefit of being able to operate with a wider range of input signal frequencies.

The curve shown above not only demonstrates the very low noise voltage characteristics but also demonstrates the effectiveness of the intermodulation compensation network. The aliased signal developed from a 7 kHz sine wave is below the noise floor (at 3 kHz equal to 12 nV/$\sqrt{Hz}$) of the chopper. The curve also shows the very large rejection of the chopping frequency; at 10 kHz the spectral content is less than the noise floor of 12 nV/$\sqrt{Hz}$, which is again below the noise level of most choppers.

It is these characteristics that allow the choppers to be used in yet more applications where they were once considered to be too noisy.

4.18. Low Noise Thermocouple Amplifier

A thermocouple is a temperature sensor made from two dissimilar metals. When the junction is heated, a small thermo-electric voltage is produced which increases with temperature.

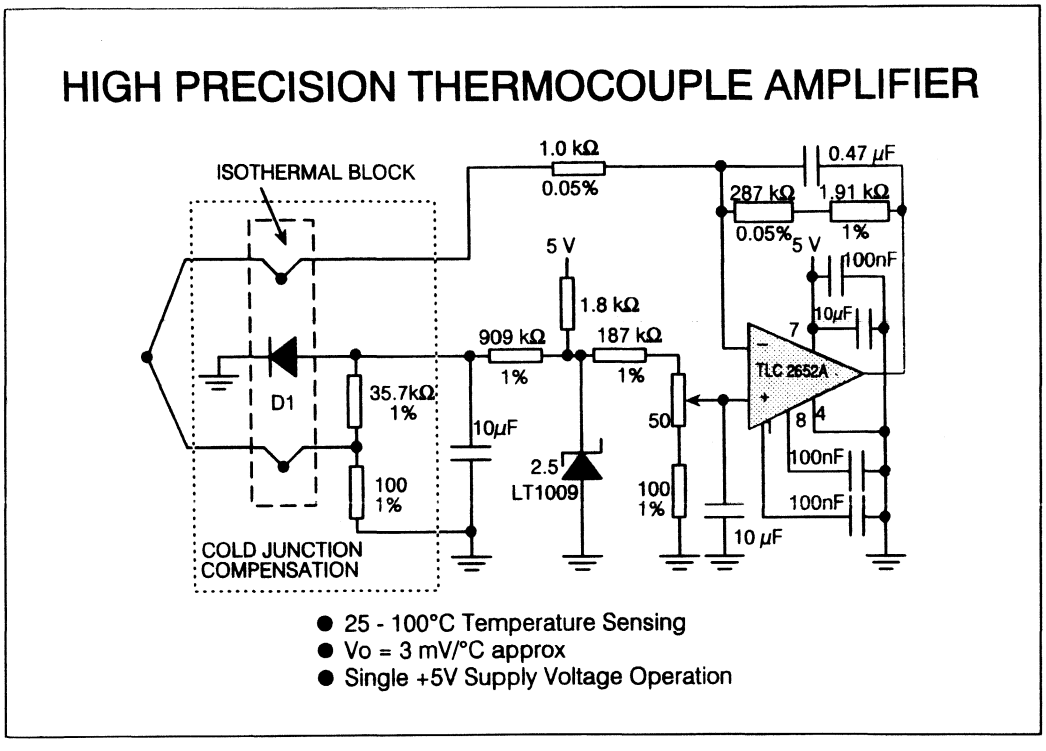


Figure 1.27 Low Noise Thermocouple Amplifier

Thermocouples are very small signal devices. For an S-type thermocouple, the average output voltage variation over its 0-1500°C temperature range is only 10.38 µV/°C. Although linearity is poor, the temperature and voltage relationships are predictable and repeatable, so digital techniques can be used for linearisation downstream.

Two thermocouples are always present, a measurement junction and a reference junction. It can be proved that the temperature drift of the reference and measurement junctions are equal. It is therefore only necessary to compensate for the drift with ambient temperature of the reference thermocouple - this technique is called "cold junction compensation". In this example the approximate 2 mV/°C change of a low cost diodes base emitter voltage is resistively divided down to the thermocouple's sensitivity (6 µV/°C) at 25°C ambient temperature. This counteracts any change in the reference junction temperature.

The circuit produces an output of 4.5 V for full scale. As the circuit is operating from a single 5 V supply, the op amp cannot swing quite to 0 V, thus limiting the lower end of the measuring range to 25°C. Ideally the 0°C would produce an output voltage of 0 V. The need for very highly accurate resistors can be avoided by using an additional gain setting trimmer

Signal conditioning at such low levels is not trivial. Careful choice of components, PCB layout, grounding and consideration of thermoelectric effects at all junctions are of the utmost importance. Mistakes in overlooking these could lead to external errors swamping any introduced by the op amp. When dealing with such small signals low frequency can be a real problem. The reference as well as the op amp should be filtered.

Due to the very small signals involved a very high performance op amp offering high open loop gain, low offset and low drift is required. These careabouts, at low frequencies, are best met by chopper stabilised op amps, the best choice being the TLC2652A.

To take advantage of the extremely low offset voltage drift of the TLC2652A - 30 nV/°C (maximum) care must be taken to compensate for the thermo-electrical effects present when two dissimilar metals are brought into contact with one another. This includes device leads being soldered to a printed circuit board. Dissimilar metal junctions can produce thermo-electrical voltages in the range of several μV/°C, which is several orders of magnitude greater than the chopper's offset drift. Air circulation can also be another cause of output voltage drift, as can thermal gradients appearing across the PCB and metal junctions

4.19. Chopper Design Careabouts

When an application requires the absolute best performance from the chopper stabilised op amp, a number of factors and design considerations should be considered.

Noise

Noise has been discussed in detail in figure 29, but the key points to remember are;

Limit Bandwidth:

The bandwidth of the op amp should be limited to reduce DC errors associated with the relatively high noise voltage of the amplifier. Take advantage of the device's low 1/f frequency however, as over very small frequencies (<1Hz), the choppers noise are less than many bipolar op amps!

Intermodulation effects:

If an input signal has a frequency component equal to greater than half the chopping frequency then intermodulation errors may be caused. In practice, chopper design techniques have minimised these errors (<70 dB down on input signal) but it may be necessary, depending upon the frequency and magnitude of input signal, to filter out these components using an extra filter stage before the chopper.

Chopping Frequency:

The standard selection chopper op amps are available in an 8 pin package and have a predetermined internal clock frequency which defines the noise performance and offset voltage of the op amps. There are however, options available in a 14 pin package which have the capability of changing the clock frequency by the use of an external clock. This external clock signal can be fed directly into the CLK IN input and the INT/EXT pin is attached to V_{DD-}. When operated in a single supply configuration the

device can be driven directly by TTL or CMOS logic without the need for extra level shifting. Although not critical, the duty cycle of the external clock should be kept between 30% and 60%.

NOISE

Limit Bandwidth... <1Hz

Intermodulation.... Vin < Fch/2

Variable Chopping Frequency

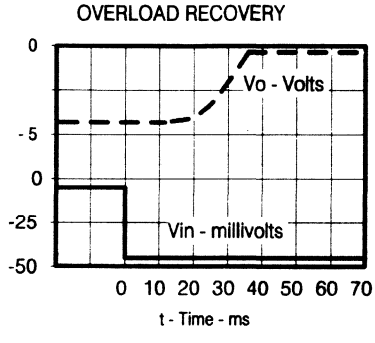
External Components

External Capacitors
- Low Leakage and Low Dielectric Absorption
- 0.1 μF or 1μF to Vdd- or CR

Overload Recovery
- CLAMP typically not required

Thermoelectric Effects

ESD and Latcup Protecction Circuits included



Chopper Design Careabouts

The advantages of being able to modify the clock frequency of these choppers are essentially two fold. Firstly the noise and offset of the op amp can be optimised for your particular circuit and secondly the clock frequency can be matched to other clock signals present within your circuit.

4.19.1. External Components

Choosing and using the Right Capacitors:

The external capacitors, C_{XA} and C_{XB}, should be carefully chosen to ensure best operation of the amplifier. Specifically, special attention should be given to the leakage and dielectric absorption of these components.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and stand-offs are recommended for operation at T_A = 125°C. In addition, guard bands are recommended around the capacitor connections on both sides of the printed board to alleviate problems caused by surface leakage on circuit boards. Very thorough cleaning of the circuit board using alcohol or similar cleaning fluids is also recommended and errors can be further reduced

by guarding the inputs of the amplifier with a ring connected to a low impedance node, normally ground.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset is needed, it is recommended that high quality film capacitors, such as mylar, polystyrene. or polypropylene, be used. in other applications, however, a ceramic or other low-grade capacitor may suffice.

The TLC2652 and TLC2654 have been designed to function with values of C_{XA} and C_{XB} in the range of 0.1µF to 1µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as closely as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that in many choppers, connecting these capacitors to the V_{DD-} pin will degrade the noise performance. This problem has been eliminated with these designs.

Overload Recovery Time/Output Clamp:

When large differential input voltage conditions are applied to the TLC2652 and TLC2654 choppers, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time. Typical recovery times are significantly faster for the TLC2652 and TLC2654 when compared to competitive products; however, if required, this time can be reduced further by using internal circuitry accessible through the clamp pin.

This Clamp circuit stops the output circuit from going into saturation due to a reduction in the closed-loop gain of the device (activated when the output is with 1V of each rail). The CLAMP pin is simply connected to the inverting input of the op amp, and it may however cause a slight degradation in the maximum output swing.

Thermoelectric effects:

To take advantage of the extremely low offset voltage drift of any chopper op amp, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius, which are orders of magnitude greater than the 0.003 µV/°C typical drift of the TLC2652).

To help minimise thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of non soldered connections (such as sockets, relays, switches etc.) in the input signal path. Cancel thermoelectric affects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire wound resistors, is also beneficial. It is also recommended to try and minimise excessive power dissipation and temperature gradients across a circuit board. Large power dissipating devices should be kept well away from precision components and air movement should ideally be kept at a minimum.

Electrostatic Discharge and Latchup avoidance:

Both these topics are discussed in detail in figure 14, but points to note are;

ESD - Care must be taken when using these devices, but both the TLC2652 and TLC2654 have been designed to withstand ESD voltages up to 2000V without causing functional damage.

Latchup - Both products have been designed to withstand 100 mA surge currents without sustaining latchup.

5. Bipolar Operational Amplifiers

5.1. Bipolar Operational Amplifiers

Bipolar is still by far the most popular technology used to develop operational amplifiers, and new, higher performance bipolar technologies are being developed continuously - the μA741 would not recognise the technologies being used today!

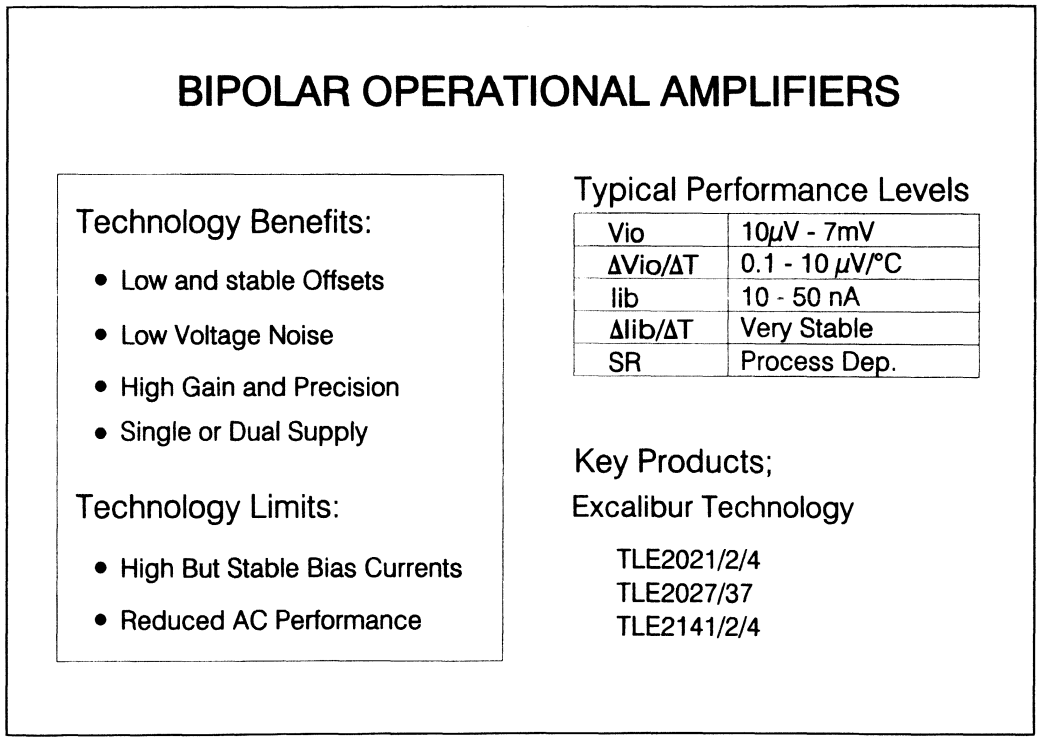


Figure 1.28 Bipolar Operational Amplifiers

Devices designed using bipolar technology have a number of benefits over Bifet or CMOS products.

5.1.1. Bipolar Advantages

Low and stable offsets;

Because bipolar transistors are relatively easy to match and their behaviour due to temperature and current change is well understood, it is possible to develop operational amplifiers with low and stable offsets. Offset voltage errors are due to V_{be} mismatches in the input transistors and the different currents flowing through the collectors of the input stage transistors. By using various trimming techniques, bipolar designs are now available with offset voltages as low as 10 µV which drift less than 0.1 µV/°C.

Low Noise;

A low noise voltage rather than low noise current specification is of most importance in the majority of applications (e.g. audio, telecom and many instrumentation systems). Bipolar op amps offer the lowest noise voltage performance among commercially available devices. The noise voltage from the input of a bipolar amplifier is dominated by the thermal noise from the base spread resistance and the emitter small signal resistance. Both of these, and other factors, can be optimised to achieve op amps with <2 $nV/\sqrt{Hz}$ noise voltage specification, this performance is impossible to achieve using a FET input amplifier. When interfacing to high impedance sources however, bipolar op amps become inferior to CMOS designs. Their high noise current specifications dominate noise errors.

High Gain;

The transconductance, gm, of the bipolar input stage is high and therefore the related open loop gain of the amplifier is also high. The benefit is the ability to design circuits which are much more 'accurate' than Bifet or CMOS designs. This high gain however does mean that an complicated compensation networks need to be used to ensure stability, a factor which lower gain JFETs have benefited from to achieve higher slew rates.

5.1.2. Bipolar Disadvantages

High Offset and Bias Currents;

Because of the bipolar input stage the bias currents of bipolar op amps is high (effectively it is the base current flowing into the input transistors). Various design techniques such as SuperBeta NPNs, or bias current cancellation circuits can be used to reduced these currents but it would be very unusual that, at room temperature, a bipolar device could compete with a FET design.

Bias currents for bipolar designs are however much more stable than for FET input designs. At high temperatures it is possible for a FET input device to actually have higher bias currents than a good bipolar design, particularly a super beta part.

Slow Lateral PNPs;

Lateral PNPs are much slower (and noisier) than the NPNs available from the same process. A typical technology would have PNPs with an f_T (transistor bandwidth) of 3 MHz, compared to NPNs which have an f_T of 150 MHz. As it is very difficult to design a device without using PNPs, the overall AC performance of an amplifier is severely limited.

Realising this many manufacturers have developed 'Complementary Bipolar Technologies' which have much faster PNPs who's f_Ts are similar to the NPNs. The result has been much faster bipolar op amps.

Excalibur is Texas Instruments' new complementary bipolar process, but as well as having faster PNPs it includes a number of other features necessary for the development of performance amplifiers. This technology is discussed in detail in the next Figure.

5.1.3. Texas Instruments' Common Bipolar Op Amps

TLE2021	LM301	LT1007	OP37
TLE2022	LM307	LT1013	RC4136
TLE2024	LM308	LT1014	RC4558
TLE2027	LM324	LT1037	RC4559
TLE2037	LM348	NE5532	uA741
TLE2141	LM358	NE5534	uA747
TLE2142	LM2902	OP07	uA748
TLE2144	LM2904	OP27	

5.2. Excalibur Technology!

Texas Instruments has recently started releasing products designed using its new Excalibur technology - today 4 whole families are available with significantly more are under development. Everyone of these designs benefits from the significant features and process enhancements made available by Excalibur - a Complementary bipolar/Bifet technology optimised for the design of cost effective operational amplifiers.

Before developing Excalibur, Texas Instruments analysed the latest system requirements for new operational amplifiers and the technology limitations which have restricted the desired levels of performance being achieved. Not surprisingly, the diverse range of applications meant a number of different process enhancements were identified, the ideal technology would therefore need to provide a range of improvements.

Texas Instruments decided that the ideal solution would be to produce a technology which featured a number of different building blocks - developing a Complementary Process alone was not enough. A further, and important, benefit of a process that offers a wide range of different structures is that very different amplifiers can be developed by using only slightly different mask levels. Increased volumes would therefore enable more cost effective products!

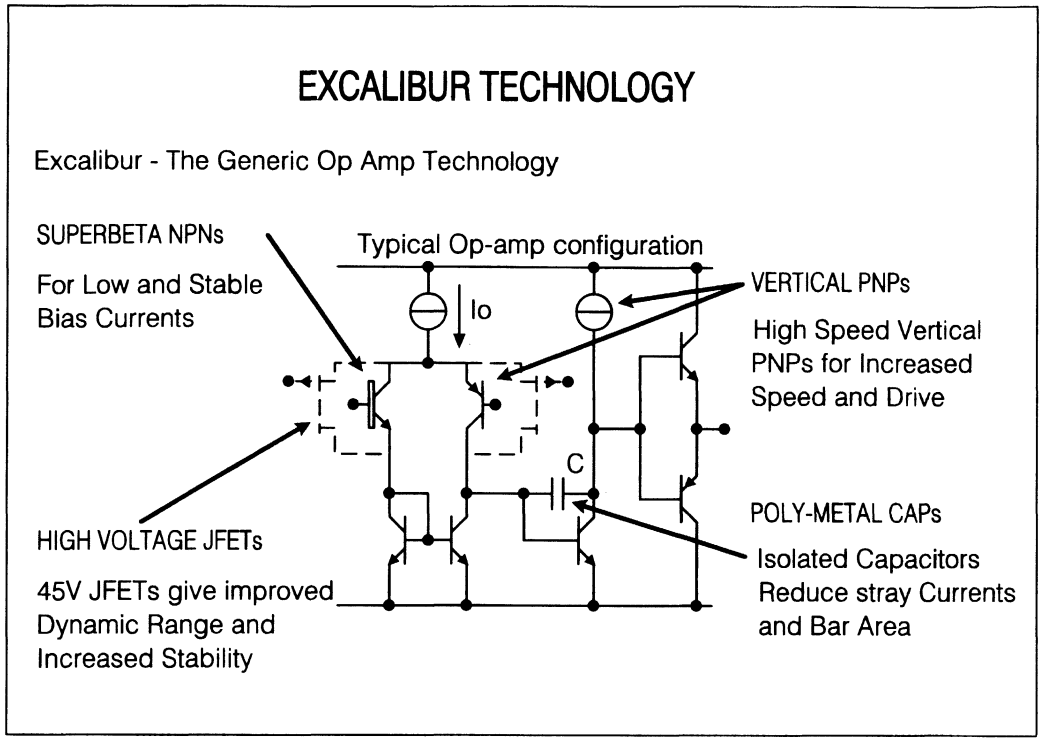


Figure 1.29 Excalibur Technology!

The main areas of development and improvement are discussed below:

5.2.1. High Speed Vertical PNPs

It is difficult to develop an operational amplifier without employing PNP transistors (they are most commonly used in an amplifiers differential input stage or as current mirrors) and as a typical lateral PNP is 50 times slower than their equivalent NPNs, they have proved a severe limitation to the speed of an op amp.

Many companies have recognised this and have developed Complementary Bipolar technologies to improve the speed of PNPs and therefore the extend the AC performance of their op amps. By concentrating on improving the speed of both the NPNs and a new vertical PNP structure, Excalibur is significantly faster than previous processes. The NPN now has an FT(transistor bandwidth) of 450 MHz, 3 times faster, and the PNP has an FT of 150 MHz (50 times faster!). The result is that new op amps can be developed with much improved AC performance without any increase in supply current.

5.2.2. SuperBeta NPNs

A limitation of precision bipolar op amps is their relatively high bias currents and noise current specifications. A recognised technique of reducing these parameters is to use superbeta NPNs in the

input stage of the amplifier. Excalibur's superbeta NPNs have an h_{fe} (transistor current gain) of 2000, 10 times higher than the standard structure. This enables a significant reduction in bias currents which because of bipolar's inherent current stability may at higher temperatures be lower than a FET input device.

5.2.3. JFET Transistors

Bifets will continue to be extremely popular op amp types and it was felt essential that Excalibur had the capability to produce performance Bifet amplifiers. A slight limitation to the JFETs used in today's op amps are their restricted supply voltage operating range. Most designs operate with maximum +/- 18 V supplies and therefore operation from higher supply voltages, such as the common +/-22 V, is not possible. Excalibur JFETs were developed with breakdown voltages of 50 V, enabling higher voltage Bifets to be processed. Applications now benefit from increased supply voltages and an improved common mode voltage range.

The offset voltage of Bifet op amps was also not forgotten. The lessons learnt from the development of the Enhanced TL05X and TL03X Bifet families have been introduced into Excalibur's structures. Offset voltages as low as 500 µV, with high stability, are available from op amps supplied in a plastic package.

The TLE2061/2/4 family and the TLE2082, discussed in the Bifet section, were developed using Excalibur.

5.2.4. Isolated Capacitors

All compensated operational amplifiers use a minimum of one capacitor within a design. In many cases this capacitor takes up significant silicon area, and causes noise and switching problems by injecting spurious current into the substrate.

The capacitors used in Excalibur are made from a Polysilicon - Nitride - Metal layer and is isolated via Field Oxide, from the rest of the circuit. The result is a 4 times improvement in capacitance per unit area and a structure which does not disrupt other parts of the circuit. Improvements in both performance and cost are achieved.

The result

Not all these structures are used in every new design but having them all available as building blocks in the same process gives the IC designer a great deal of flexibility and choice in his circuit design. The end user benefits from performance amplifiers which, because they are made from a widely used process are truly cost competitive.

5.3. TLE202X Low Power Precision Op Amps

The TLE2021, TLE2022 and TLE2024 were the first operational amplifiers to be processed using the Excalibur technology. These low power products were designed using the new high speed vertical PNPs available in Excalibur, and the result is a family of devices that offer significant AC performance with minimal supply currents.

TLE2021/2/4 - LOW POWER PRECISION OP AMP

Low Power, Precision AND Speed

- Vertical PNPs enable outstanding Speed/Power Performance;
  - Icc = 235μA
  - BW = 2.8MHz
  - SR = 0.9V/μs
- Low offset voltages;
  - TLE2021B= 100μV (max)
- Low Drift;
  - Vio = 2μV/°C
  - Vio = 5nV/month
  - Icc = 0.08μA/°C
- Single or Dual Supply operation to 40V

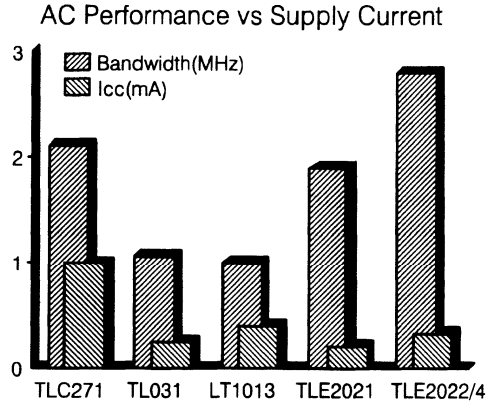


Figure 1.30 TLE202X Low Power Precision Op Amps

Improved AC Performance - The graph above compares the Bandwidth and Supply current for a number of low power operational amplifiers. It immediately shows that all TLE2021/2/4 devices achieve much improved bandwidth without any increase in supply current. Performance in fact exceeds that of some Bifet and CMOS op amps.

Slew rate is also significantly improved when compared to low power alternatives - typically 0.9 V/μs from 235 μA. The device is now a viable alternative to Bifet and CMOS designs which are often used for their improved AC performance.

Precision - What further makes this device stand out is its suitability for precision applications. The tightest selection has a maximum offset of just 100 μV. This combined with a high Open Loop Gain (A_{vd} equals 120 dB), and superior stability with time and temperature results in an amplifier ideal for low power instrumentation, test and measurement equipment. The op amps offsets will typically vary by 2 μV/°C and 5 nV/month - this equates to a V_{io} change of 1 μV in 16 years!

The 'A' selection part has 200 μV maximum offset voltage and the standard part has a Vio of 500 μV.

Performance stability - In addition to low offset voltage drift, a patented bias circuit was designed using Excalibur's JFETs. The result is that the supply current varies typically by 0.08 μV/°C. In fact ALL temperature versions specify the same supply current spec. at both 25°C and over the full range.

Supply current stability has a number of system benefits above its obvious advantage to low power circuits. Supply current impacts the performance of most op amp parameters, including gains, slew rate, bandwidth, offset voltage, bias currents and even the output drive capability. By maintaining a relatively constant supply current, the drift with temperature of these other specifications is also reduced. Well defined and constant system performance with temperature is very achievable.

Single or Dual Supply Operation - Using Excalibur's new PNPs, the devices have a common mode input range down to the negative supply (0 V to 3.2 V from 0 V and 5 V supplies) and so are the ideal choice for low level, single supply single conditioning applications. The absolute maximum voltage range is +/-20 V, so applications with large supply voltages for increased dynamic range can also benefit.

Phase-Reversal Protection - All devices feature phase-reversal protection circuitry that eliminates unexpected change in output states when one of the inputs goes below the negative rail.

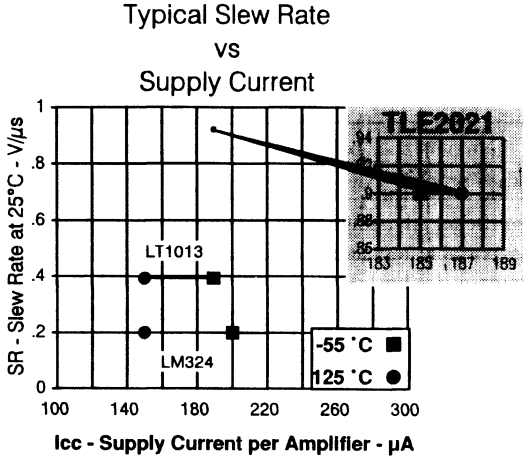
Applications - Low power systems will benefit the most from using the TLE2021 family of op amps. Several hand-held Telecom equipment gain a significant advantage from the combination of low power consumption and good AC performance, while portable test and measurement applications can take full advantage of the precision and stability of these designs. The parts have been used in magnetic sensors, process monitoring and control equipment, and also single supply instrumentation systems such as interfacing to a strain gauge.

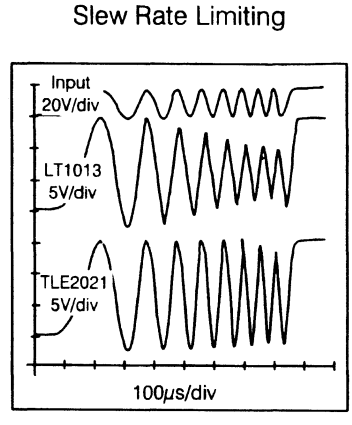
5.4. TLE202X AC Performance

5.4.1. TLE2021 Slew Rate verses supply current.

It is unusual for low power bipolar operational amplifiers to achieve significant levels of AC performance, but by making use of Excalibur's high speed vertical PNPs, the TLE2021 family of precision op amps have achieved slew rates of up to 5-times higher than other low power bipolar designs. The graph above compares the AC performance of the TLE2021 against the LT1013, OP21 and the LM324

This graph also shows the supply current stability of these designs with temperature. By designing the current source using a patented circuit designed with Excalibur's JFETs, it has been possible to develop a part which has practically zero drift in supply current. Because supply current is a major factor in many other op amp parameters, this stability of Icc is also carried over to other specifications. The stability of everything from V_{IO} to slew rate is improved!





TLE202X AC Performance

5.4.2. TLE2021 Improved AC performance

The second graph in this figure highlights how an improvement in slew rate can affect the actual signal clarity achievable from an op amp. A 20 V pk-pk sine wave with a swept frequency is fed into a simple unity gain operational amplifier circuit. It can be seen that the LT1013 starts to slew rate limit at only 6 kHz, causing signal degradation and a reduction in magnitude. The TLE2021 is still performing comfortably at 14 kHz.

5.5. Precision 2-Wire 4 to 20 mA Current Loop

5.5.1. What is a Current Loop?

Often information from an analogue sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The most commonly used current loop interface standard consists of a minimum of two wires providing both the power supply for the sensor and signal conditioning circuit as well as transferring the information sensed in form of a current, which varies proportionally with the measured signal. The current in the loop varies usually from 4 ma, corresponding to no signal, to 20 mA for full

scale - referring to the well known 4 to 20 mA current loop. Up to 4 mA of the loop current can be used for supplying the sensor, signal conditioning and voltage-to-current converter.

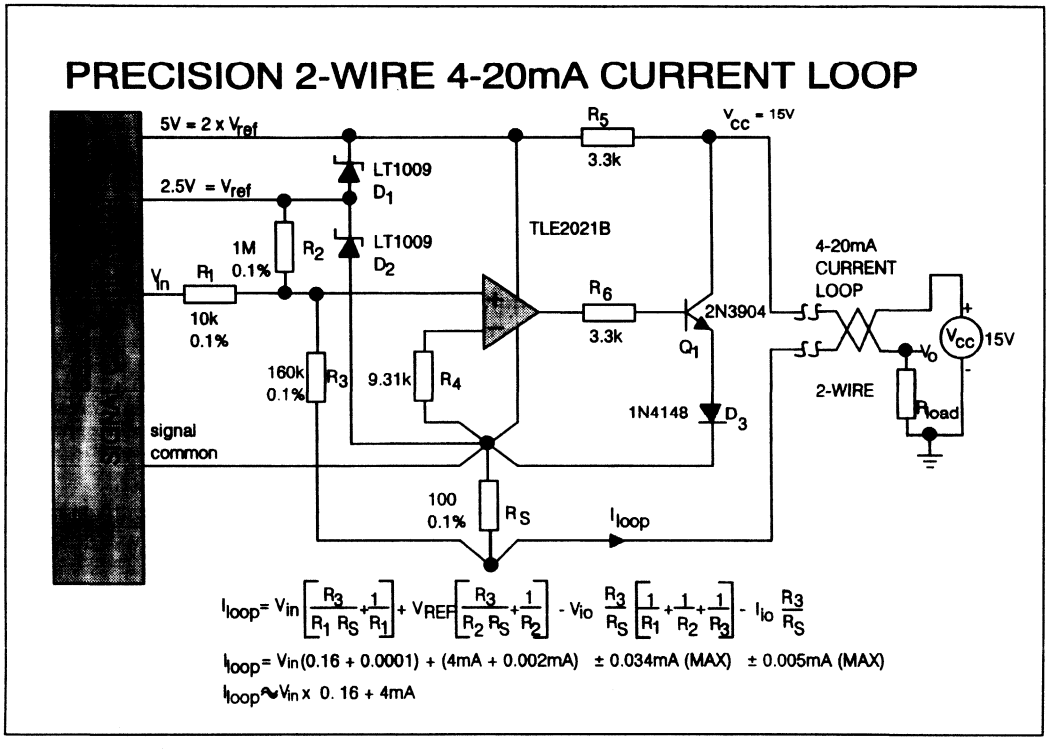


Figure 1.31 Precision 2-Wire 4 to 20 mA Current Loop

Precision 4 to 20 mA Current Loop

The circuit presented provides a 4 to 20 mA output current for a 0 to 100 mV input voltage. By modifying R_1, R_2 and R_3 the input range or the output current can be adjusted. The total error is kept very low provided that the recommended precision components are used.

The employed Excalibur op amp, the TLE2021B, is a high performance op amp well suited for this type of application. The TLE2021B is here configured as a voltage-to-current converter, transmitting a very stable loop current, I_{loop}, proportional with the input voltage, V_{in}. The converter's transconductance or "gain" can be adjusted by R_1 and its current-offset varies with R_2. Resistor R_4 reduces the influence of the op amp's input bias current to that of its input offset current.

The loop current is divided up in three major paths: The primary current path is through transistor Q_1, whilst the secondary paths are via the reference and through the op amp. All current flowing through R_S is within the controlled and regulated 4 to 20 mA current loop. The current flowing through R_3 is outside the loop control and contributes to the circuit's total error. This current can be taken into consideration in the design equations but with the chosen component values, its error becomes insignificant.

High system accuracy and stability is achieved without trimming by using two LT1009 voltage references in series producing a precision +5 V reference. This implementation not only provides a stable 0.2% precision reference for the voltage-to-current converter but also ensures that picked up noise and hum from long loop wires are suppressed from the op amp supply by the reference element's low dynamic impedance. In addition, the reference and its +2.5 V centre point are available for external signal conditioning circuitry, provided that a limited current is taken. The converter itself needs a minimum of 630 µA (400 µA for the reference and 230 µA for the op amp), leaving (4 - 0.63) mA = 3.37 mA to be used by additional circuitry. If really low power is required, the LT1009 voltage references should be replaced by LT1004s reducing the quiescent current consumption to basically that of the TLE2021B op amp or 240 µA.

Why use the Excalibur TLE2021 Op Amp?

- **Common Mode Input Voltage to Negative Supply Rail**
  By analysing the application it is seen that the input common mode voltage is zero volt.
- **5V Single Supply Capability**
  This op amp feature eliminates the need for a third negative supply wire or a charge-pump creating a negative rail from the positive. Also, the low minimum operational voltage is utilised.
- **Output Swing Close to the Negative Rail**
  By analysing the circuitry it is seen that an output swing down to two V_{be} from the negative rail is required. Few dual supply op amps can actually swing that low.
- **Low Power Consumption**
  A total of 4 mA is available for the converter and sensor interface. TLE2021 uses less than 230 µA leaving more current for other parts of the circuit.
- **Low and Stable Input Offset Voltage**
  From the output current expression on the figure, it is clear that low input offset voltage is required. A 1 mV offset voltage would contribute with a current error of 0.17 mA. The TLE2021B with its maximum input offset voltage of 100 µV(200 µV max @ 5 V supply) gives low error. Additionally, its offset voltage also remains stable with temperature and time featuring 2 µV/°C and 5 nV/month typical drift.

5.5.2. Design Details

Assuming that the voltage at the non-inverting input terminal of the TLE2021B is of zero volt relative to "Signal Common", and that $I_{R_S} = I_{loop}$, the sum of the currents at the non-inverting terminal gives:

$$\frac{V_{in}}{R_1} + \frac{V_{ref}}{R_2} - \frac{I_{loop} R_S}{R_3} = 0;$$

Solving this with respect to I_{loop} gives:

$$\boxed{I_{loop} = V_{in} \frac{R_3}{R_1 R_S} + V_{ref} \frac{R_3}{R_2 R_S}} \quad (1)$$

The design equations specifying the resistor values can be derived from (1). Assuming

V_{ref} = 2.5V and V_{in} ranges from 0- to 100 mV, it follows:

(a) $I_{loop(min)} = V_{ref} \frac{R_3}{R_2 R_S} \quad \Rightarrow \quad 4\text{ mA} = 2.5 \frac{R_3}{R_2 R_S}$

(b) $I_{loop(max)} = V_{in(max)} \frac{R_3}{R_1 R_S} + 4\text{ mA} \quad \Rightarrow \quad 20\text{ mA} = 0.1 \frac{R_3}{R_1 R_S} + 4\text{ mA}$

Equation (a) and (b) have in total four unknown resistor values. By choosing two of them the equations decide on the other two. The basic guidelines applied for the choice of the resistor set satisfying (a) and (b) are:

R_S should be small to minimise its voltage drop. Two problems are associated with a high voltage drop across R_S. Firstly, it causes variation in the reference diodes current with the loop current and hence affects their stability. Secondly, a high voltage drop increases the current flowing outside the control loop through R_3. However, very small resistor values are not available with high accuracy - say 0.1%, but a good compromise is 100 Ω.

R_1's value is a compromise between minimising errors resulting from the op amp's input offset currents, I_{IO}, to a level below that of the op amp's offset voltage, and simultaneously not loading the source. With $I_{IO(max)}$ = 3 nA, a 10 kΩ resistor gives only 30 µV offset error compared with the op amp's 200 µV (max) offset voltage at 5 V supply. $R_4 = R_1 \| R_2 \| R_3$ ensures that only input offset current rather than input bias current contributes to the error.

R_2 should maximum be 1 MΩ to allow a 0.1% high precision resistor to be used.

R_3 should be as high as possible to limit the current flowing outside the control loop but satisfy the same criteria as for R_2.

A set of values satisfying the above criteria and equation (a) and (b) is:

$R_S = 100\ \Omega$; $R_1 = 10\ k\Omega$; $R_2 = 1\ M\Omega$; $R_3 = 160\ k\Omega$; $R_4 = 9.32\ k\Omega$;

R_5 delivers the current required for the LT1009 shunt references, the op amp plus additional current for the sensor and its interface circuit. This current is stable with constant V_{in} but as the voltage drop across R_S varies with I_{loop}, the drop across R_5 varies as well. This in turn causes the current through the LT1009 references to shift accordingly. To avoid changes in the reference voltage this current must be kept fairly stable; hence the drop change across R_5 must be minimised placing constraints on a minimum power supply voltage and the value of R_{load}. Choosing R_5 = 3.3 kΩ causes the current in the LT1009 references to vary by only 700 µA, provided that R_{load} = 50 Ω. This choice also allows for up to 1.5 mA reference current to be used for the sensor and its interface.

Error budget

The op amp's offset error, V_{IO}, modifies the loop current, I_{loop}, of equation (1) as the voltage at the non-inverting input is $\pm V_{IO}$ rather than zero volt with respect to Signal Common assumed for (1). If the op amp's input offset current, I_{IO}, is taken into consideration, it should be summed with the other currents at the non-inverting terminal of the op amp. This yields:

$$\frac{V_{in} - V_{io}}{R_1} + \frac{V_{ref} - V_{io}}{R_2} - \frac{I_{loop} R_S + V_{io}}{R_3} - I_{io} = 0 ; \quad \Rightarrow$$

$$I_{loop} = V_{in}\frac{R_3}{R_1 R_S} + V_{ref}\frac{R_3}{R_2 R_S} - V_{io}\frac{R_3}{R_S}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right) - I_{io}\frac{R_3}{R_S}; \qquad (2)$$

An additional error source adding to I_{loop} of (2) is the current bypassing the control loop through R_3. All current passing through R_S is inside the control loop. In equation (1) we assumed that $I_{loop} = I_{RS}$ but a more correct expression is:

$$I_{loop} = I_{RS} + I_{R3} \quad \text{or} \quad I_{loop(3)} = I_{loop(1)} + I_{R3};$$

where $I_{loop(1)}$ is I_{loop} given by (1). By ignoring the insignificant effect from the op amp's offset error on the bypass current error: $V_{R3} = V_{RS} = I_{loop(1)} R_S$ resulting in:

$$I_{loop(3)} = I_{loop(1)} + I_{loop(1)}\frac{R_S}{R_3} \quad <=> \quad I_{loop(3)} = I_{loop(1)}\left(1+\frac{R_S}{R_3}\right);$$

Substituting $I_{loop(1)}$ with I_{loop} of (1) yields:

$$I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S}+\frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S}+\frac{1}{R_2}\right);$$

By adding the errors contributed by V_{IO} and I_{IO} in equation (2), ignoring the insignificant effect from the bypassed loop current on these errors, we have:

$$I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S}+\frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S}+\frac{1}{R_2}\right) - V_{io}\frac{R_3}{R_S}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right) - I_{io}\frac{R_3}{R_S}$$

The difference between the worst case $I_{loop(3)}$ at 25°C and the ideal $I_{loop} = V_{in}\,0.16 + 4$ mA is specified in the following error table:

Errors in 4- to 20 mA Current Loop Circuit		**Worst Case Error**		
Error Relative or Absolute	**Tolerance Source**	**Low Level**	**Full Scale**	**Unit**
R_1, R_2, R_3, R_S	0.1%	12.0	60.1	µA
V_{ref}	0.2%	8.0	8.0	µA
V_{IO}	200 µV	34.3	34.3	µA
I_{IO}	3 nA	4.8	4.8	µA
I_{R3}	(R_S/R_3) I_{loop}	2.5	12.5	µA
Total Worst Case Error in I_{loop}		±61.6	±119.7	µA
Total Worst Case Error in % of Ideal I_{loop}		±1.5	±0.6	%

Note: Low Level = 4 mA, Full Scale = 20 mA.

The worst case untrimmed error of ±0.6% for full scale at 25°C is mainly dominated by resistor tolerances and the op amps input offset voltage. The chance of the individual errors being worst case and contributing in the same direction or adding up with the same sign is unlikely - so typically, the performance will be much better. However, by trimming R_2 for low levels (4 mA) and R_1 for full scale (20 mA) all of the above errors can be eliminated, reducing inaccuracy to drift with time and temperature of the same parameters. Such a trimmed circuit can achieve a similar accuracy as the untrimmed one at 25°C but over a 0°C to 70°C temperature range.

5.6. Low Power High Performance Band-Pass Filter

High Q, High Frequency Filters

Designing active filters of high order requires high Q factors of each second order building block, usually cascade coupled, to achieve the overall wanted filter response. Simple second order building blocks constructed around a single standard 1 MHz type op amp suffer from high Q sensitivity to passive components and op amp gain accuracy. If a Q of 10 has to be implemented the maximum frequency is normally restricted to below 1 kHz. Some network topologies offer however little passive sensitivity but require more op amp open loop gain at the frequencies of interest. Multiple op amp second order filter building blocks are often the preferred solution for high Q high frequency filters as the Q sensitivity with respect to the individual op amps is reduced.

In recent years, active compensation of the op amp's first pole has been frequently described in articles. Such schemes allow standard 1 MHz op amps to be used at frequencies up to a decade higher than with previous designs. However, the knowledge to the op amps exact dominant pole frequency is usually required in order to cancel its effect with a second op amp. Multiple monolithic op amps like duals or quads with their better matched frequency characteristics alleviate the problem to some extent and topologies compensating for both first and second effects in the op amps open loop frequency response exist too.

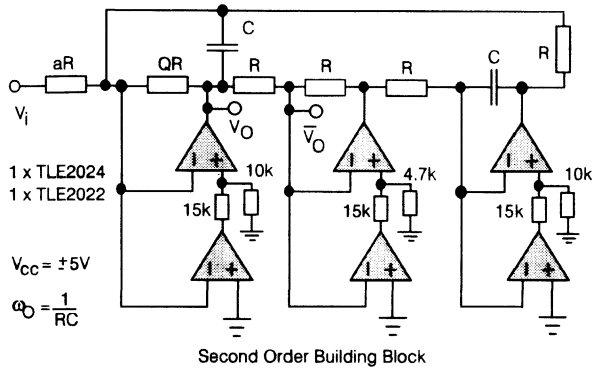
5.6.1. High Quality Bandpass Filter Building Block

Double integrator loop second order building blocks are most often used for high Q implementations. Circuit configurations exist offering simultaneously lowpass, highpass and bandpass outputs from the same three op amp structure. Adding a fourth op amp makes bandstop filter circuits possible.

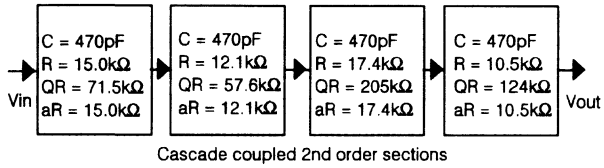
The figure shows a high quality second order building block which has been designed for bandpass implementations only. Very desirable properties are available, such as both non-inverting and inverting outputs and a simple summing node option, allowing for use in active latter structures or leap-frog network applications.

Active compensation within the given double integrator loop occurs automatically without any critical matching requirements on the passive components, and without the need for matched op amps, which are in reality never obtainable. The pole frequency, $\omega_0 = 1/(RC)$ and the gain factor, $k = 1/a$, realised by the bandpass building block are both independent of the op amps gain-bandwidth products, so that the design equations become very simple, and gain-bandwidth product variations have no effect on the centre frequency of the overall filter. Convenient nominal values, R, C, QR and aR have been given for the passive components, but, neither the phase nor the magnitude compensation that occurs in the

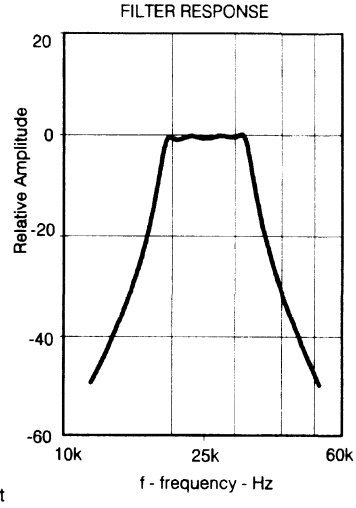
double integrator loop, is affected by deviations of the passive component values from the nominal suggested.



Second Order Building Block



Cascade coupled 2nd order sections



Low Power High Performance Band-Pass Filter

The transfer function can be derived as:

$$V_O = - V_i \frac{\frac{1}{Cs} \parallel (QR)}{aR} - V_O \frac{1}{RCs} \frac{\frac{1}{Cs} \parallel (QR)}{R}; \qquad \Rightarrow$$

$$\boxed{\frac{V_O}{V_i} = -\frac{1}{a} \frac{\frac{1}{RC} s}{s^2 + \frac{1}{RC}\frac{1}{Q} s + \frac{1}{R^2C^2}} = k \frac{\omega_O s}{s^2 + \frac{\omega_O}{Q} s + \omega_o{}^2}; \qquad (1)}$$

The design equations become very simple:

$$\text{Choose C;} \quad \text{Calculate} \quad R = \frac{1}{C\,\omega_o}; \quad RQ = \frac{Q}{C\,\omega_o}; \quad aR = \frac{1}{k\,C\,\omega_o}; \qquad (2)$$

Higher Order Chebychev Bandpass Filter Design

A higher order bandpass filter can be realised by simply cascade coupling more second order sections using the building block just described.

When designing a Chebychev bandpass filter the following requirements determine the order, ripple, Q and ω_o of the individual sections:

1. A Chebychev filter's normalised ($\omega_o = 1$) lowpass frequency response, $|H(j\omega)|$ is given by:

$$|H(\omega)| = \frac{1}{\sqrt{1 + \varepsilon^2 \cosh^2(n \cosh^{-1}\omega)}}; \qquad (3)$$

where $\omega = 2\pi f$, n = filter order and $\varepsilon^2 = 10^{\frac{\text{xdB filter ripple}}{10}} - 1$;

Once the acceptable pass-band filter ripple has been decided, and the required attenuation at $\omega = \omega_1$ (measured relative to the frequency, $\omega_H = 2\pi f_H$; which is the frequency where the amplitude versus frequency response leaves the ripple box) is given, the minimum low pass filter order can be calculated from (3) by solving the equation with respect to n:

$$n = \frac{\cosh^{-1}\left(\sqrt{\frac{|H(\omega_1/\omega_H)|^{-2} - 1}{\varepsilon^2}}\right)}{\cosh^{-1}(\omega_1/\omega_H)}; \qquad (4)$$

choose the normalised low-pass filter order as half the next whole even number greater than n.

2. The next step is to determine the bandpass filter's centre frequency, ω_{oBP} and bandwidth, B. Initially we consider the normalised bandpass filter with $\omega_{oBP} = 1$. A Chebychev filter's bandwidth is the difference in frequency between the highest frequency f_H where the amplitude versus frequency characteristic leaves the ripple box and f_L, the lowest frequency where the response leaves the ripple box. The normalised filter's bandwidth will be placed with logarithmic symmetry around the centre frequency of the filter, e.g.:

$$B = f_H - f_L = 10^x - 10^{-x} \Rightarrow 10^x = \frac{B}{2} + \frac{1}{2}\sqrt{B^2 + 4}; \quad \text{where } f_H = 10^x \text{ and } f_L = 10^{-x} \qquad (5)$$

3. Q_{LP} and ω_{oLP} for the individual filter stages of a n'th order normalised lowpass filter with the decided ripple is found in a standard filter table. These normalised ($\omega_o = 1$) lowpass filter parameters are now transformed into normalised ($\omega_o = 1$) bandpass filter parameters, Q_{BP} and ω_{oBP} by the following equations:

A first order low-pass section is converted into a second order bandpass section by:

$$Q_{BP} = \frac{\omega_o}{B\,\omega_{oLP}}; \quad \omega_{oBP} = \frac{\omega_o}{2\,Q_{BP}}; \qquad (6)$$

A second order lowpass section is converted into a second order bandpass section by:

$$Q_{BP1} = Q_{BP2} = Q_{BP} = \frac{Q_{LP}}{\sqrt{2}} \sqrt{1 + \frac{4}{\delta^2} + \sqrt{(1 + \frac{4}{\delta^2})^2 - \frac{4}{\delta^2 Q_{LP}^2}}}; \quad (7)$$

$$\omega_{oBP1} = \frac{\omega_o}{2}\left(\delta \frac{Q_{BP}}{Q_{LP}} + \sqrt{(\delta \frac{Q_{BP}}{Q_{LP}})^2 - 4}\right); \quad (8)$$

$$\omega_{oBP2} = \frac{\omega_o}{2}\left(\delta \frac{Q_{BP}}{Q_{LP}} - \sqrt{(\delta \frac{Q_{BP}}{Q_{LP}})^2 - 4}\right); \quad (9)$$

Where $\delta = \frac{B}{\omega_o}\omega_{oLP}$; $\omega_o = \omega_{oBP1} * \omega_{oBP2} = 1$; (normalised bandpass filter).

4. Finally, relating the design to the actual described second order bandpass building block the component values can be determined from:

   Choose the value of the capacitors, C. Then calculate the resistors and include the de-normalising frequency transformation:

   $$R = C * \omega_{oBP} * \omega'_o/\omega_o; \quad (10)$$

   Where ω'_o is the de-normalised and total bandpass filter's centre frequency.

8th Order Chebychev Design Example

This section demonstrates a filter design example using the high performance second order building block and theory outlined in the previous sections.

We will construct a low power, bandpass filter with a centre frequency of 25 kHz and a bandwidth of 12.5 kHz. A maximum ripple of 0.5 dB in the pass-band is acceptable and a minimum attenuation of 65 dB below 10 kHz and above 62.5 kHz is required.

- Normalising the centre frequency of 25 kHz to $\omega_o = 1$ gives a normalised bandwidth, $B = 0.5$;
- From (3): $\varepsilon^2 = 10^{0.05} - 1 = 0.122018$;
- From (5): $f_H = 0.5/2 + 0.5\sqrt{0.5^2 + 4} = 1.2808$ and $f_L = 1/f_H = 0.7808$;
- Normalising the geometric symmetric frequencies, 10 kHz and 25 kHz gives 0.4 and 2.5 respectively. $\omega_1 = 2.5$ relative to f_H is then given by $\omega_1/f_H = 2.5/1.2808 = 1.9519$;

  $|H(\omega_1/\omega_H)| = 10^{-65dB/20} = 0.5623 * 10^{-3}$;

- From (4): $n = \dfrac{\cosh^{-1}\sqrt{\dfrac{(0.5623 * 10^{-3})^{-2} - 1}{0.122018}}}{\cosh^{-1} 1.9519} = 7.16$; =>

  Normalised lowpass filter order = 8/2 = 4 => two second order sections;

- From a table of normalised lowpass Chebychev, 0.5 dB ripple filter parameters is found Q_{LP} and ω_{oLP} for a 4th order function:

Section	Q_{LP}	ω_{oLP}

A	0.705110	0.597002
B	2.940554	1.031270

- The two lowpass second order sections (A and B) transforms into four bandpass second order sections (1, 2, 3 and 4), for which we can now calculate the filter parameter values.

From section A: $\delta_1 = \delta_2 = B\,\omega_{oLP} / \omega_o = 0.5 * 0.597002 / 1 = 0.298501$;

From (7): $Q_{BP1} = Q_{BP2} =$

$$\frac{0.705110}{\sqrt{2}} \sqrt{1 + \frac{4}{0.298501^2} + \sqrt{\left(1 + \frac{4}{0.298501^2}\right)^2 - \frac{4}{0.298501^2 * 0.705110^2}}}\ ; \Rightarrow$$

$$Q_{BP1} = Q_{BP2} = 4.75072\ ;$$

From (8): $$\omega_{oBP1} = \frac{1}{2}\left(0.29850\frac{4.75072}{0.705110} + \sqrt{\left(0.29850\frac{4.75072}{0.705110}\right)^2 - 4}\right);\ \Rightarrow$$

$$\omega_{oBP1} = 1.11137\ ;$$

From (8): $$\omega_{oBP2} = \frac{1}{2}\left(0.29850\frac{4.75072}{0.705110} - \sqrt{\left(0.29850\frac{4.75072}{0.705110}\right)^2 - 4}\right);\ \Rightarrow$$

$$\omega_{oBP2} = 0.899789\ ;$$

From section B: $\delta_3 = \delta_4 = B\,\omega_{oLP} / \omega_o = 0.5 * 1.031270 / 1 = 0.515635$;

From (7): $Q_{BP3} = Q_{BP4} =$

$$\frac{2.940554}{\sqrt{2}} \sqrt{1 + \frac{4}{0.515635^2} + \sqrt{\left(1 + \frac{4}{0.515635^2}\right)^2 - \frac{4}{0.515635^2 * 2.940554^2}}}\ ; \Rightarrow$$

$$Q_{BP3} = Q_{BP4} = 11.7686\ ;$$

From (8): $$\omega_{oBP3} = \frac{1}{2}\left(0.515635\frac{11.7686}{2.94055} + \sqrt{\left(0.515635\frac{11.7686}{2.94055}\right)^2 - 4}\right);\ \Rightarrow$$

$$\omega_{oBP3} = 1.28614\ ;$$

From (8): $$\omega_{oBP4} = \frac{1}{2}\left(0.515635\frac{11.7686}{2.94055} - \sqrt{\left(0.515635\frac{11.7686}{2.94055}\right)^2 - 4}\right);\ \Rightarrow$$

$$\omega_{oBP4} = 0.777517\ ;$$

Summarising the parameters of the normalised second order bandpass filter sections:

Section	Q Bandpass	ω_{oBP}
1	4.75072	1.11137
2	4.75072	0.899789
3	11.7686	1.28614
4	11.7686	0.777517

- The final component values can now be determined by choosing C = 470 pF and using equation (2) and (10) to calculate the resistor values. $\omega'_O = 2\pi * 25$ kHz, $\omega_O = 1$ and aR = R gives:

Section	C	R	QR	aR
1	470 pF	Ideal: 15.05 kΩ E96 std. value: 15.0 kΩ	Ideal: 71.62 kΩ E96 std. value: 71.5 kΩ	Ideal: 15.05 kΩ E96 std. value: 15.0 kΩ
2	470 pF	Ideal: 12.19 kΩ E96 std. value: 12.1 kΩ	Ideal: 57.90 kΩ E96 std. value: 57.6 kΩ	Ideal: 12.19 kΩ E96 std. value: 12.1 kΩ
3	470 pF	Ideal: 17.42 kΩ E96 std. value: 17.4kΩ	Ideal: 205.0 kΩ E96 std. value: 205kΩ	Ideal: 17.42 kΩ E96 std. value: 17.4kΩ
4	470 pF	Ideal: 10.53 kΩ E96 std. value: 10.5 kΩ	Ideal: 123.9kΩ E96 std. value: 124 kΩ	Ideal: 10.53 kΩ E96 std. value: 10.5 kΩ

Note: If unity gain is desired in the passband for the total filter, choose a = 1/Q => aR = R/Q.

Low Power Design Using The TLE2022 and TLE2024

By implementing the above design example using the Excalibur TLE2022 dual and TLE2024 quad op amps provide excellent AC performance for very little power consumption. Although the 8th order design example requires 8 * 6 = 48 op amps, the worst case total power consumption is only 12 mA and 8.4 mA typical. This is significant less compared to a realisation using four second order integrator filter blocks each implemented around three OP27 or LT1007 op amps adding up to a total of 24 op amps, consuming in worst case 96 mA and 64 mA typical. In addition, the sensitivity to both passive and active elements would have been higher.

The TLE2022 and TLE2024's typical unity gain bandwidth of 2.8 MHz for only 250 µA supply current per op amp makes them ideal for low power filter designs - specially at low supply voltages. Operation is guaranteed and characterised down to ±2.5 V. The only consideration for AC operation at high

frequencies is their limited slew rate of 0.9 V/µs. However, this is sufficient for operation to 35 kHz with ±5 V supplies and to 85 kHz with ±2.5 V supplies.

5.7. TLE2141/2/4 - High Speed Single Supply Op Amps

The TLE2141 single operational amplifier is the latest Excalibur device. Like the other bipolar designs it uses Excalibur's high speed PNPs to enable it to achieve extremely high speed - it is probably the **Worlds fastest single supply op amp!** It combines a number of features which make it particularly well suited to high speed, precision applications particularly in control loops for system or process monitoring.

TLE2141/2/4 - HIGH SPEED SINGLE SUPPLY OP AMP

One of the WORLD'S FASTEST Single Supply Op Amps

High Speed: SR = 30V/µs min
UBW = 5.9MHz
Vo(pk-pk) = 400kHz (Vcc= +/-15V)

Fast Settling Time: 340ns to 0.1%
400ns to 0.01%

Low Noise: 10Hz.....15nV/√Hz
1kHz.....10.5nV/√Hz

Low Offsets: 500µV (max)

ALL FROM SINGLE or DUAL SUPPLIES

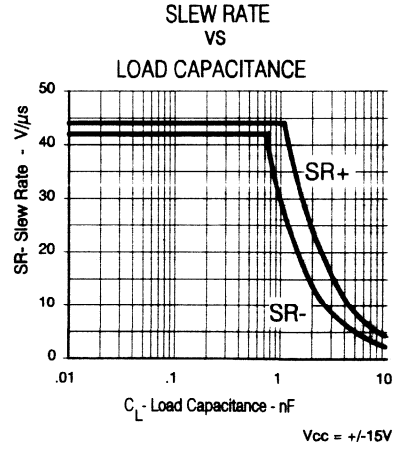


Figure 1.32 TLE2141/2/4 - High Speed Single Supply Op Amps

High Speed - The TLE2141 uses a double PNP input stage which enables it to operate from a single supply (i.e. its common mode input range includes ground). This technique has, in the past, limited the AC performance operational amplifiers - but by using Excalibur's high speed vertical PNPs and a patented input stage, the device has outstanding AC performance. The typical and symmetrical slew rate for the TLE2141 is **45 V/µs** (30V/µs min) and its **settling time to 0.01%** is typically only **400 ns**. These two parameters combined with a Gain-Bandwidth Product of 5.9 MHz highlight just why this device is so well suited to control type applications. It should be noted that the TLE2141 is internally compensated.

Low Noise - Another parameter which one does not normally associate with a single supply, PNP input, operational amplifier is low noise. The TLE2141 however has a noise voltage specification in the audio band of **15 nV/$\sqrt{\text{Hz}}$** at 10 Hz and **10.5 nV/$\sqrt{\text{Hz}}$** at 1 kHz. This combined with the excellent AC performance and resulting low distortion makes the devices particularly well suited to hi-fi audio applications.

Output Drive - The NPN output stage has been designed to swing almost Rail to Rail (V_{CC-} +0.3 V to V_{CC+} - 1.8 V) without inducing phase reversal, and will happily drive 10 nF capacitive loads. When this is combined with the 20 mA (min) short circuit output current, then the device is extremely well suited to driving heavy loads such as long cables or for use in 4-20 mA current loops.

Precision - This special design also exhibits an improved sensitivity to IC component mismatches that is evident by a 500 µV offset voltage and 1.7 µV/°C typical drift. The device also has the common mode and power supply rejection ratios set at a minimum of 85 dB and 90 dB respectively.

Applications - These wide range of features make the device extremely well suited to a number of different applications. High speed and fast settling time, combined with precision makes the device an ideal choice in fast actuator/positioning drivers or other control loop applications as well as performance audio systems. The accuracy, single supply operation (with rail to rail output) and low noise makes the TLE2141 particularly suitable for instrumentation and measuring equipment.

The device can also be configured as a comparator - both inputs can be maintained at $V_{CC+/-}$ without damage and the typical open loop propagation delay with TTL inputs is 200 ns.

5.8. TLE2142/4 High Speed Lowpass Filter

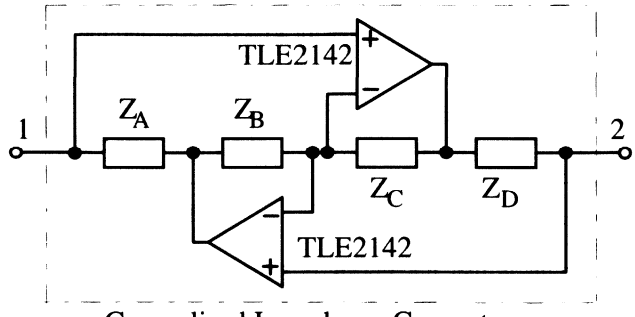
In the past most filters were built using LCR networks, this is still true for very high speed applications. The op amp, in some ways, led to the demise of the passive LCR filter. This mainly due to op amp active filters not requiring inductors.

In low frequency applications the size of inductors and capacitors would be very large limiting their use. Op amp active filters, however can reduce the size of passive components as well as introducing gain. At high frequencies the speed of the op amps have always limited the active filter's use. High speed op amps are over coming this.

Passive LCR filter network design is a highly developed field, with several books published on it. Despite this, low order filters can be easy to design, by synthesising them in a ladder form it was relatively easy to build up the filter sequentially. The largest advantage of LCR filters is their very sharp responses, that is due to the parallel LC resonance. Another advantage is their relative low sensitivity to variations of component values.

By far their largest problem is the inductor used in them. For most frequencies the inductors will normally very large and bulky. These problems are increased by their far from ideal electrical performance, being. lossy due to high serial resistance and magnetic losses.

The development of op amp gyrators has led to some interest in gyrator substituted LCR ladder filters. A gyrator, quite simply, converts an impedance to its inverse, that is a capacitor to an inductor. By converting a capacitor into an inductor the parallel LC resonance can be synthesised without the need for inductors.



Generalised Impedance Converter

A gyrator can be made quite easily from the configuration shown above, using two op amps in what has been called a Generalised Impedance Converter.

Placing another impedance Z_E between node 2 and ground the impedance seen looking into node 1 will be equal to:

$$Z_{IN} = \frac{Z_A Z_C Z_E}{Z_C Z_D}$$

Making Z_4 a capacitor while Z_1, Z_2, Z_3 and Z_5 are resistors the input impedance looking into node 1 will be:

$$Z_{IN} = \frac{R_A R_C R_E}{R_B \, 1/sC_E} = K_m s C_D$$

Where K_m equals $R_A R_C R_E / R_B$.

This has converted the capacitor into a grounded inductor, and is very useful for high pass filters. For lowpass, bandpass and bandstop filters a floating inductor will also be required. The floating inductor can be synthesised from two GICs back to back. Another way is to use Frequency Dependent Negative Resistors, FDNRs, denoted by symbol D.

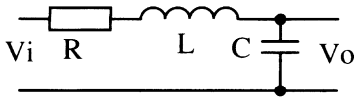
The equation of a second order LCR low pass filter is:-

$$T(s) = \frac{1/sC}{R + sL + 1/sC}$$

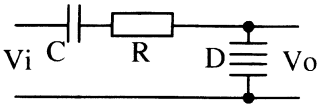
Where T(s) is the ratio of Vo to Vi. This can be converted to a circuit using FDNRs by dividing the numerator and denominator by s, the complex angular frequency operator. This transforms T(s) to:

$$T(s) = \frac{1/s^2C}{R/s + L + 1/s^2C}$$

So converting the resistor to a capacitor, the inductor to a resistor, and the capacitor to a FDNR. The circuit schematics are shown below.



LCR Lowpass Filter



CRD Lowpass Filter

The advantage of this circuit is that the FDNR is referred to ground, and only the resistors and capacitors are floating. The FDNR is made by using the GIC with Z_A, Z_B , Z_C , and Z_D as described before but with a capacitor, C_E, placed between node 1 and ground, and using node 2 as the input.

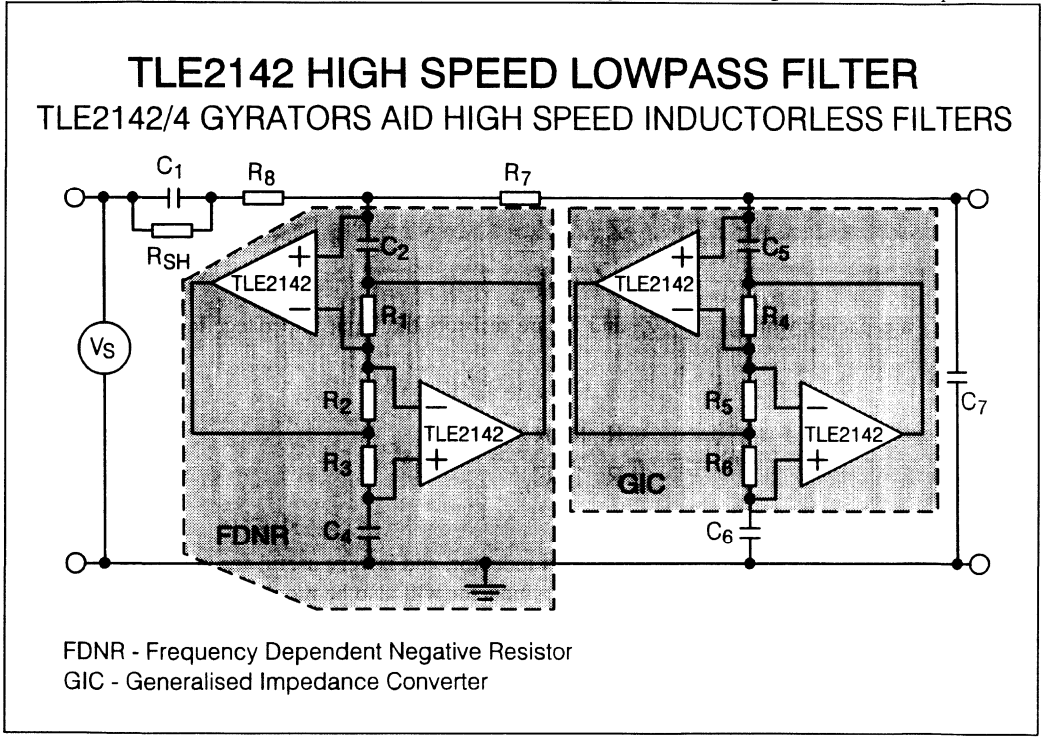


Figure 1.33 TLE2142/4 High Speed Lowpass Filter

The impedance seen looking into node 2 is:

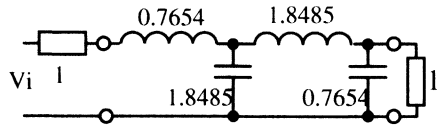
$$Z_{IN(2)} = \frac{R_B \, 1/sC_D \, 1/sC_E}{R_A R_C}$$

Expressing this in angular frequency, jω, this becomes

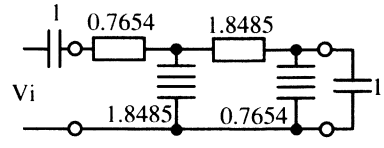
$$Z_{IN(2)} = \frac{-1}{D\omega^2}$$

A negative resistance that decreases with the square of frequency. Normalising the component values gives $R_B=R_C= 1$ and $C_D = C_E= 1$, $R_A= D$.

The figure above uses two FDNRs to make a fourth order Butterworth lowpass filter, both types of 1 Hz prototype are shown below



LCR 4th order Butterworth lowpass filter



CRD 4th order Butterworth lowpass filter

For a 20 kHz 3 dB bandwidth, the resistors and FDNRs must be scaled by, k_m, $2\pi 20000$ (125.7×10^3).

Setting all capacitors to 1 nF means that all resistors must be scaled by, k_m:

$$k_m = \frac{1}{(2\pi \times 20000)(1\times 10^{-9})} = 7958$$

Therefore $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = 1$ nF

R_n	Prototype	Value /kΩ	Component (E96) /kΩ	R_n	Prototype	Value /kΩ	Component (E96) /kΩ
R_1	1	7.958	7.87	R_2	1	7.958	7.87
R_3	1.8485	14.71	14.7	R_4	1	7.958	7.87
R_5	1	7.958	7.87	R_6	0.7654	6.091	6.04
R_7	1.8485	14.71	14.7	R_8	0.7654	6.091	6.04

Note: A shunting resistor R_{SH} is in parallel with C_1 in order to pass through the DC signal. Although low pass filters using FDNRs have in theory the right transfer functions, in reality there is a DC blocking capacitor on the input of the filter. R_{SH} shunts this capacitor out at DC, and a high value quickly makes its effect on the transfer function negligible.

The TLE2142/4 are well suited to this form of filter due to their high output current drive capability and their excellent stability. This stability shows itself in both the high slew rate and very small settling times whilst driving 500 pF capacitive loads. For greater DC accuracy the TLE2141 could be used in place of the TLE2142/4 devices.

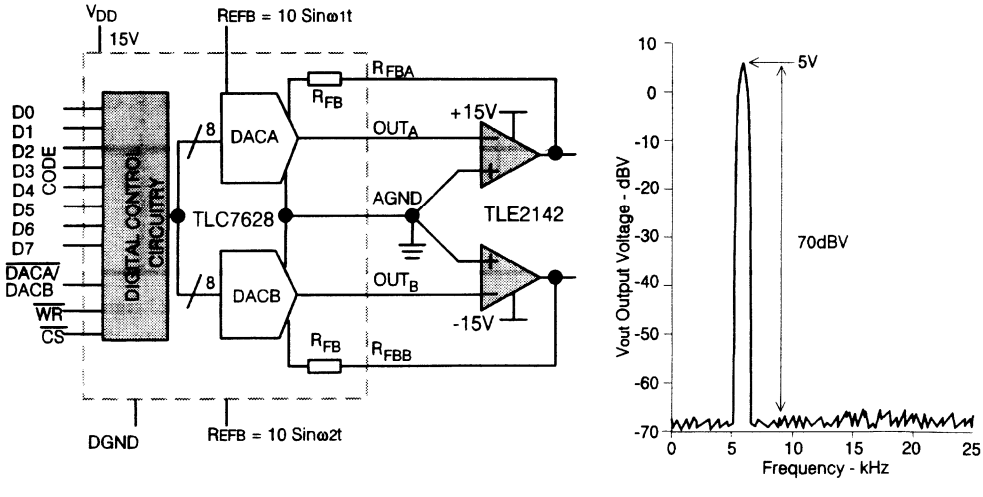
5.9. High Performance Gain Control

In today's applications analogue systems are having to interface to more and more digital systems. This is applicable to the running of the engine in a car to the production of music in your Hi-fi.

Automatic gain control in the past was done by voltage controlled resistors or some other technique of altering the resistance in a feedback loop. Interfacing to digital systems, where the digital signal processor is the control element allows much more simple and reliable techniques for AGC. Multiplying DACs are one such solution

A multiplying DAC multiplies its reference input voltage by the code fed into its digital inputs. This can be very useful where multiplication of an analogue and a digital signal is required and for AGC circuits. The **TLE2141** is well suited to these applications offering its high unity-gain bandwidth and slew-rates coupled with its low offset voltage and common-mode range down to the negative rail.

The configuration shown has numerous applications, one being as a digital audio gain adjust. With audio systems having bandwidths extending to above 20 kHz the op amp used needs to have low distortion and a good unity-gain bandwidth. Depending on the position of the op amp, it will also need a good low noise level. The TLE2142 has been designed to offer the high speed and high performance required at low noise levels.



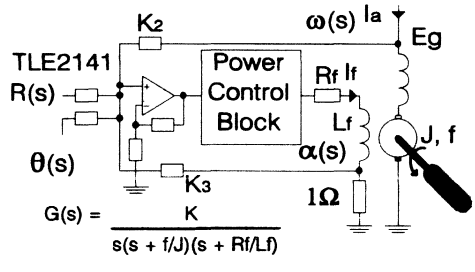
High Performance Gain Control

The DAC used must also be capable of responding to the signal level required by the system. The TLC7628 is capable of operating from a 15 V supply whilst maintaining TTL compatibility, and have reference input voltages to ±10 V. The TLC7628 is the only one of its type to be able to interface

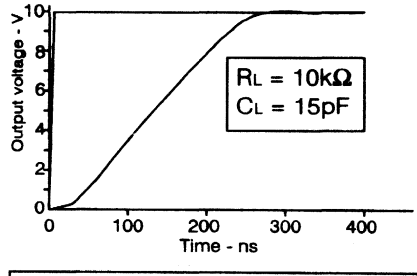
directly to Texas Instruments' DSPs. The speed of the system will be limited by the DAC; the guaranteed resistor ladder value is 20 kΩ this coupled to the maximum output capacitance due to the ladder of 120 pF gives a 3dB bandwidth of 66 kHz. This is more than ample for audio, for higher speeds of operation the feedback resistors R_{FB} can be made smaller; reducing the time constant and gain. The reduced gain may not be a problem as the DAC would essentially function as a digital attenuator, and so for noise optimisation would be preceded by a form of pre-amp.

5.10. High Performance Control Circuits Amplifier

A common linear function in which performance amplifiers are frequently used is in electronic control systems. An analogue measurement element requires signal processing before it is measured and fed back to the control element. In the past these systems were predominantly analogue, however DSP based systems are becoming increasingly common - in both cases linear signals must be handled and op amps are the main signal conditioning element.



Inverting large signal pulse response



Control circuit Op amp requirements

Accuracy -	Low Offset High Gain
Versatility -	CMR to -ve Rail
Speed -	High Bandwidth Large Slew Rate Small Settling Times

TLE2141 Settling Times
0.1% = 10bits in 340ns (typ)
0.01% > 13bits in 400ns (typ)

Control Circuits Amplifier

This figure shows a typical analogue system, where the control element has to monitor and affect the position of a field controlled motor. The normal operation of the motor has a transfer function of G(s) between the control input voltage, r(s), and the motor position θ(s). Stability of the system can be assured by measuring key variables within the system and feeding them back to the input. By sensing

the field current, it is possible to evaluate the torque and/or acceleration of the motor (this is the second derivative with respect to time of the position of the motor). The back e.m.f. developed across the motor can be used to find its angular velocity (the first derivative with respect to time of the position of the motor). Feeding these signals back to, and comparing them with, the actual excitation of the sensor, makes it is possible to evaluate and control the position of the motor..

In the above, and other analogue systems, the signal processing modifies the open loop system gain, in a way similar to how an op amp's feedback changes its open loop gain. A technique called 'State Variable Feedback' (often used in active filter design), is frequently used in analogue systems - Here the control network uses differentials and integrals of the feedback signal in order to change the systems operation and ensure stability. It is in these functions that operational amplifiers are commonly used.

In Digital systems the signal conditioning circuits perform more of a typical function - signals are filtered, amplified and level shifted to ensure they are in a format suitable for an ADC. A form of State Variable feedback is also used in digital systems - known as PID (Proportional, Integral and Derivative) control, again measurements are taken of the control signal before they are fed back to the system.

The key factor however is that both systems require performance operational amplifiers. High speed and fast settling times reduce delays and improve response times, low offsets and high open loop gains improve system accuracy. While the ability to operate from single or dual supplies with wide common mode input and output ranges improves flexibility and increases dynamic range. All these factors were specifically considered when Texas Instruments developed the TLE2141, the latest op amp designed using the Excalibur technology. The part, developed for use in single or dual supply applications, has an impressive 45 V/µs slew rate and very impressive settling times.

AC performance and fast settling times are critical parameters if an op amp is to be used effectively in a control system. An op amp can be approximated to a two pole model, the compensation capacitor splits the poles of the op amp creating a low frequency dominating pole. The op amp's feedback modifies the position of the dominating pole and raises it to a frequency similar to that of the second pole. When a pulse is applied to an op amp, it is the interaction of these two poles which give the characteristic exponential decaying sine wave superimposed upon on the pulse input. The position of the second pole determines the stability of the pulse response - if it is too low (implying a poor phase margin), large overshoots and long settling times will occur. Large overshoots can cause a system to swing the 'wrong way' and poor settling time can result in the system not reaching equilibrium. An example of a critical system is a hard-disc drive - here response time is crucial and poor op amp stability could cause the reader head to crash into the disc. Therefore in high speed systems an op amp requires not only a fast slew rate but must also have a good settling time and large phase margin.

As highlighted, the TLE2141 provides a phase margin of 58°, 42 V/µs slew rates and a settling time to 0.01%(12 bit or greater) of just 400 ns. The slew rate therefore ensures a fast pulse rise time and the large phase margin will quickly damp the overshoot, making the part ideal for these form of applications. To minimise the overall steady state error the op amp must have a small DC. error. The TLE2141's high open loop gain coupled with its offset voltage of 500 µV provide the very small steady state errors required by many systems, including those where high speed might at first seem to be the only requisite.

5.11. TLE2027/37 - Precision Excalibur Op Amps

The TLE2027 and TLE2037 are among the most recent op amps to be developed and fabricated using the Excalibur technology. These devices have been optimised for precision and include a novel output stage that features a 'Saturation Recovery Circuit' which enables much improved small signal response and outstanding levels of distortion.

Precision - The parameters of most importance in a precision application are; Offset Voltage, Drift, Bias Currents and Open Loop Gain - both these devices have outstanding performance in all these areas. The TLE2027A and TLE2037A have a maximum offset voltage of only **25 µV** and a maximum offset voltage drift of **1 µV/°C and 1 µV/month**. A bias current cancellation circuit reduces bias currents to typically 6 nA enabling larger external resistors without impacting overall DC accuracy.

An outstanding parameter of both devices is their open loop gain, **Avd; - at 153 dB**, it is probably the **highest in the world!** The resulting improvement in the op amps circuits 'loop-gain' causes an increase in overall performance - everything from offset voltage, input impedance and distortion are improved.

TLE2027/37 - PRECISION EXCALIBUR OP AMP

Low Noise, High Speed and Precision

Low Input Offset Voltage;
TLE2027A/37A ..... 25µV max

High Open Loop Gain ..... 45V/µV or 153 dB!!!

Low Noise Voltage;
3.3nV/$\sqrt{Hz}$ @ 10Hz
2.5nV/$\sqrt{Hz}$ @ 1kHz

Wide Bandwidth;
TLE2027 ..... 15MHz
TLE2037 ..... 76MHz (Decompensated)

Output Features Low Distortion and Saturation Recovery

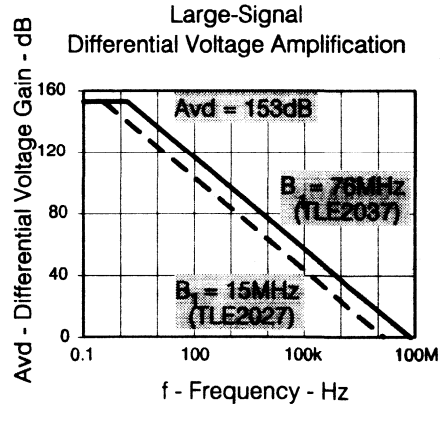


Figure 1.34 TLE2027/37 - Precision Excalibur Op Amps

AC Performance - The TLE2037 is a decompensated version of the TLE2027. It must be used with a minimum closed loop gain, Acl, of 5, but the unity gain bandwidth product for the **TLE2037 is**

80 MHz (compared with **15 MHz** for the TLE2027). Slew Rates for the TLE2027 and TLE2037 are 2.8 V/µs and 7.5 V/µs respectively.

Low Distortion - Linked to an increase in AC performance both devices feature a **Saturation Recovery Circuit** which improves the small signal response and enables the device to be used at much higher frequencies with increased output swings. A further advantage is the extremely low levels of distortion even when driving loads as low as **600 Ω,** which has enabled the device to be used in low noise applications such as Audio systems.

Low Noise - A large input stage, and clever design and layout techniques has given the device an extremely low noise voltage specification - **3.3 nV/$\sqrt{\text{Hz}}$ at 10 Hz**, and **2.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz.** This is an obvious further benefit to precision measurement systems and audio applications.

Applications - The excellent AC performance and low noise makes the devices ideally suited to Audio and Telecom applications, whilst the low offsets and excellent overall precision has enabled the parts to be used in Instrumentation, Measurement and Test equipment.

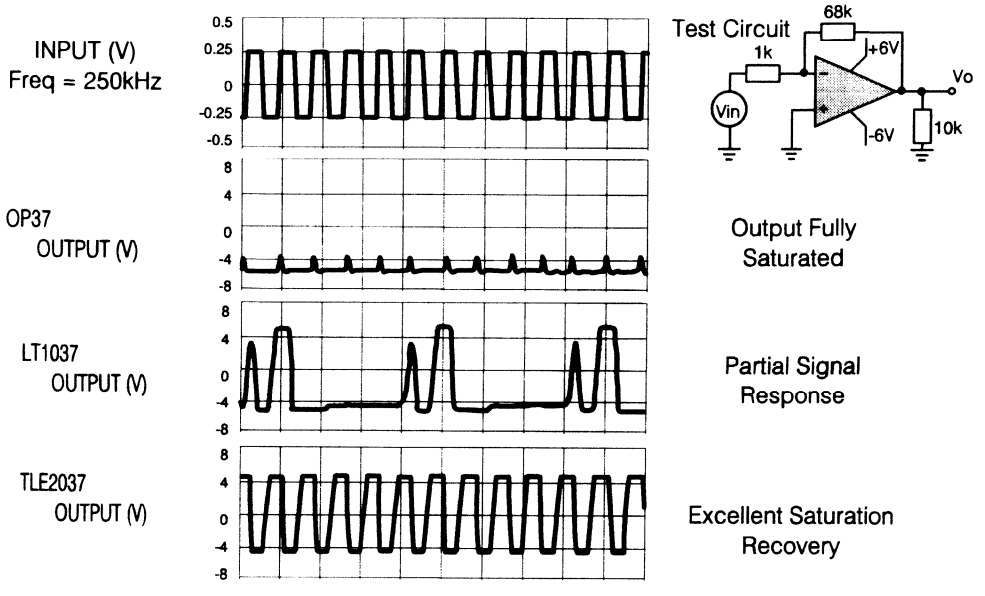
5.12. TLE2037 Saturation Recovery

In conventional OP-27 type amplifiers the output voltage remains predictable only if it stays within the V_{om} (maximum V_{out}) specification. If an input signal is applied which tries to force the output voltage beyond the V_{om} limit, the output may not respond correctly to subsequent input signals until after a given amount of time has passed. This time is the "Output Saturation Recovery Time".

There are three things that can cause the OP-27 type amplifiers to exhibit output saturation recovery problems. First, in some of the amplifiers, the final common emitter gain stage is allowed to be driven heavily into saturation. the excess base charge built up on the device can only be removed via a high value pull down resistor. Therefore a finite time must pass before enough charge is removed to assume normal operation.

Secondly, the current sources in the class AB output stage are also allowed to saturate. These are not driven as heavily into saturation, but they will also take a finite amount of time to recover.

Thirdly, and perhaps most importantly, the bias generator for the entire circuit can be disturbed from its equilibrium point when the output stage current sources saturate. If disturbed enough, the bias circuit can shut off completely until the start-up circuit engages. If this happens the entire circuit loses power and the output signals will not become valid again until the bias generator recovers from its equilibrium point. This results in a huge output saturation recovery time.



TLE2037 Saturation Recovery

In the TLE2027/37, special circuitry has been added to keep the final gain stage and the output stage current sources out of saturation. Therefore, no saturation recovery time is needed and the device continues to operate in a normal, stable and predictable manner.

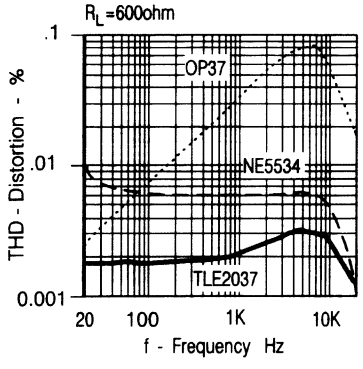
5.13. TLE2037 Distortion Measurements

The graphs below compare the 'Total Harmonic Distortion + Noise' of 3 different op amps, over frequency, whilst driving 100 kΩ and 600 Ω loads.

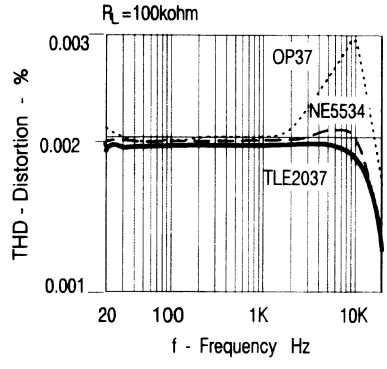
The three amplifiers highlighted in the graphs (the NE5534, LT1037 and TLE2037) are all bipolar designs and have been chosen because of their specified low levels of noise and distortion. These graphs highlight the superior performance of the TLE2037 Excalibur op amp.

The THD of an amplifier is dependent upon many parameters, specifically the open loop gain, bandwidth, slew rate, load and the input signal magnitude. The circuit used to compare these three amplifiers emphasises many of these points. A non-inverting gain of 40 dB has been chosen to highlight the importance of the loop-gain of the op amp. To ensure that noise does not conceal the THD of the op amps a 22 kHz noise filter has been introduced - this explains the shape of all curves at high frequencies. This frequency is however wide enough to highlight any problems due to slew rate limiting.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



A_V = 100
V_O = 20V Pk-Pk
Vcc = +/- 15V
22kHz Filter



Measured on Audio Precison Distortion Analyser

TLE2037 Distortion Measurements

Loop gain (the difference, 1+Aβ, between the open loop and closed loop gain curves) is a crucial factor in low distortion circuits. This, combined with the obviously low levels of noise for bipolar op amps, explains why CMOS or Bifet designs suffer from relatively poor distortion compared to bipolar. The TLE2037 has a typical open loop gain of 153 dB (45 million!) and so distortion is significantly reduced. Slew rate is another crucial factor in low distortion circuits as at high frequencies and high gains an op amp may not be capable of operating without clipping or distorting the output signal.

The second graph, examines how a load affects an op amps distortion. The impedance used in these measurements is 600Ω and it shows that the OP-37 device is really not suited for applications with loads as heavy as this. What the graph does highlight is the outstanding performance the TLE2037, it has significantly better distortion than its competitor, the OP-37 and also outshines the NE5534.

The TLE2037 is therefore an ideal op amp in applications driving high impedance nodes and can be used for driving cables as well as multiple paralleled loads. The overall low distortion of this part also makes it particularly useful in audio applications including microphone pre-amps, filters and equalisation circuits.

5.14. TLE2037 High Performance Pre-Amp

A system requiring the ultimate in ac performance is audio Hi-fi. CD players, with a dynamic range exceeding 90 dB, are pushing the performance of amplifiers to new levels.

Phonographic recording/replay is still the standard for many good Hi-fi and they require the ultimate in high performance amplifiers. The TLE2037 with an open-loop gain of 153 dB, an offset of 25 µV and an 80 MHz gain-bandwidth product of 76 MHz is an excellent choice in audio applications. The low distortion and excellent output saturation recovery, discussed earlier, endorse the TLE2037s audio capabilities.

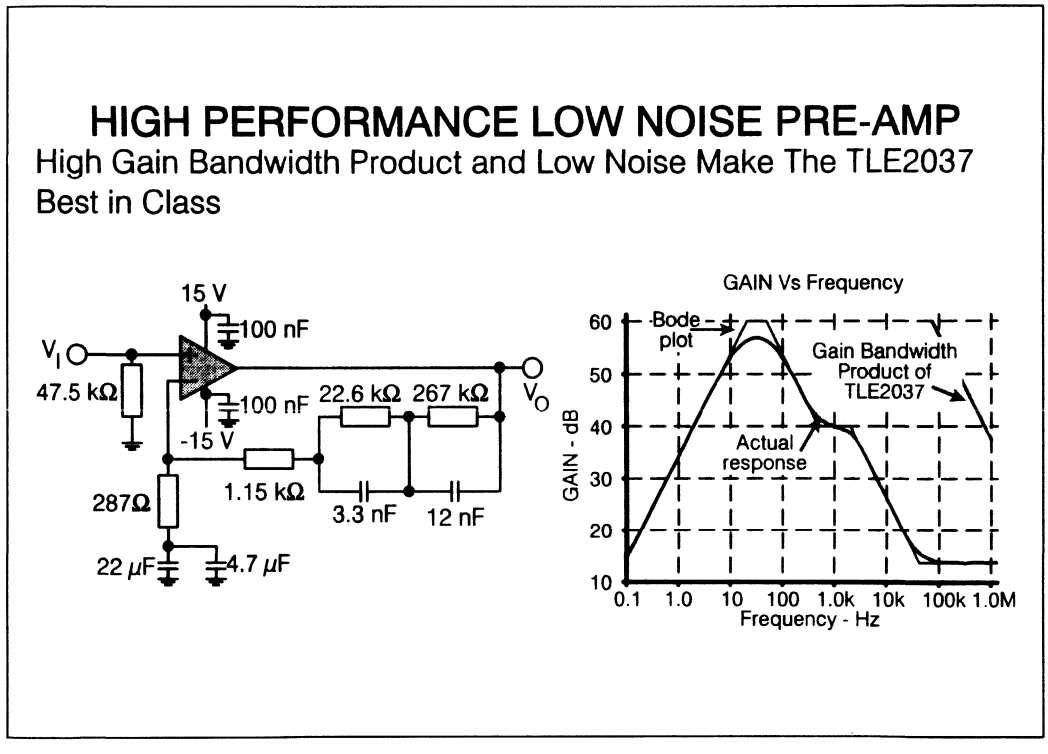


Figure 1.35 TLE2027/37 Application

Record equalisation circuits illustrate the importance of high gain and wide bandwidth in an ac application. The RIAA specification defines the characteristic of the phono replay pre-amplifier, and takes into account the frequency response of magnetic pick-ups. The pre-amp must match and cancel out the pick-up's response. The result is roll-offs at 50 Hz and 2120 Hz with a zero at 500 Hz. The circuit incorporates a low frequency pole and a corresponding zero at 20 Hz to remove rumble and low frequency effects.

For a gain of 1000, the op amp needs a large gain-bandwidth product to remove any gain error. The chosen op amp, TLE2037, has a loop-gain in excess of 40 dB at 20 kHz. Equally as important to low distortion is the device's 100 kHz full power bandwidth.

To achieve these levels the op amp has been decompensated. This means, as described in section 3.7 of signal conditioning, that the compensation capacitor has been reduced to allow faster slew rates and higher bandwidth. However the decompensated op amp should only be used with closed loop gains of greater than 5, preserving the Aβ phase margin. Therefore the high frequency gain of the circuit has been designed to flatten out with a gain of 5. This is done by introducing a zero at 40 kHz.

The types of components used must also be considered. The circuit has been purposely configured so as not to require the use of noisy, low performance electrolytic capacitors.

Polypropylene capacitors with their very low tan d give very good performance and have been used throughout, except for the lowest frequency zero where a polycarbonate capacitor has been used.

The resistors used are all metal film, giving high precision and low flicker noise. They are readily available in E96 series values and hence provide a cheap and accurate solution to the pre-amp's requirements.

5.15. High Precision Op Amp

As with any design, the input stage will have a significant effect on the overall performance of the system, particularly noise levels, DC accuracy and AC accuracy. One configuration which needs maximum performance is the instrumentation or difference amplifier, typically used in applications that require the ability to pick-out small differential voltages which are super-imposed on large common-mode signals. One op amp ideal for such applications is the **TLE2027A**.

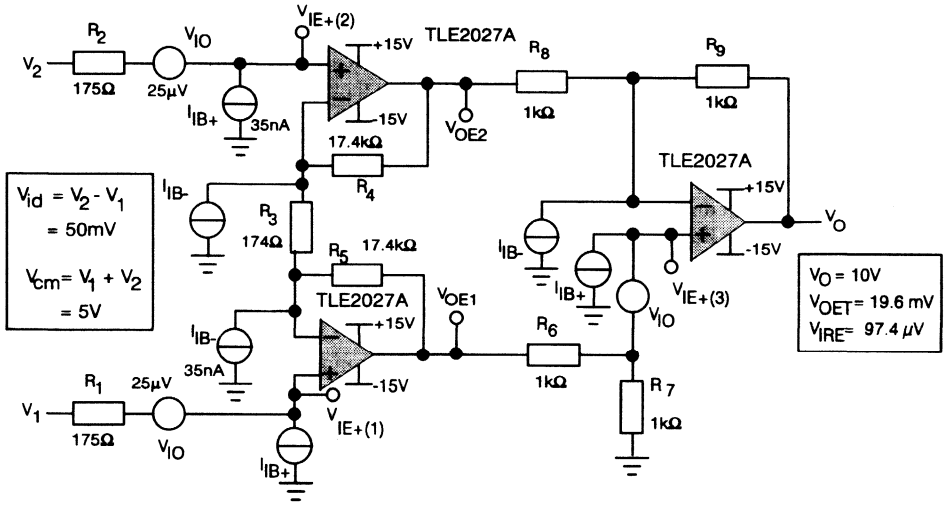
The ideal instrumentation amplifier has infinite input impedance, large differential voltage gain and zero common-mode gain. The most simple instrumentation amplifier consists of a single amplifier configured as amplifier A3 above. This has major drawbacks in:-

1) The input impedance is not infinite, but is equal to the sum of R_6 and R_7 on the non-inverting input and varies with differential input voltage on the inverting input.

2) The common-mode gain depends largely on the matching of resistors R_6 and R_7 to R_8 and R_9.

These problems can be overcome by the configuration shown below. Amplifiers A1 and A2 provide high differential gain, and unity common-mode gain. Another advantage is that the input impedance of the instrumentation amplifier is now the input impedance of the amplifiers.

The choice of amplifier will now have the largest effect on the total performance of the system, and for optimum performance errors associated with each amplifier will need to be reduced. Op amps are always used in a feedback loop and due to their finite open-loop gain and finite gain-bandwidth product, errors will be introduced. The feedback will reduce some of these problems and using a high performance op-amp will set most problems at a much lower level than others.



High Precision Op Amp

5.15.1. Op amp considerations.

One consideration is **input impedance**, which is the input impedance of the op-amp multiplied by its desensitising factor 1+Aβ; An op-amp with a large open loop gain will increase the input impedance to the order of $10^{12}\Omega$. This means that the **bias currents** are a much more important problem, especially when considering performance over temperature. The TLE2027 implements bias current cancellation techniques, resulting in the op-amp having low bias currents coupled with high speed and large open-loop gain.

Common-mode and **power supply** effects are another source of error and should not be neglected. The op amps will normally be looking at very small differential signals superimposed on large common-mode signals, which means that to preserve performance and accuracy the op amp needs to have a large common-mode rejection ratio. The TLE2027 has a typical CMRR of 131 dB, which is equal to 282 nV/V, and a PSRR of 144 dB equivalent to 63 nV/V.

The **gain error** due to the op-amp can introduce further system performance limitations, especially when operating at the high gains demanded by instrumentation amplifiers. The TLE2027 has an open loop gain of 45 million! - hence with a gain of 1000 the gain error is still only 0.0022%.

Drift of the op amp's offset voltage can limit the overall accuracy of the system, in particular with time and temperature, as this is one parameter which cannot be corrected or nulled out. The effects of both these are normally technology dependent, and as already discussed the excalibur process provides stability in both domains. The TLE2027A has a typical temperature co-efficient of input offset voltage, α_{VIO}, of 200 nV/°C. When considering the drift with temperature there are two aspects to take into account, the most obvious being the change in ambient temperature. The other is due to changes in junction temperature caused by self heating of the integrated circuit. The ultimate drift in offset voltage due to self heating will be package dependent due to differing thermal resistances.

Application errors

The configuration shown uses op amps A1 and A2 to provide a large differential gain (201) whilst providing a unity common mode gain. The errors associated with these op amps will be very similar.

The worst case values of CMRR and PSRR of the TLE2027 reduces errors associated with a common-mode voltage of 5 V and a 15 V supply (10% tolerance) to 16.5 µV. The quiescent supply current dissipates a power of 141 mW, this coupled with power dissipated in the output stages to drive the feedback and load resistors increases the offset voltages of A1 and A2 by 20.9 µV and 27.5 µV respectively. The cancellation circuitry for the bias currents reduces their related errors to 6.1 µV; while the open loop gain of the TLE2027 reduces any gain error to 252 nV (for a 50 mV differential input voltage).

Taking these into account the errors referred to the non-inverting input, V_{IE+}, is equal to:-

$$V_{IE+} = V_{IO1} + I_{IB+}*R_1 + \Delta T\alpha_{VIO} + V_{in1}* CMRR + 2V_{cc}*10\%*PSRR.$$

For A1 V_{IE+1} = 68.5 µV and for A2 V_{IE+2} = 75.1 µV.

The feedback network around each op amp ensures that the inverting input will be equal to the non-inverting input (the actual system input) plus or minus the errors, V_{IE+}, discussed above. This results in V_{IE+} also appearing as an input for the opposing op amp in the differential input pair. Therefore op amp A1 will multiply its offset errors by its normal non-inverting gain and it will also multiply the offset errors of A2 by its inverting gain, (the converse is true for A2). Op amp A3 with its differential gain will effectively result in the offset errors of A2 being multiplied by -201, and the offset errors of A1 multiplied by 201. The bias currents from the inverting input cause an offset voltage on the output of each amplifier equal to the bias current multiplied by the feedback resistor (R_5 or R_4), this can be referred to the input of the op amp by dividing by the non-inverting gain.

This results in the output of amplifier A1, V_{OE1}, being equal to:-

$$V_{OE1} = V_{IE+1} * \left(1 + \frac{R_5}{R_3}\right) - I_{IB-}*R_5 - V_{IE+2} * \left(\frac{R_5}{R_3}\right)$$

while the output of amplifier A2, V_{OE2}, will be:-

$$V_{OE2} = V_{IE+2} * \left(1 + \frac{R_4}{R_3}\right) - I_{IB-}*R_4 - V_{IE+2} * \left(\frac{R_4}{R_3}\right)$$

These equations ignore the very small gain error of the TLE2027. The inverting input bias current error, $I_{IB-}*R_5$, equals 609 µV.

Op amp A3 should remove the common-mode signal still present on the outputs of A1 and A2. It will also introduce similar errors to A1 and A2 except that the bias current error will be greater due to the larger source resistors. Assuming true matching between resistors R_6, R_7, R_8 and R_9, the bias current error will be reduced to the offset current error. When using op amps with bias current cancellation techniques the benefits of matching source resistances are reduced and will actually reduce the performance for low noise applications. The input stage has special circuitry, using matched transistors, to provide the bias currents for the differential input transistors.

The errors introduced by junction temperature will also be different; the output of A3 will be approximately 10 V while its inputs should be about 5 V, resulting in its output sourcing 5 mA which dissipates a further 25 mW within its output. This extra power dissipation coupled with quiescent power will cause a drift of 21 µV. Taking this drift and the offset current error of 15 µV, 30 nA x 500 Ω, into account the error introduced by A3 will be 77.5 µV; the non-inverting gain of A3 doubles this to yield 155 µV, which in this configuration is negligible.

The non-inverting errors due to A1 and A2 are multiplied by 201. This results in an error due to A1 of

$$201 \times 68.5\ \mu V - 609\ \mu V = 3.16\ mV.$$

and an error due to A2 of:-

$$201 \times 75.1\ \mu V - 609\ \mu V = 14.49\ mV.$$

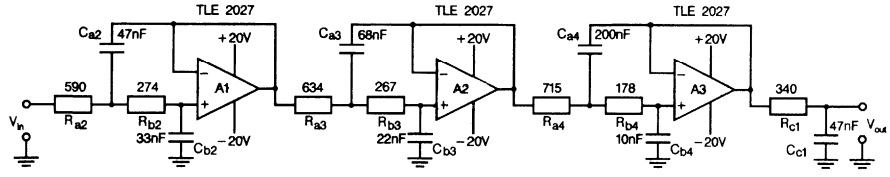
Due to the structure of the circuit the errors of A1 and A2 would normally subtract, but as these errors are related to separate integrated circuits they will tend to be uncorrelated, dual precision op amp would have most of these errors subtracted from each other. A way of minimising the probable overall error is to take a RMS sum of these errors. If this is done the error achieved is 19.6 mV. Relating this error to the input of the instrumentation amplifier results in an offset error of only 97.4 µV.

The large common-mode signal has increased the errors due to the op amps' finite common mode rejection ratio, and such a large common-mode signal applied to the third amplifier could add further errors caused by mismatching between resistors R_6 to R_9. Replacing R_7 with a trimming variable resistor allows for any further error adjustment.

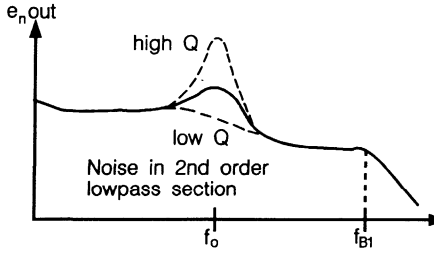
5.16. Wide Dynamic Range Lowpass Filter

5.16.1. Low Noise Active Filter Design

The maximum signal-to-noise-ratio or dynamic range of an active filter is determined through its output noise spectral density and the rms noise voltage. The noise performance of each filter can be analysed by taking the sum of the squares of the individual noise sources and calculating their impact on the output voltage. This calculation is often complex as many noise sources are involved.



10kHz, 7TH ORDER BUTTERWORTH LOWPASS FILTER



Noise approximation of
2nd order sections:

- DC to f_o : (low Q)
  e_n^2 out $\simeq 4kT[R_a + R_b + r_n + g_n(R_a + R_b)^2]f_o K^2$
- f_o to f_{B1} :
  e_n^2 out $\simeq 2\pi kTr_n(f_{B1} - f_o)K^2$

Wide Dynamic Range Lowpass Filter

If an active filter is required with a wide dynamic range, the fundamental design considerations below must be followed:

- The dynamic range increases with extended supply rails. The Excalibur TLE2027 is capable of operation from ±22 V supplies providing an output swing in excess of ±19 V with a 2 kΩ load.
- To benefit from the low input noise voltage performance of the chosen op amp, the noise from its source impedance should be less than the noise it generates itself. TLE2027's input noise voltage is equivalent to the thermal noise from a 380 Ω resistor.
- The input noise current of the op amp multiplied by the impedance it is flowing through should be less than the thermal noise from the source impedance and less than the op amp's input noise voltage. With network impedances below 20 kΩ seen by the input noise current sources, noise current is not likely to dominate a TLE2027 application.
- The impedance level of the passive network should be kept low enough to prevent the thermal noise it exhibits to exceed the noise contribution from the op amp.
- In higher order filters, the individual filter sections can be placed in an order to minimise noise by having the highest Q sections first, but this limits the filter's maximum input swing and affects the

top of the dynamic range. A compromise should be made to ensure that all sections utilise the maximum dynamic range of the op amp.

Current flowing in resistors produce excess noise in addition to the thermal noise due to inhomogeneity in the resistor material. Metal film type resistors produce less noise than carbon film resistors and should hence be employed. In addition, larger sized resistors are less noisier than smaller ones.

- Sensitivity of large capacitors to mechanical vibrations, microphonics or hum pick-up can be a problem although large capacitors are normally associated with low impedance levels. Dividing a large capacitor up in two makes it possible to cancel picked up hum by ensuring that magnetic fields passed through the two capacitors in opposite direction.
- Thermo-electrical voltage changes caused by rapid temperature variations across joints of dissimilar materials increase low frequency noise. The solution is to reduce air flow across the circuit.
- In low frequency designs, the op amp's flicker or 1/f noise must of course be considered. TLE2027 has a very low 1/f corner adding insignificant noise to filter designs above 100 Hz.
- Use non-inverting op amp filter configurations in low gain applications, as their noise is less. In a unity gain configuration, an inverting amplifier produces twice as much output noise as a non-inverting amplifier.

Often, a compromise between several diverting requirements has to be made. One example is the necessity for a general low impedance level, which of course has to be considered together with the chosen op amp's drive capability.

5.16.2. 2nd Order Lowpass Filter Section

To realise a higher order lowpass low noise filter, a standard Sallen and Key 2nd order filter block was chosen. Cascade coupling of three sections are used to implement the total filter shown. The chosen 2nd order block can be designed to provide excellent noise performance but exhibits relative high Q factor sensitivity to the op amp's gain accuracy. However, as long as a unity gain or follower op amp configuration is used, the gain can be made very accurate without the need for precision resistors. A further limitation is that the open loop gain left in the op amp at the highest frequency, f_O, of interest must be high enough to implement the necessary Q factor accurately. A guideline for the op amp's required unity gain bandwidth, $B1 > 300 * Q * f_O$.

By applying the fact that the sum of the current flowing into the junction between the two input series resistors and the feedback capacitor must be zero, the transfer function for the individual 2nd order lowpass filter section can be shown to be given by:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_a R_b C_a C_b}}{s^2 + \left(\frac{1}{R_a C_a} + \frac{1}{R_b C_a}\right)s + \frac{1}{R_a R_b C_a C_b}} = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (1)$$

From this it follows that:

$$\omega_o = \sqrt{\frac{1}{R_a R_b C_a C_b}}; \quad \text{and} \quad \frac{1}{Q} = \sqrt{\frac{R_b C_b}{R_a C_a}} + \sqrt{\frac{R_a C_b}{R_b C_a}}; \quad (2)$$

Design Procedure

Given ω_o and Q for the filter, the design steps can now be derived as follows:

1. Choose C_a
2. Choose $C_b = k * C_a$; where k = ratio between any two capacitors in a standard series, like E6, E12 or E24. A restriction for k that allows a solution of the resistor design equations is given by:

$$k < \frac{1}{4Q^2};$$

3. Calculate R_a from: $$R_a = \frac{1}{2 C_a \omega_o} \frac{1}{k Q}\left(1 \pm \sqrt{1 - 4 k Q^2}\right);$$

4. Calculate R_b from: $$R_b = \frac{1}{R_a k C_a^2 \omega_o^2};$$

Note that the values of R_a and R_b can be swapped.

Sensitivity

The sensitivity of Q and ω_o with respect to the filter parameter, x, is defined as:

$$S_x^Q = \frac{d(\ln Q)}{d(\ln x)} = \frac{x}{Q}\frac{dQ}{dx}; \quad \text{and} \quad S_x^{\omega_o} = \frac{d(\ln \omega_o)}{d(\ln x)} = \frac{x}{\omega_o}\frac{d\omega_o}{dx}; \quad (3)$$

Thus, S_x^Q gives the incremental change in Q due to an incremental change in x. For example if S_x^Q is equal to 0.5, then it implies that a 2% change in x will cause a 1% change in Q. For the given 2nd order block, the following sensitivities can be found by applying equation (3) on (2):

$$S_{R_a}^{\omega_o} = S_{R_b}^{\omega_o} = S_{C_a}^{\omega_o} = S_{C_b}^{\omega_o} = -\frac{1}{2};$$

$$S_{A_1}^{\omega_o} = 0 ; \text{ where } A_1 \text{ is the unity gain accuracy of the op amp.}$$

$$S_{R_a}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o R_a C_a};$$

$$S_{R_b}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o R_b C_a};$$

$$S_{C_a}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o C_a}\left(\frac{1}{R_a} + \frac{1}{R_b}\right);$$

$$S_{C_b}^{Q} = -\frac{1}{2};$$

$$S_{A_1}^{Q} = \frac{Q}{\omega_o R_b C_b};$$

5.16.3. Why Use the TLE2027

The High performance Excalibur op amp TLE2027 is well suited for low noise active filter applications because of its low noise voltage of 2.5 $nV/\sqrt{Hz}$ combined with its wide unity gain bandwidth of 15 MHz. In addition, TLE2027's good output drive capability and low distortion allow for a low impedance passive network to be used, which in turn exhibits less thermal noise. In applications where a wide dynamic range is required, the TLE2027 offers operation from ±22V supplies. Particularly, in lowpass filter design as the one shown, it is possible to maintain excellent DC accuracy thanks to the Excalibur op amp's extreme low and stable offset voltage. Selections down to 25 µç max. are available.

Low Noise Design Considerations

The noise of a 2nd order section can be analysed directly from the formula:

$$e^2_{n\,out} = \int_{-\infty}^{+\infty} \left(\sum_{j=1}^{k} \left\{ |T_{i,j}(j\omega)|^2 \, i^2_{j,n}(\omega) \right\} + \sum_{i=1}^{m} \left\{ |T_{e,i}(j\omega)|^2 \, e^2_{i,n}(\omega) \right\} \right) d\omega \qquad (4)$$

Where $T_i(j\omega)$ and $T_e(j\omega)$ are transfer functions from noise current and noise voltage generators having efficiency i and e respectively. The noise sources are easy to identify; however the transfer functions for the noise sources are more cumbersome. The real difficulties start when we want to integrate the noise over frequency to determine the total output noise. Computer calculations using Macro models that include noise for the op amp and added thermal noise sources for the resistors can give fairly accurate results. However, they don't allow for direct analysis of the contribution from the individual noise sources and circuit optimisation.

As long as we are discussing low noise lowpass filter design with low Q values, the analysis can be simplified by dividing the noise up into two frequency areas; below and above the filter's cut-off frequency, f_o. Assuming low Q factors, it can be shown from (4), that the noise density in the low frequency passband is constant and that the noise in the high frequency stopband is coming mainly from the op amp's noise voltage frequency limited by the op amp's unity gain bandwidth or the succeeding filter roll off. The approximated total rms noise voltage at the output of the 2nd order block takes then the form:

$$\boxed{e^2_{n\,out} \cong 4\,k\,T\,(R_a + R_b + r_n + g_n\,(R_a + R_b)^2)\,f_o\,K^2 + 2\pi\,k\,T\,r_n\,K^2\,(f' - f_o)}\;; \qquad (5)$$

Where $r_n = \dfrac{e^2_n}{4\,k\,T}$; ($e_n$, is the input voltage noise associated with the opamp used).

and $g_n = \dfrac{i^2_n}{4\,k\,T}$; ($i_n$, is the input current noise associated with the opamp used).

$k = 1.38 * 10^{-23}$ J/K ; (Boltzmann's constant).

T = Absolute temperature in Kelvin ; (298 @ 25°C).

f_0 = Lowpass filter's cut-off frequency.

f' = Unity gain bandwidth, B1, of the used op amp.

K = Filter gain.

The first term of formula (5) can be interpreted as broadband noise in the passband of the filter $0 < f < f_0$, while the second as a broadband noise in the stopband $f_0 < f < f' * \pi/2$; assuming a first order roll-off noise bandwidth. Note that the stopband noise is determined by the op amp's input and that flicker noise is not included. Evaluating the noise using (5) makes it easy to compare the individual sources contribution to the total noise.

7th Order 10 kHz Lowpass Butterworth Filter Design

For the shown lowpass filter a Butterworth approximation was chosen. This provides an accurate DC gain, which is often important in lowpass filter applications, where high DC performance is required. The impedance level of each passive network was chosen as low as possible to reduce thermal noise but simultaneously kept at a level where the op amp was capable of driving it.

Butterworth Filter Parameter Values

The composite 7th order 10 kHz lowpass filter can be realised using three second order lowpass filter blocks and one 1st order simple RC network in a cascade coupled configuration. The Q factors and ω_0 values for the normalised filter stages are available from a Butterworth filter table:

Stage	Q Factor	ω_0	Gain at ω_0	Max Gain
1	A real pole	1	-3.00 dB	0 dB
2	0.554958	1	-5.20 dB	0 dB
3	0.801937	1	-1.97 dB	+0.22 dB
4	2.246979	1	+7.03 dB	+7.25 dB

Calculation of Component Values

From a noise point of view it was decided to place the passive RC section, stage 1, last. This slightly limits the input swing and the top of dynamic range due to overshoot in stage 4, but significantly reduces the stopband noise. A disadvantage from this structure is the relatively high output impedance of the filter. However, if the filter is interfaced to the high impedance input of an A/D converter this should not present any problem. The order of the filter sections realised with the previous described 2nd order lowpass Sallen and Key building blocks becomes now:

Realised Stage Order: 2, 3, 4, 1

Table Stage Order: 1, 2, 3, 4

By using the design procedure for the second order blocks and performing the frequency transformation from the normalised $\omega_0 = 1$ to $\omega_0 = 2\pi * 10$ kHz, follows:

Stage	C_a	C_b	R_a	R_b

2	47 nF	33 nF	Ideal: 594.2Ω E96 std. value: 590Ω	Ideal: 274.9Ω E96 std. value: 274Ω
3	68 nF	22 nF	Ideal: 635.8Ω E96 std. value: 634Ω	Ideal: 266.3Ω E96 std. value: 267Ω
4	200 nF	10 nF	Ideal: 708.3Ω E96 std. value: 715Ω	Ideal: 178.8Ω E96 std. value: 178Ω

The last stage in the cascade realisation is a first order pole formed by C_{c1} and R_{c1} to yield a 10 kHz lowpass filter.

Design procedure: Chose C_c and calculate R_c from, $R_{c1} = 1/(2\pi * 10\ kHz * C_{c1})$. The final values are given in the table below:

Stage	C_{c1}	R_{c1}
1	47 nF	Ideal: 338.6Ω E96 std. value: 340Ω

Sensitivities of Implemented Filter

From the previous discussed sensitivity equations, the sensitivity with respect to Q an ω_o for all stages was found as follows:

Stage	$S^{\omega_o}_{R_a}$	$S^{\omega_o}_{R_b}$	$S^{\omega_o}_{C_a}$	$S^{\omega_o}_{C_b}$	$S^{\omega_o}_{R_c}$	$S^{\omega_o}_{C_c}$	$S^{\omega_o}_{A_1}$	$S^{Q}_{R_a}$	$S^{Q}_{R_b}$	$S^{Q}_{C_a}$	$S^{Q}_{C_b}$	$S^{Q}_{A_1}$
2	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.2	0.5	-0.5	1.0
3	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.2	0.5	-0.5	2.2
4	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.5	0.8	-0.5	20.0
1					-1	-1						

Note the high Q sensitivity with respect to the op amp's unity gain accuracy in stage 4. The TLE2027's open loop gain of more than 60 dB or 1000 at 10 kHz, when loaded with the low impedance feedback network, gives however only a Q error of $20 * 0.1\ \% = 2\%$.

5.16.4. Noise Evaluation of Total Lowpass Filter

The equivalent noise resistance, r_n, of the TLE2027's typical input noise voltage, e_n, is given by:

$$r_n = \frac{e_n^2}{4\,k\,T} \cong 380\Omega\,;$$

The equivalent noise conductance, g_n, of the TLE2027's typical input noise current, i_n, is given by:

$$g_n = \frac{i_n^2}{4\,k\,T} \cong 9.7\mu\text{Siemens}\,;$$

Analysis of the noise current impact on the total output noise shows that it can be ignored with the chosen impedance level, hence it is left out of the calculations. Applying equation (5) on the individual 2nd order filter sections lead to a good approximation for the noise of the total 7th order Butterworth lowpass filter.

Stage 2. Ignoring contribution form g_n and assuming the stopband noise is completely removed by the succeeding filter stages, this section's contribution to the total output noise is given by:

$$e^2_{n\,out2} \cong 4kT\,(\,590 + 274 + 380\,)\,10 * 10^3 = 0.205 * 10^{-12}\ V^2\,;$$

Stage 3. Ignoring contribution from g_n and assuming that stopband noise is rolled off by 3rd order corresponding to a noise bandwidth of, $f_o * 1.05$, this sections contribution to the total output noise is given by:

$$e^2_{n\,out3} \cong 4kT\,(634 + 267 + 380)\,10 * 10^3 + 4kT\,380\,(1.05 - 1.00)\,10 * 10^3\ V^2;$$

$$e^2_{n\,out3} \cong 0.213 * 10^{-12}\ V^2\,;$$

Stage 4. Ignoring contribution from g_n and assuming that stopband noise is rolled off by 1st order corresponding to a noise bandwidth of, $f_o * \pi/2$, this sections contribution to the total output noise is given by:

$$e^2_{n\,out4} \cong 4kT\,(\,715 + 178 + 380\,)\,10 * 10^3 + 4kT\,380\,(\,\frac{\pi}{2} - 1.00\,)\,10 * 10^3\ V^2;$$

$$e^2_{n\,out4} \cong 0.245 * 10^{-12}\ V^2\,;$$

Stage 1. The noise of this stage comes from the thermal noise of the resistor, R_{c1}, which is band limited with a 1st order roll off given by R_{c1} and C_{c1}, hence this sections contribution to the total output noise is given by:

$$e^2_{n\,out1} = 4kT\,r_n\,\frac{\pi}{2}\,f_o \cong 4kT\,380\,\frac{\pi}{2}\,10 * 10^3\ V^2 = 0.088 * 10^{-12}\ V^2\,;$$

The total output noise of the filter, E_n can now be calculated from:

$$E_{n\,tot} = \sqrt{\sum_{j=1}^{4} e_{n\,out\,j}^{2}} \cong \sqrt{0.205 + 0.213 + 0.245 + 0.088}\,\mu V = 0.867\mu V\ ;$$

In practice, a slightly higher noise level can be measured, as the simplified noise model don't hold for section 4 due to its relative high Q factor of approximately 2.25. This peak in section 4's transfer function results in increased noise around the filter's -3dB frequency. However, a total dynamic range in excess of 130 dB can be achieved for this 10 kHz, 7th order Butterworth lowpass filter.

6. High Temperature Op Amps

6.1. High Temperature Process

In a number of engineering sectors there is an increase direct transducer signal conditioning. This can subject the signal conditioner to the extremes in temperature, stress and pressures. Some of the largest problems to which op amps are subjected is elevated ambient temperature operation.

In automotive applications this can involve direct cylinder block mounting, while industrial applications may require the op amps to be mounted on the vessel containing the process. In the past this would have involved using expensive hybrid devices in ceramic packages.

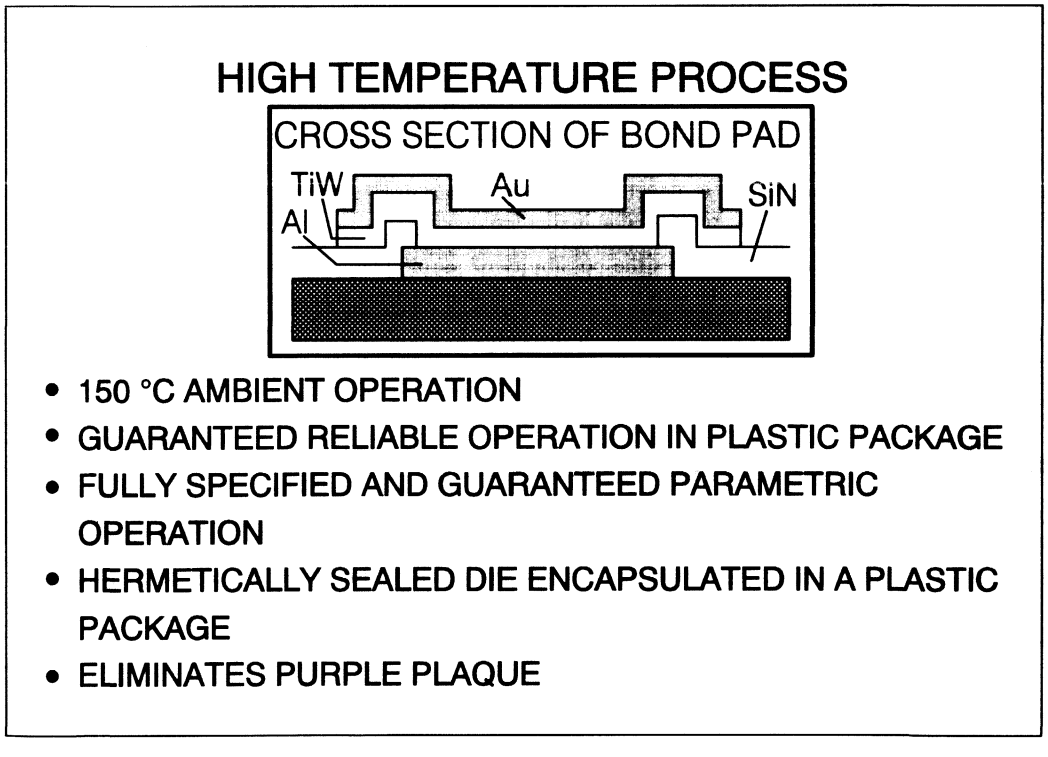


Figure 1.36 High Temperature Process

Plastic packages have for a long time suffered great reductions in reliability when subjected to high temperatures for great periods of time. This has been due to several factors of the package and bonding.

6.1.1. Integrated Circuit Process

An integrated circuit will normally have all the silicon covered with Silicon Nitride. This has two main functions, one is to protect the surface from external effects , while the other is to protect the die from moisture ingression. There must, however, be holes in the silicon nitride to enable the bond wire to connect the silicon to the outside world. These holes in the silicon nitride can now let moisture into the silicon.

Plastic packages will normally let much more moisture into the integrated circuit than ceramic packages. This has led to plastic packages being rarely used in harsh environments. Texas Instruments' high temperature process now enables hermetically sealed devices to be produced in a plastic package.

6.1.2. High Temperature Process

The metal used for a bond wire is gold, Au, while the bond pad is aluminium, Al. In order to seal the bondpad, an extra non corrosive metal layer is required. Due to its high conductivity and resistance to corrosion, gold would at first seem to be the best choice, gold does not adhere properly to aluminium. For higher reliability a different metal layer must be used between the gold and aluminium. The alloy chosen is Titanium Tungsten (TiW), and the bond pad is hermetically sealed.

Purple Plaque

A further advantage of the TiW layer is that it removes the possibility of Purple Plaque. When Aluminium comes into contact with gold, ie when the bond wire connects with a standard bond pad, a purple intermetallic compound is developed which is harmful to the device. This phemenon is independent of package, and is excelerated at higher temperatures.

The high temperature process removes the possibility of purple plaque occurring and therefore gives further reason for using the new designs in plastic rather than expensive ceramic packages.

With the development of this process Texas Instruments has now released two products, TL2828 and TL2829, that are fully functional and whose performance is fully specified and guaranteed up to an ambient temperature of 150°C

6.2. High Temp Process Qualification

ANy new product (and process) must go through a qualification process. This is to make sure that the device is reliably manufacturable. Due to the very harsh nature of the environment in which these products are to be used, and that it is a new process, the qualification procedure for the first op amp, TL2829, was very thorough - far in excess of any other linear design.

The table below shows the qualification procedure for the TL2829 op amp.

TEST	CONDITIONS
Steady State Life	155°C for 5000 hours with bias.
Autoclave	121°C for 2000 hours without bias at 15 psi and 100% humidity.
Temperature Cycle	-65°C to 150°C for 5000 cycles.
Storage	170°C for 3000 hours.

Steady State Life Test

Steady State Life Test is used to evaluate parameter drift over the lifetime of the product. 5000 hours at 155°C equates to 7 months of accelerated life test, which is more than an order of magnitude longer than for standard devices.

Autoclave

Autoclave is used to test the performance of the device in high moisture environments. The TL2829, with its encapsulated die, was designed for use in high humidity applications, and so was tested for much longer periods that standard palstic devices

Temperature Cycle

Temperature Cycling tests the manufacturability and reliability of a part, and particularly the quality of bonding. To test the device to its extremes the TL2829 was subjected to over 5000 cycles.

Storage

Storage is afurther measure of reliability of the device and package combination. Due to the TL2829's high temperature range it was subjected to higher ambient temperature tests for far longer periods than standard devices.

Throughout all these extended tests no failures occurred, which is impressive for any product, and highlights the outstanding reliability of Texas Instruments' high temperature op amps.

6.3. High Temperature Op-Amps

The TL2828 and TL2829 are the first in a series of very high temperature op amps from Texas Instruments. They are at present the only readily available standard monolithic integrated circuit operational amplifier capable of functioning at ambient temperatures of 150°C.

Texas Instruments now has another temperature range group, the smallest being the commercial temperauture range, denoted by C. The next range is industrial denoted by I which extends from -25°C (some devices operate from -40°C) to 85°C The military temperature range goes from -55°C to 125°C and is denoted by M. Most of Texas Instrument voltage regulators will have a special Q temperature range which specifies the operating junction temperature range instead of the ambient temperature range, this extends from -40°C to 125°C.

The TL2828 and TL2829 are the first devices to operate over the Z temperature range which goes from -40°C to 150°C..

Both devices are single supply op amps capable of operating from a 4 V supply up to a maximum of 30 V. The supply current of the TL2829 is only 1.2 mA at a 5 V supply over the whole temperature range for all four op amps.

The high density of op amps and low quiescent power adds to its capabilities of functioning at very high ambient temperatures.

HIGH TEMPERATURE OP AMPS

TL2828 and TL2829 HIGH TEMPERATURE RANGE OP AMPS

- Free-Air Operating Temperature Range
  -40°C to 150°C
- Low Input Offset Voltage
  7 mV (max) @ 25°C
  10 mV (max) over full range
- Wide Range of Supply Voltages :
  Single Supply . . . 4 V to 30 V
  Dual Supply

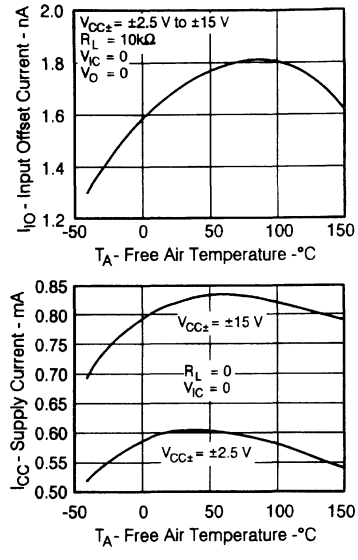


Figure 1.37 High Temperature Op-Amps

7. Summary

7.1. Device Macro-Models and Simulations

Since the introduction of operational amplifiers, very much simplified models of their behaviour have been used to try and predict the output of the device when stressed with various forms of inputs.

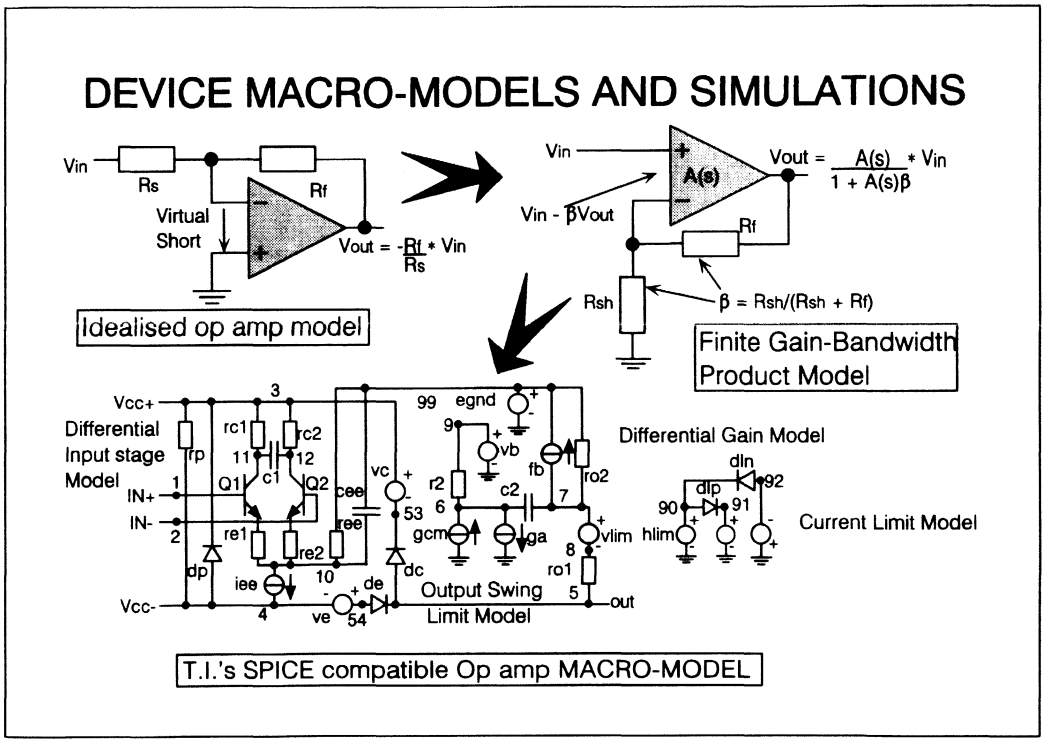


Figure 1.38 Device Macro-Models and Simulations

The simplest of models is that of the virtual short between the inputs of the device. This assumes that the gain is infinite and has infinite input impedance. This model works reasonably well with high performance op amps with their high open loop gains of more than one million. It proves unsatisfactory when trying to consider other aspects in the performance of the op amp, such examples are the errors associated with its input and more importantly the device's frequency response.

For DC. applications the high input impedance is normally a very good assumption, almost all op amps have impedances greater than 1 MΩ and the gains frequently used, are low enough that the op amp is not used in open loop conditions. Taking into consideration all the offset voltages and input bias and offset currents adds to the complications of the simplified model. Hence a more complete model has the virtual short across the inputs replaced with an offset voltage in series with the non-inverting input with biasing current sources connected to the inputs of the device. These are all DC. effects, and can reflect the performance of the op amp reasonably well, but modelling most of the ac. aspects of the op amp can be very difficult.

The op amp can be considered as operating as a low pass filter with enormous gain, the large gain minimises most of the low pass filter effects at low frequencies, but at higher frequencies these effects must be taken into account. The analysis can be made easier by use of the Bode plot, and relating the circuit's ideal gain to the op amp's actual gain. This will show the point where the open loop gain of the op amp takes over from the ideal gain.

The whole model can be improved by considering the feedback equation of any system:-

$$G_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

Where G_{CL} is the closed loop gain, A_{OL} is the open loop gain and β is the feedback around the amplifier. Using this equation increases the accuracy of the model considerably but can also increase the complexity to beyond that of pen, paper and calculator, especially for systems using several op amps. The difficulty of ac. analysis is compounded by operating the op amp with large signals, which can drive the device out of its assumed linear mode.

With the advent of modern day computers a much simpler way of analysing op amp circuits has arrived: Macro-models of the op amps. The macro-model is a simplified model of the op amp taking into account all of its key parameters. Texas Instruments has released macro-models of all its op amps and these are capable of operating with a wide variety of simulation packages, one example is Microsim's PSPICE™.

The macro-model is a derivative from Boyle's model, which uses real transistors to model the actual input stage of the op amp. The following stages via the input stage model the gain and its roll-off over frequency, along with bias current errors and further ac and dc limitations. Each of the parameters are derived from the specifications of the op amp and so simulate the performance of op amp to a much higher level of accuracy than the designer with only a pen and paper can. The macro-models, as with most things, provide a compromise between optimum performance with simulating speed, cost and ease of use. A full model of the device will give a better representation of the device but would take much longer to simulate and would also cost considerably more.

Plus another thing to consider is than no op amp manufacturer releases full spice simulation models of their devices, however, Texas Instruments has now released a Macro-Model Data Manual. This contains a Macro-Model for each of its op amps, except for the latest products which contain the model within their datasheets.

7.2. Texas Instruments' Signal Conditioning

In today's seminar most of Texas Instruments' newest and most exciting voltage regulators and op amps have been discussed. These products have been designed with you the customer in mind. It is only by

gaining and using **Market Understanding** that Texas Instruments will be able to develop the uA741s and OP-07s of the future.

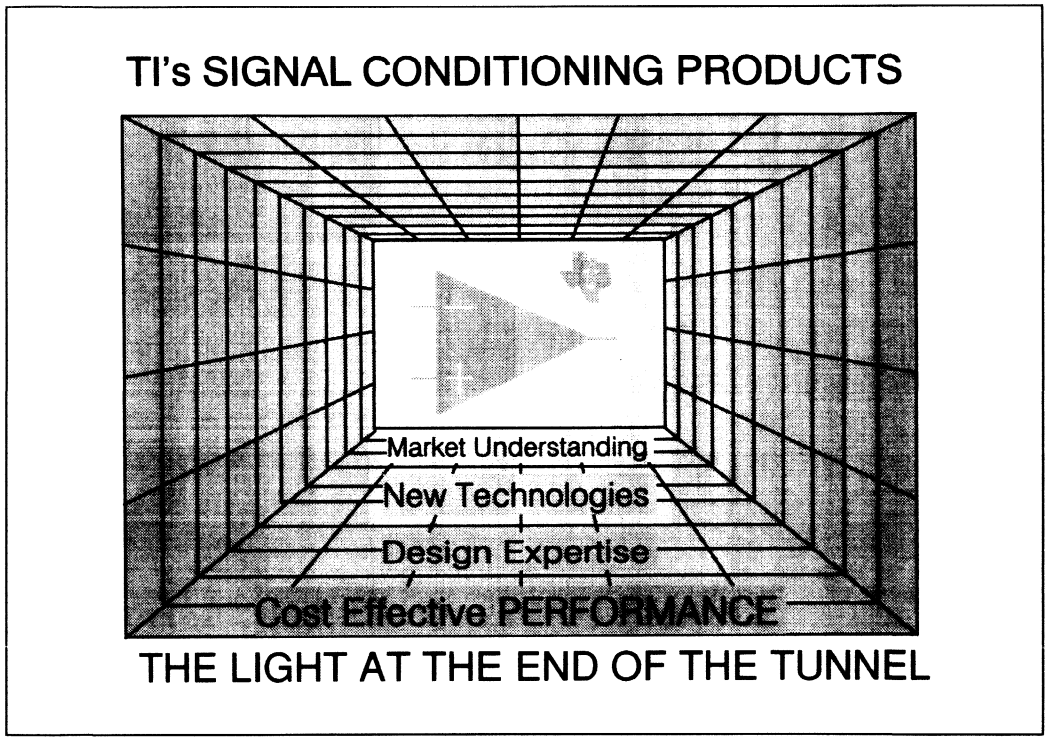


Figure 1.39 Texas Instruments' Signal Conditioning

In hand with this market understanding Texas Instruments is developing **new** and improving on existing **technologies**. This is further helping Texas Instruments develop high performance products for today's and tomorrow's markets.

The **design expertise** built-up in developing the new technologies, also helps in producing the high performance products that is required by today's system.

All these 3 things when coupled to Texas Instruments' enormous semiconductor manufacturing base helps it to provide high performance products at a cost effective price, and should help Texas Instruments become the light at the end of the tunnel of your system requirements.

Section 2
Data Conversion

Section Contributions by:

Dave Cox

Simon Ramsdale

Tim Ardley

Contents

1. Introduction

Data acquisition is the process of transforming signals from the "real" analog world into the digital domain for storage, display, processing, data transmission or control. A data acquisition system is an electronic system used to perform this task and comprises sensors, transducers, signal conditioning, sample and hold circuits, analog multiplexers, and analog to digital converters (ADC). Recovery of a digital signal into analog form is sometimes required. The components, such as digital to analog converters (DAC) and filters, used to perform this function are also covered under the heading of data conversion.

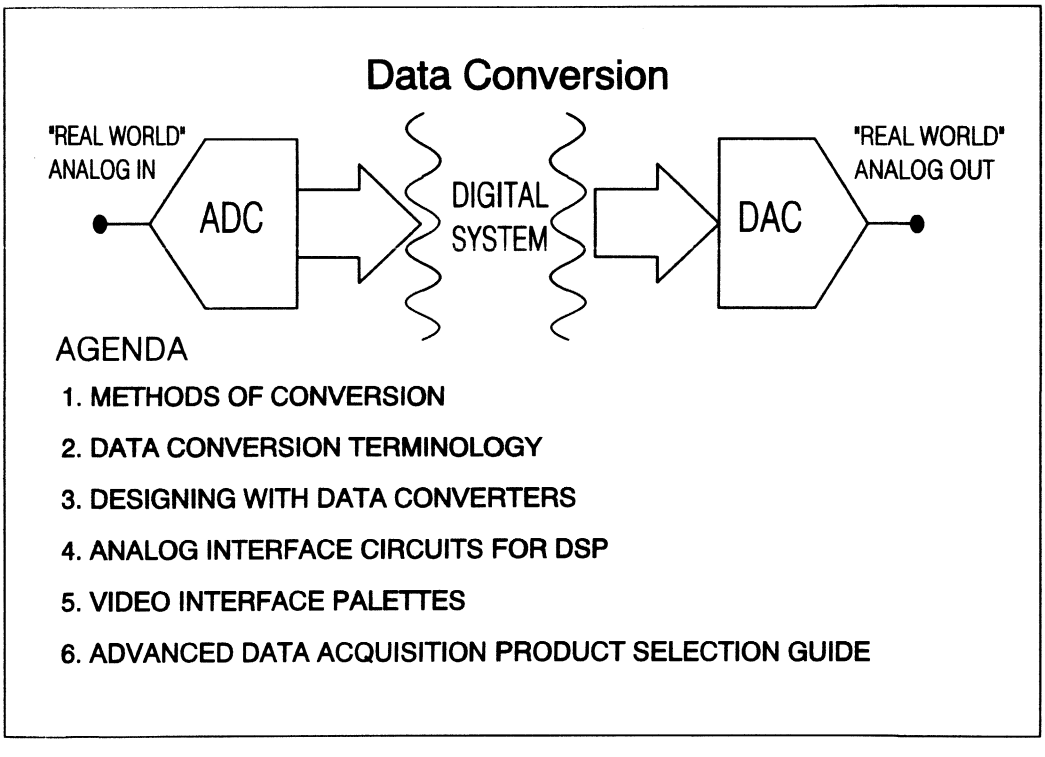


Figure 2.1 - Data Conversion

2. Methods of conversion

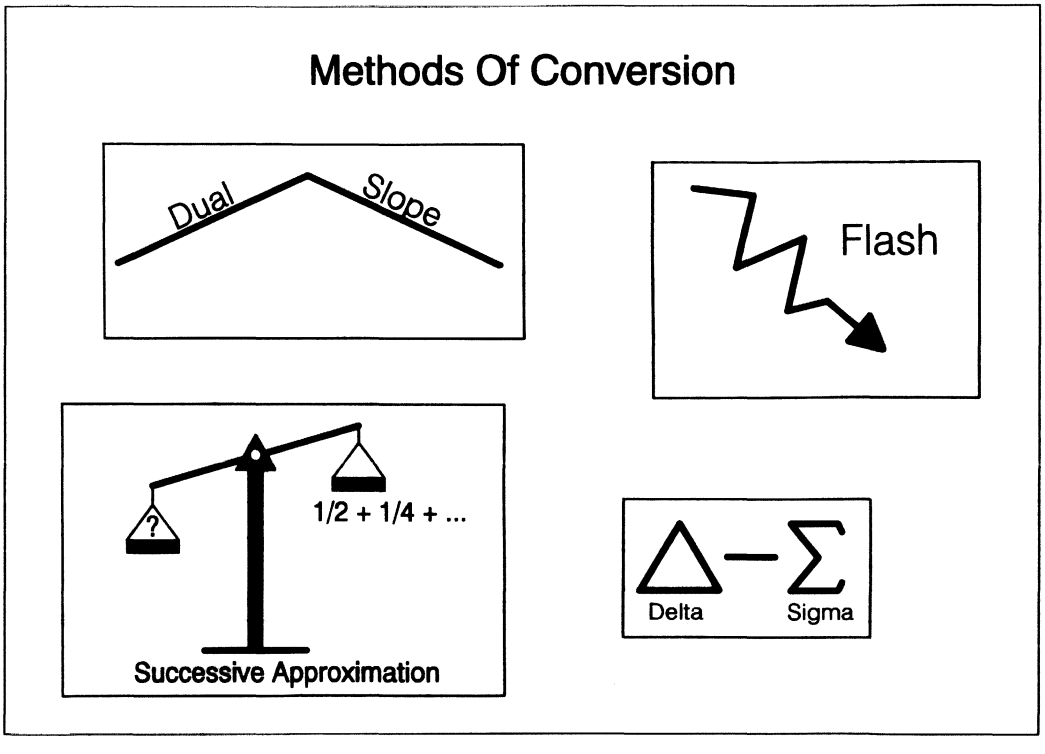


Figure 2.2 - Methods of Conversion

This first section looks at the methods used to "translate" between the analog and the digital worlds. It explains the advantages and disadvantages of each type, and what makes it the appropriate choice for a particular application.

Applications for data acquisition systems cover a wide range; from weighscales, speech and audio processing to instrumentation and video recorders. Each application has its own requirements but two common parameters must be considered in all systems. These are bits of resolution, and conversion time. To meet these diverse needs , different conversion methods are employed. Some are optimised for speed of conversion, while others are known for their higher resolution. Six common techniques for analog to digital (A/D) conversion are as follows:

- **Single Slope**
- **Dual Slope**
- **Successive Approximation**
- **Semi-Flash**
- **Flash**
- **Oversampling (Delta-Sigma)**

Conversion methods for digital to analog (D/A) signal recovery also vary with the speed and resolution requirements. In the following examples, some of the common conversion techniques will be discussed and related to typical applications.

2.1. Dual slope principle

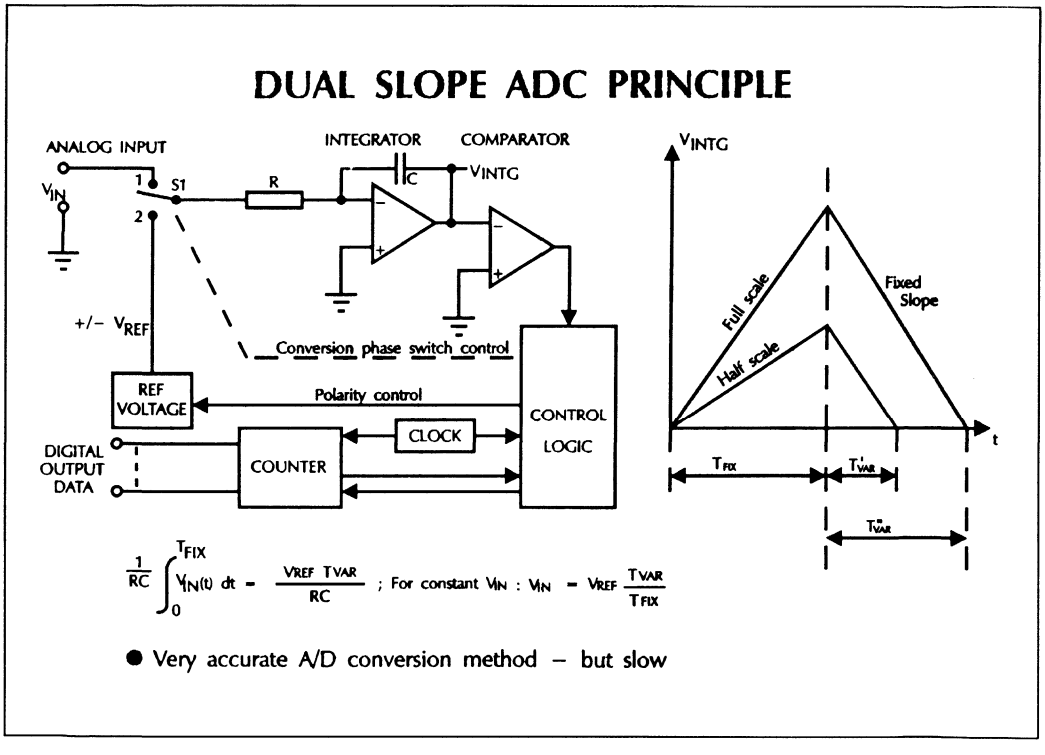


Figure 2.3 - Dual slope principle

The most simple A/D conversion method is the single-Slope technique, which arrives at its digital output by comparing the unknown analog input signal with a ramp voltage. A digital value is obtained by counting the number of clock pulses needed to build a ramp from 0V to the value of the unknown analog input signal. The requirements for a good single slope converter are a stable reference voltage,

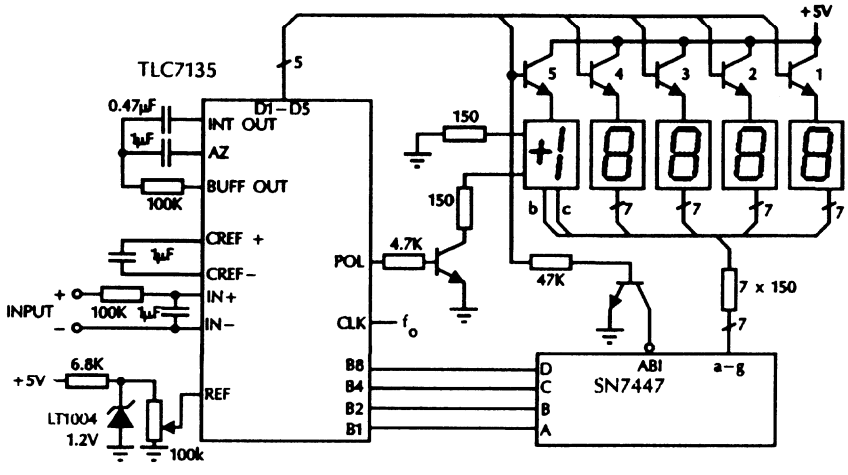
clock, ramp generator and low offset comparator. Integrated implementations are usually low to medium accuracy. This technique however has a long conversion time .

Dual Slope conversion is also slow but very accurate. The method uses a counter and an integrator to convert an unknown analog input voltage into a ratio of time periods multiplied by a reference voltage. A first period of time, TFIX, and uses an unknown analog voltage, VIN as input. At the end of the peak value proportional to the input voltage is held on the integrator output. S1 is then switched to position 2 and a second voltage, VREF of opposite polarity , which is used as the input to the amps down at a rate only dependent on the reference value. The resultant value of the first period is integrated down to 0V in a variable time, TVAR proportional to the amplitude of the input signal, VIN. Putting these two ramps together, using the same clock to count time periods TFIX and TVAR, the unknown input voltage VIN can be determined from:

$$V_{IN} = V_{REF} \times (T_{VAR} / T_{FIX})$$

Using the same integrating network cancels errors due to comparator offset, capacitor tolerances, long term counter clock drift and integrator nonlinearities. While the conversion speed of a dual slope converter is slow (milliseconds), high resolution (10-16 bits) is possible. Resolution is determined from the ratio of counts in the integration periods. For example 1 in 20,000 counts is equivalent to better than 14 bits of resolution, with the basic error as +/-1 count plus the reference voltage error.

2.1.1. A 4 1/2 Digit panel meter using TLC7135



- Multiplexed common anode LED display
- Conversion rate : 2.5 conv/sec for f_o = 100kHz

Figure 2.4 - A 4 1/2 Digit panel meter using TLC7135

Dual slope converters such as the LinCMOS(TM) TLC7135 are ideally suited to any application which requires precise measurement of slowly varying analog signals. The TLC7135 offers resolution of 50 ppm (one part in 20,000) making it an excellent choice for applications such as digital voltmeters, precision panel meters, weigh-scales and for precise or wide-range temperature measurement with a visual display.

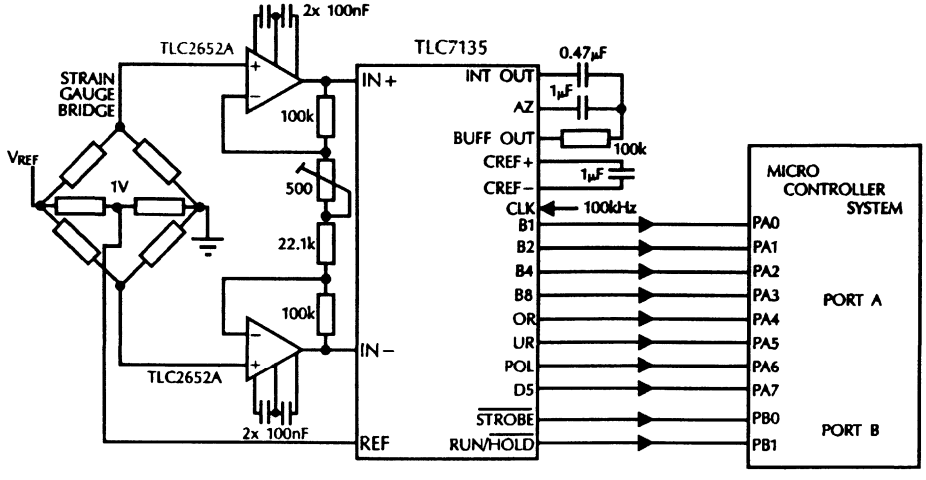
In this general purpose 41/2 digit panel meter, a voltage input or transducer signal (transformed into a voltage between +/-2V) is converted with more than 14 bits resolution. The result is displayed, including sign, on a 41/2 digit LED display. The TLC7135 has multiplexed binary coded decimal outputs which are easily interfaced to many numeric displays. The common-anode driver in this application (transistor array 1-5) drives the digit indicated by the digit select lines (D1-D5). The binary coded decimal (BCD) to seven segment decoder "SN7447" determines which segments of the LED are lit to form the correct digit. The most significant digit is blanked on zero reading.

TLC7135

- **1/2 digit precision ADC**
- **50ppm resolution**
- **1pA typical input current**
- **Zero error < 10æV**
- **Autoranging capability**
- **Easy interface to uP and UARTs**
- **Multiplexed BCD output**

The circuit uses a low power LT1004 1.2V bandgap reference available from Texas Instruments. The input shows a typical RC filter for input signal smoothing. Depending on the needs of the application, the time constant for this filter can be made shorter or longer, or the filter can be deleted completely if not required. The 0.47æF integrating capacitor should be of a type with low dielectric absorption such as a polypropylene capacitor. However, polystyrene or polycarbonate capacitors will also work well. A high dielectric absorption causes the integrating capacitor value to be different during the integrate and de-integrate phases. Choosing the clock frequency fO, such that an integral multiple of 50Hz periods occur during the signal integrate phase, maximizes the 50Hz pick-up rejection. The applied fO=100kHz is such a frequency providing 2.5 conversions per second.

2.1.2. A 14 bit data acquisition system



- TLC2652A provides 200.00 mV FS sensitivity
- TLC7135's control signals allow simple microcontroller interface

Figure 2.5 - A 14 bit data acquisition system

The TLC7135 interfaces easily to UARTs or microprocessor systems via control signals. The control lines BUSY, STROBE, RUN/HOLD, OVER-RANGE and UNDER-RANGE support microprocessor based measurement systems. The control signals can also support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

In this application only 10 interface lines are required for the interface between the 14 bit accurate converter and a microprocessor or peripheral parallel port. It is possible to eliminate the use of the multiplexed digit select lines (D1-D4) by counting the digit strobes from the STROBE output in a software register. The most significant digit select line (D5) is used to simply monitor that an end-of-conversion has occurred.

In order to synchronize data transfer between microprocessor and TLC7135, the microprocessor tests D5. If D5 is true, then an end-of-conversion has occurred. A data pointer is then initialized and assembly of 5 BCD coded digits begins. The next 4 STROBE pulses will find D5 false, causing the BCD digits to be stored in memory or register locations. The fifth STROBE pulse signals an end of data transfer, so the user can display or manipulate the data as desired. The RUN/HOLD input allows the microprocessor to control the TLC7135 mode of operation. Holding RUN/HOLD high results in continous conversions. When RUN/HOLD is held low the TLC7135 will remain in auto-zero mode. If

RUN/HOLD is pulsed high, the TLC7135 will perform a conversion, output new data, and return to auto-zero mode.

The TLC7135 has a standard +/-2V full scale input voltage and 20,000 counts maximum; e.g. one count corresponds to 100uV. Additionally, its analog zero error is less than 10uV and the drift less than 0.5uV/ °C. Consequently, if increased sensitivity is required, extreme DC precision op amps are required for amplification.

In this application the sensitivity has been increased by a factor of ten to 200mV for full scale without compromising accuracy. Two TLC2652A chopper-stabilized op amps with a maximum of 1uV offset voltage and negligible drift amplify the strain-gauge bridge signal 10 times using an instrumentation amplifier configuration. 1 count in this application corresponds to only 10uV strain-gauge bridge signal.

2.2. Successive approximation

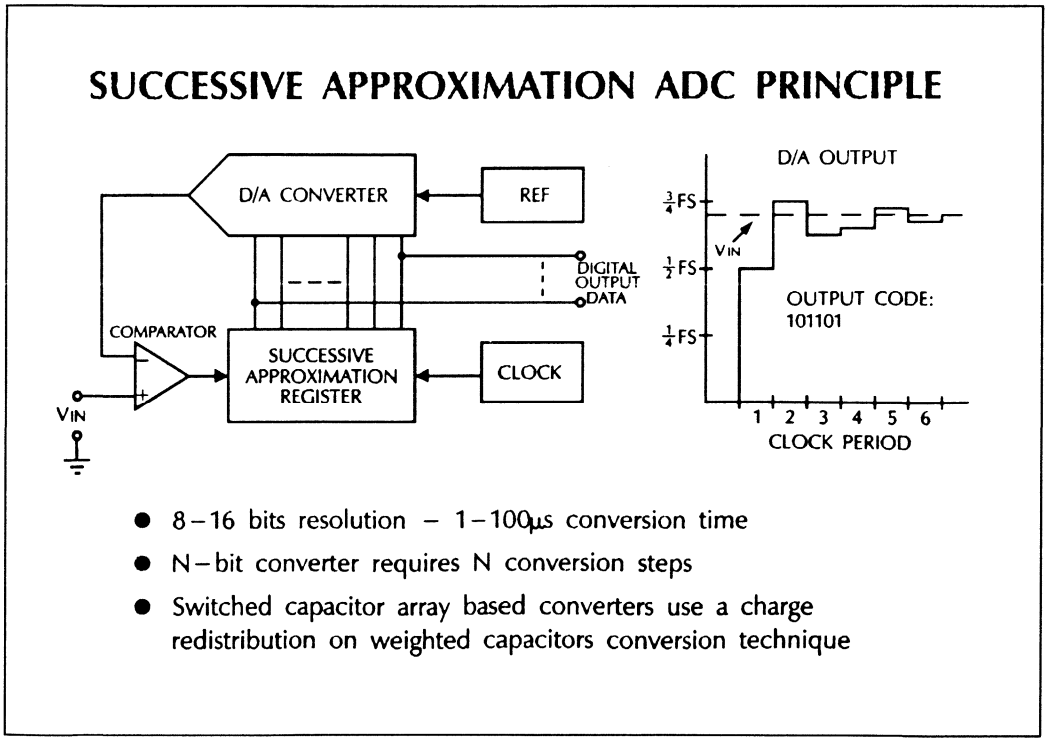


Figure 2.6 - Successive approximation Principle

Successive approximation ADCs continue to be the most popular type of converter. A wide range of devices with resolution from 8-16 bits are available and with conversion rates from 100us to below

1us. Successive comparison of an unknown analog input voltage with binary weighted values of a reference give this method its name of "successive approximation". A converter of N-bit resolution takes "N" steps to achieve a digital output.

One input of the comparator, shown in the block diagram, is driven by an unknown input signal, VIN , while the output of the DAC drives the other. The successive approximation register provides the input to the DAC and responds to the output from the comparator.

When the DAC has its MSB set to logic 1 (with all other bits zero), by the successive approximation register (SAR), it will produce a voltage output of 1/2 the reference and analog input full scale range. The comparator then determines whether the DAC output is above or below the unknown input signal. If, as shown, the input signal VIN is above the DAC output value, the MSB is retained in the successive approximation register while the next weight of 1/4 the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register.

While the successive approximation converter process continues, the input signal must be held constant using a sample and hold circuit in front of the comparator. Alternatively, the signal should, as a rule of thumb, vary maximum 1/2 LSB during conversion. This puts a slew-rate or full scale frequency limitation on the signals the converter can handle.

More recent successive approximation converter designs, using switched capacitor networks utilizing charge redistribution, are replacing older designs using resistive ladder DACs. This is due to the switched capacitor technique's smaller chip area, higher speed and inherent sample and hold function. Texas Instrument's Advanced LinCMOS technology with its double polysilicon layers is an ideal process for building well matched switched capacitor circuits for successive approximation ADCs.

2.2.1. The TLC1550/TLC1551 10-bit Analog to Digital Converter

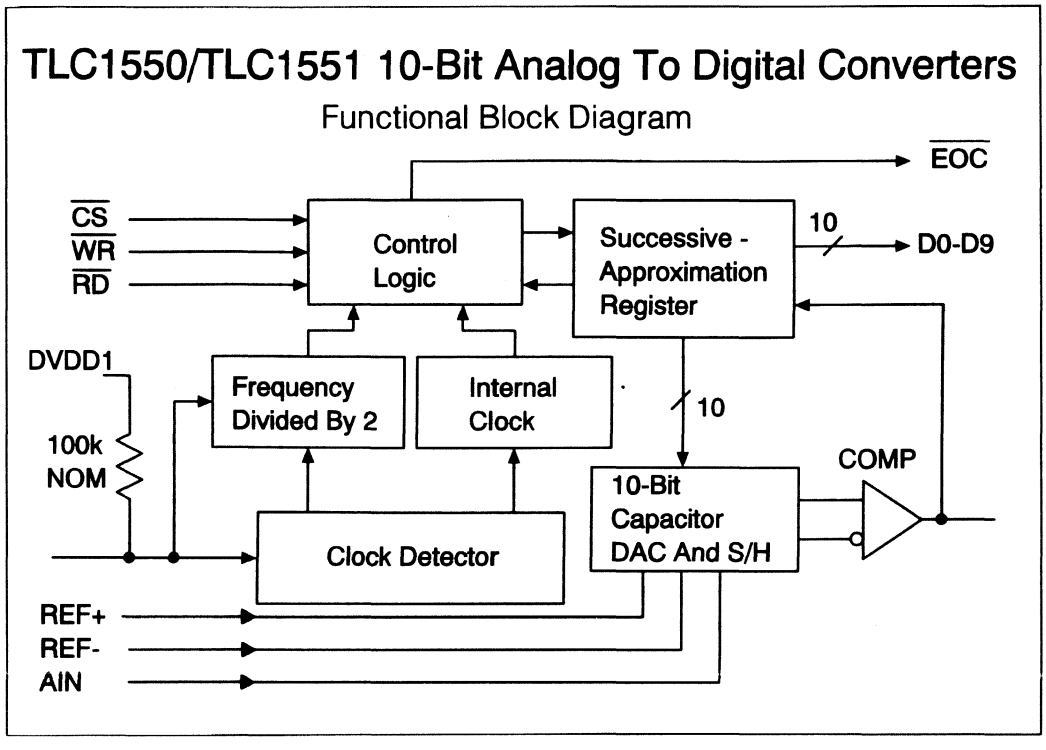
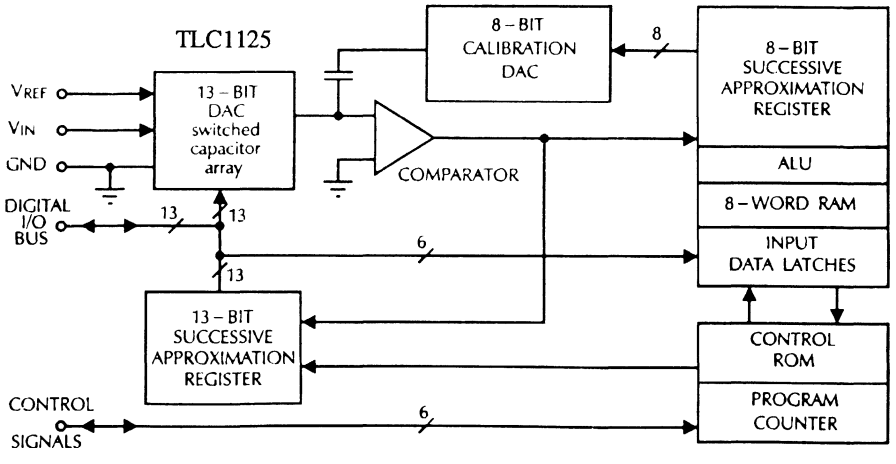


Figure 2.7 - TLC1550/TLC1551 10-bit Analog to Digital Converter

A wide range of 8-10 bit LinCMOS successive approximation ADCs with serial or parallel output and input multiplexer options are available from Texas Instruments. The TLC1550/TLC1551 is an example of a 10-bit ADC designed for easy interface to DSP. Its features include:

- **Low power dissipation (40mW maximum)**
- **Parallel interface**
- **External or internal clock**
- **6us conversion time**
- **±0.5 LSB total unadjusted error - TLC1550**
- **±1.0 LSB total unadjusted error - TLC1551**

2.2.2. Self calibrating 12 bit plus sign ADC - The TLC1225



- Self – calibration eliminates expensive trimming at factory and offset adjustment in the field

Figure 2.8 - Self calibrating 12 bit plus sign ADC - The TLC1225

TLC1225 is a 12-bit-plus-sign successive approximation ADC utilizing a self-calibration technique to eliminate expensive trimming of thin-film resistors at the factory. Additionally, this technique ensures excellent long term stability, avoiding regular field trimming to maintain conversion accuracy.

The design uses a switched capacitor based charge redistribution technique for the D/A conversion. As 12-13 bits accuracy of capacitor matching is difficult to achieve, seven of them are calibrated during a non-conversion, capacitor-calibrate cycle in which all seven of the capacitors are calibrated at the same time. The calibration or conversion cycle may be initiated at any time by issuing the proper command word to the data bus.

TLC1225 Self calibrating ADC

- **Self calibration eliminates expensive trimming**
- **0V to 5V Unipolar or -5V to +5V Bipolar ranges**
- **12uS conversion time**
- **True differential inputs**
- **Low Power . . . 85mW max**

Calibration cycle (simplified description)

Comparator Offset Calibration Steps:

Step 1 : The input, VIN is shorted to GND in order to ensure that the comparator input is zero. A coarse offset calibration is performed by manipulating the offset error using switches and offset storage capacitors. After this action some of the offset still remains uncalibrated. Step 2 : An A/D conversion is done on the remaining comparator offset with the 8 bit calibration DAC and 8 bit successive approximation register. The result is stored in the RAM.

13 Bit DAC Capacitive Ladder Calibration Steps:

Step 1: The input is internally disconnected from the 13 bit capacitive DAC.

Step 2: The MSB capacitor is tied to VREF, while the rest of the ladder capacitors are tied to GND. The ADC conversion result from the Comparator Offset Calibration Step 2 above, is retrieved from the RAM and is input to the 8 bit DAC.

Step 3: Step 1 of the Comparator Offset Calibration sequence is performed. The 8 bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.

Step 4: Now the MSB capacitor is tied to GND, while the rest of the capacitors are tied to VREF. An MSB capacitor voltage error on the comparator output capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8 bit word and stored in the RAM.

Step 5: The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Step 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

Conversion Cycle (simplified description)

Step 1: Step 1 of the Comparator Offset Calibration sequence is performed. The remaining offset obtained in Step 2 of the Comparator Calibration sequence, is retrieved from the RAM and is input to the 8 bit DAC. Thus, the comparator offset is completely corrected.

Step 2: The input signal, VIN is sampled onto the 13 bit capacitive ladder.

Step 3: The 13 bit ADC conversion is performed. As the successive approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in the 8 bit successive approximation register. This register controls the 8 bit DAC so the total accumulated error for these capacitors is subtracted out during the conversion process.

A conversion takes only 12us. A calibration cycle takes 4 times longer. Calibration is required upon power-up to achieve full accuracy. Regular recalibration is recommended to avoid drift. This is particularly true in systems where self-heating or environmental temperature changes occur.

TLC1225 Analog design considerations

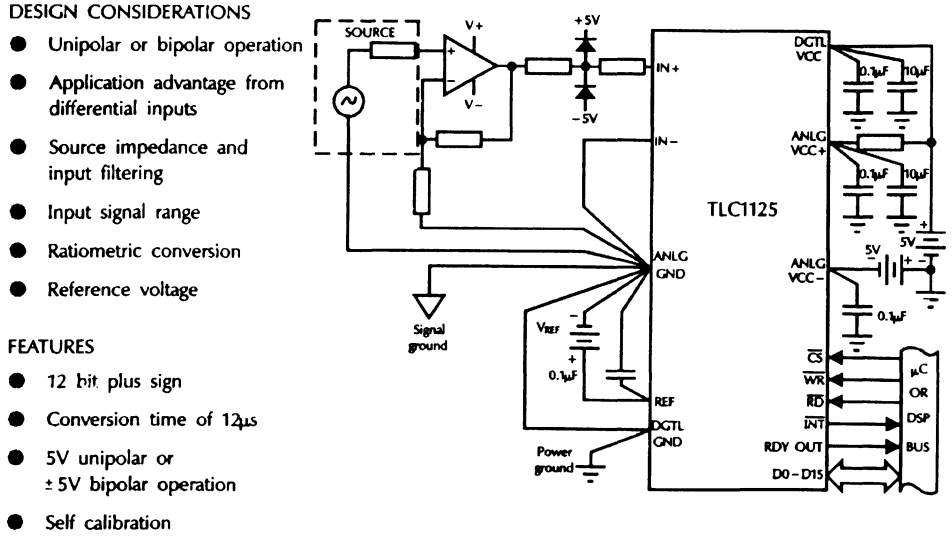


Figure 2.9 - TLC1225 Analog design considerations

When designing with a medium to high resolution converter like the TLC1225 several fundamental considerations have to be made.

Power supply

The device features a 0 to 5V analog input range with a single +5V supply voltage (Unipolar configuration) or -5 to +5V analog input range with +/-5V supplies (Bipolar configuration). The choice of the configuration depends on the application and available supply voltages.

Proper supply grounding of both digital and analog supplies are required as shown. Avoid ground loops that inductively could pick up hum. Also, signal ground leads should only carry the return current from the signal source. Any additional current may cause a voltage drop and result in system errors. Noise spikes on the supply lines can also cause conversion errors.

All supply input pins should be bypassed by 1 to 10uF low inductance capacitors with short leads. Further high frequency decoupling can be achieved with a 100nF ceramic capacitor, placed in parallel

with the aforementioned tantalum capacitors. A separate regulator for the TLC1225 or other analog circuitry will greatly reduce digital noise on the analog supply line.

Differential inputs

The device is provided with a true differential input structure. This can be utilized to reduce effects of noise and hum signals common to both input wires. Common-mode noise often appears where long input leads are used or in noisy environments. There is no time interval between the sampling of IN+ and IN- input so these are truly differential and simultaneous sampling rejects even high frequency common-mode signals within the bandwidth of the ADC. Keep IN+ and IN- input leads twisted and their PCB tracks close together.

The true differential input structure allows for simple interface to differential sources such as some strain-gauge configurations. Also, the input can often save a pre-processing differential instrumentation amplifier or act as the third amplifier in such a configuration.

Noise constraints

A general rule of thumb is that the input leads should be kept as short as possible and that the source impedance should be as low as possible.

Long input leads can pick up noise from a digital clock signal with edges too fast for the differential input amplifier's common-mode rejection. This noise can cause conversion errors. Input bypass capacitors may be used for noise filtering. However, the charge on these capacitors will be depleted during the input sampling process when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source impedance must keep pace with the charge depletion of the bypass capacitors during the sampling sequence. The above phenomenon becomes more significant as source impedance and conversion rate increases. For source impedances below 100 Ohm, a 1nF bypass capacitor at the input will prevent pick-up due to series lead inductance of a long wire.

Even in applications without an input bypass filter capacitor, high source impedance can cause a voltage drop when charging the internal capacitors during the sampling phase. Note, that some op amps, when used as signal source, have high output impedance for the current spikes required to charge the internal capacitors of the TLC1225.

Signal conditioning

The input signal range is limited by the supply voltages which means 0 to 5V in unipolar mode and -5 to +5V in bipolar mode of operation.

In either mode, when using a signal conditioning op amp supplied from the same analog supply (supplies), you will need an output swing to the supply rails within a fraction of a millivolt. No op amp can guarantee this performance but some come very close. The LinCMOS precision op amp TLC2201 has a complementary CMOS output state that can swing very close to either rail when not loaded. In addition, it can operate with a single +5V supply as well as with +/-5V supplies. Using this op amp eliminates adjustment of the input range, but a few codes in both the top and bottom of the ADCs dynamic range will be missed due to the limited output swing. A worse limitation is often the accuracy and stability of the power supply (supplies) limiting the input range significantly, even if 1% voltage regulators are used.

For applications demanding high frequency signal conditioning a faster precision op amp like the TLC2027/37 should be employed. However, such op amps have not got rail-to-rail output swing so

higher supply voltages must be used. If +V and -V exceeds the ADC supplies, precautions must be taken to avoid over-voltage on the ADC's input pins. A suitable protection can be accomplished by a small series resistor (preferable a PTC resistor) followed by schottky clamping diodes to either supply. To ensure that the bulk of current from any over-voltage will flow in the schottky diodes rather than in the ADC's internal ESD protection circuitry, an additional small series resistor can be added in series with the input. The maximum input current for the ADC caused by over-voltage should be kept well below +/-5mA.

Mode of operation

The ADC can be used in either absolute or ratiometric reference applications. In an absolute reference system, where the analog input varies between very specific voltage limits, a 13 bit precision voltage source reference is required. An example of such an application is a temperature measuring system using a sensor, which provides 10mV/°C independent of the supply voltage.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the REF pin can be tied to the ADC's positive supply. This technique relaxes the stability requirement of the system

reference as the analog input and the ADC reference move together maintaining the same output code for a given input condition. An example of a ratiometric transducer is a strain-gauge bridge supplied directly from the system power supply. Often both the VIN- and the REF pins are tied to the system power supply via resistive voltage dividers to define an input dynamic range window slightly smaller than that of the supply voltages. This allows a driving op amp to operate at the same supplies as the ADC without needing rail-to-rail swing.

Reference input

The restrictions on the source impedance for the analog inputs also applies to the reference input. In addition, noise from the reference must be kept at a minimum by careful decoupling of both low and high frequency noise.

In summary, precision 12 bit ADCs require some adjustments to compensate for offset errors. The TLC1225, with its self-calibration facility ensures low and stable offset with time and temperature eliminating initial trimming and re-adjustment due to aging.

2.3. Flash Analog to Digital Conversion

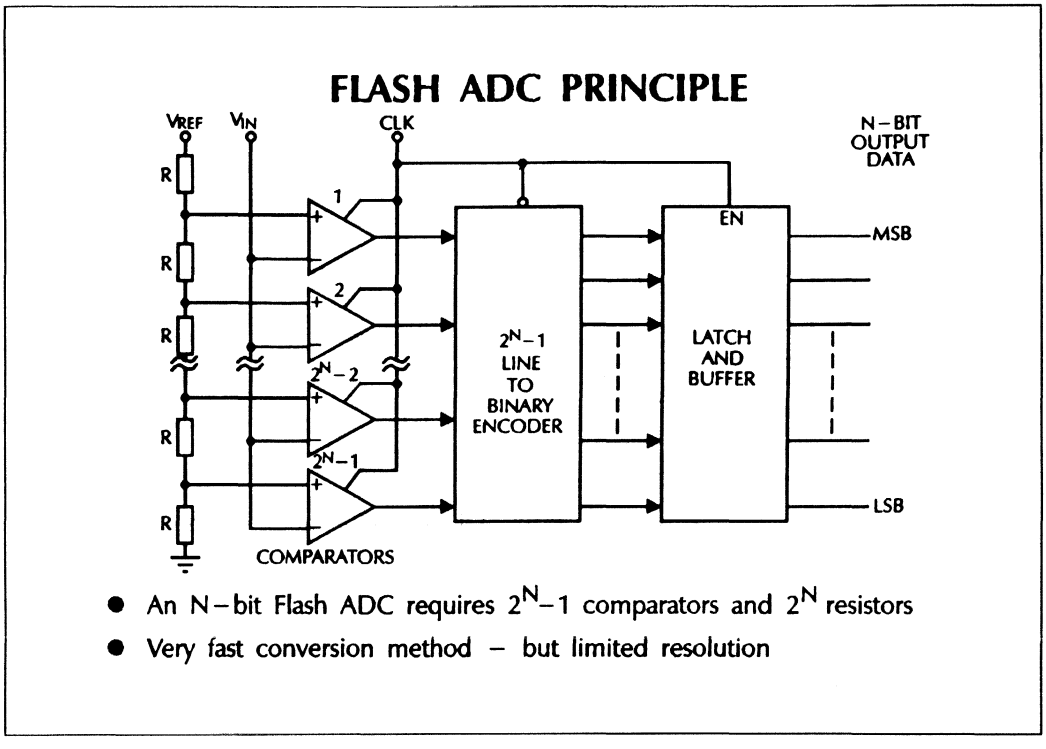


Figure 2.10 - Flash Analog to Digital Conversion

The flash ADC derives its name from its ability to do a very fast conversion. This is accomplished by providing a comparator for every quantisation level. Hence, an N bit flash ADC requires 2N - 1 comparators.

These comparators all examine the input simultaneously and make an immediate conversion. The block diagram shows that each comparator has one input connected to the input signal and the other to a tap on a reference potential divider. The resultant so-called "thermometer" code is then encoded into binary and is output through a latch. This technique provides the fastest means of conversion but requires the use of a large die area for the comparators and resistor ladder .

Presently, the flash converters available cover 4 to 10 bit resolution with sampling rates into the Gigaherz range. However, the most popular applications are in the video field, where 6 to 8 bit resolution and 20 mega samples per second are the standard specifications.

A compromise between "speed" and chip area is the semiflash method using a two step flash principle. In this case, the most significant bits are coded first and then the remaining bits afterwards. This trades off a reduction in speed with a reduction in the number of comparators required and

consequently the size (and cost) of the die. An example is the LinCMOS 8 bit semiflash ADC, TLC0820 with a conversion rate up to approximately 1 mega-samples per second.

2.3.1. CCD Document scanner

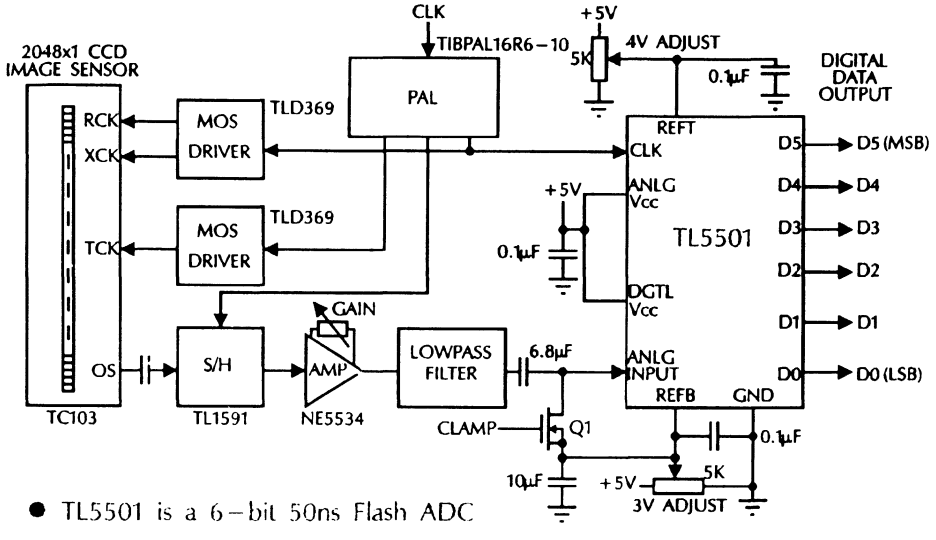


Figure 2.11 - CCD Document scanner

TL5501 Flash ADC

- **6 bit resolution**
- **LSB linearity**
- **Conversion rate up to 20MSPS**
- **Analog input range ...1V**
- **5V single supply operation**

Document scanners for facsimile transmission (FAX machines) over the public telephone network are an expanding market. This implementation is scanning the document using a TC103 (2048 x 1) CCD line image sensor controlled from a PAL chip via some TLD369 MOS drivers and level shifters. The CCD output video signal data stream (typ 500kHz) is superimposed on a DC voltage and reset between each pixel. A coupling capacitor removes the DC and a TL1591 sample and hold circuit holds the signal level between pixels leaving a continous video envelope. The video signal is then amplified to a one volt peak to peak signal required by the TL5501 flash ADC. Post lowpass filtering removes

residual clock signals. The video signal is then clamped to +3V by Q1 to provide DC restoration and adjust the DC component for the ADC input pin ANLG INPUT. The digitized video signal appears at a pixel rate of typically 500kHz on the output of the TL5501 ADC.

2.4. Video DACs

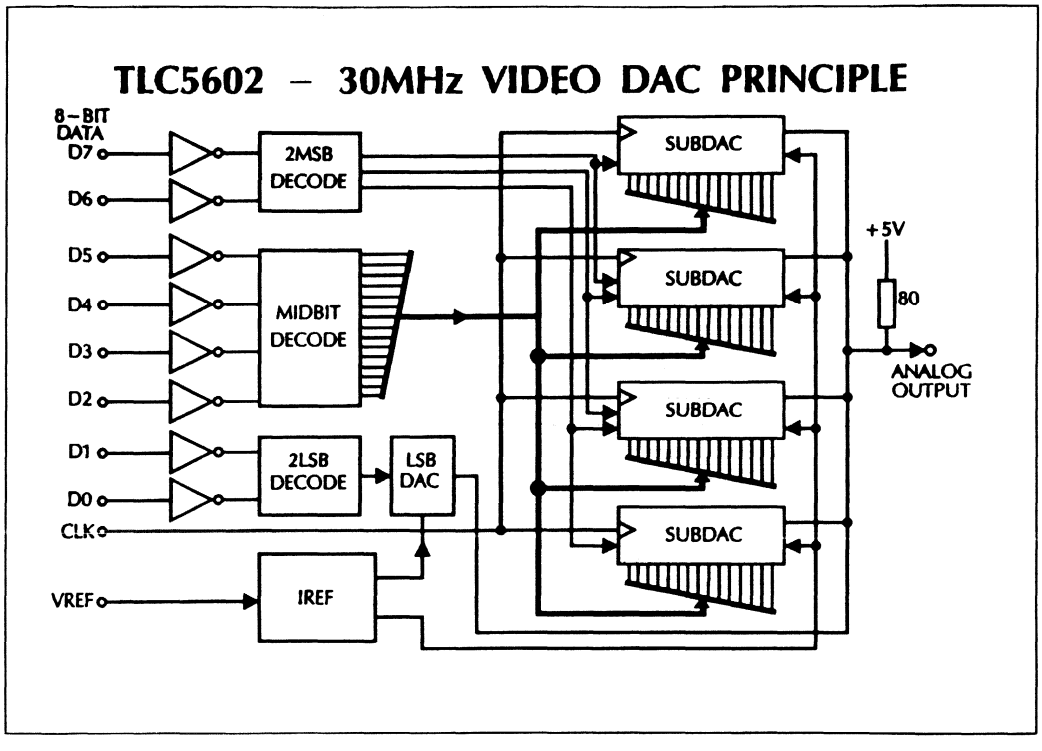


Figure 2.12 - TLC5602 : A 30 MHz Video DAC

A traditional problem with high speed DACs is that of glitch errors which occur at the changeover from one code to the next. This is especially true at the midpoint code where all bits change at the same time. If there are differences in internal propagation delays, there can be large transient errors at the output as the bits change over. To overcome this problem the 8 bit TLC5602 DAC is designed with three distinct building blocks.

1. **The two least significant bits determination block**
2. **The two most significant bits determination and control block**
3. **The four middle bits determination block**

The whole DAC works on the basis of summation of current, which is controlled by the IREF block. As the digital input code increases, the amount of current drawn is reduced, so that the output voltage increases linearly.

The input binary word is divided into three. The middle four bits (D2-D6) are fed to a decoder which controls a series of FET switches . For example, if the input were 10102 = 1010 , 10 of the switches would be turned off. This code is fed via a bus to four SUBDAC blocks in parallel. The two MSBs then determine which blocks are either fully on, fully off or are responding to the code fed in from the MIDBIT bus. For example, if the MSBs are 01, the first SUBDAC is fully on and the second is controlled by the bus.

The outputs from the SUBDACs are linked at the output where they are summed and converted to a voltage by an internal 80 ohm pull-up resistor.The two least significant bits are determined in a similar manner but switch a smaller ratioed current.

TLC5602 DAC

- **8 bit resolution**
- **1/2 LSB linearity**
- **Conversion rate up to 20MS/s**
- **Analog input range ...1V**
- **5V single supply operation**
- **LinEPIC process**
- **Low Power ... 80mW**

This conversion technique has two major advantages:

1. Glitches are greatly reduced because there are only small changes between adjacent codes.

2.Breaking down the mid four bits and using the MSBs as control bits means that similar , small currents are being switched on and off as the digital code increases. since the SUBDACs are very well matched this provides inherent linearity and means that differential gain errors are much reduced due to code widths being much the same throughout the transfer curve.

The currents are generated using the precise resistance of MOSFETs which are well matched across the whole chip. Additionally, the 1um LinEPIC CMOS process gives very low power consumption without large glitches on the supply rails.

2.4.1. A Video Frame Store

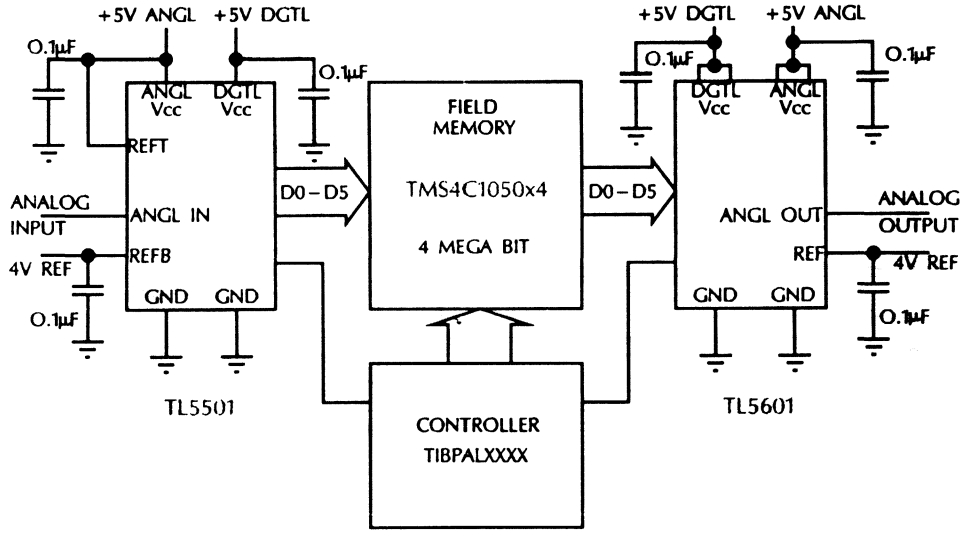


Figure 2.13 - video frame store

A typical application area for 6-8 bit video DACs and flash ADCs is for video recorder frame-store where a video signal frame can be digitized and held in a field memory. By continuous scanning of the stored video picture in the memory followed by digital to analog conversion a frozen or still video picture is achieved.

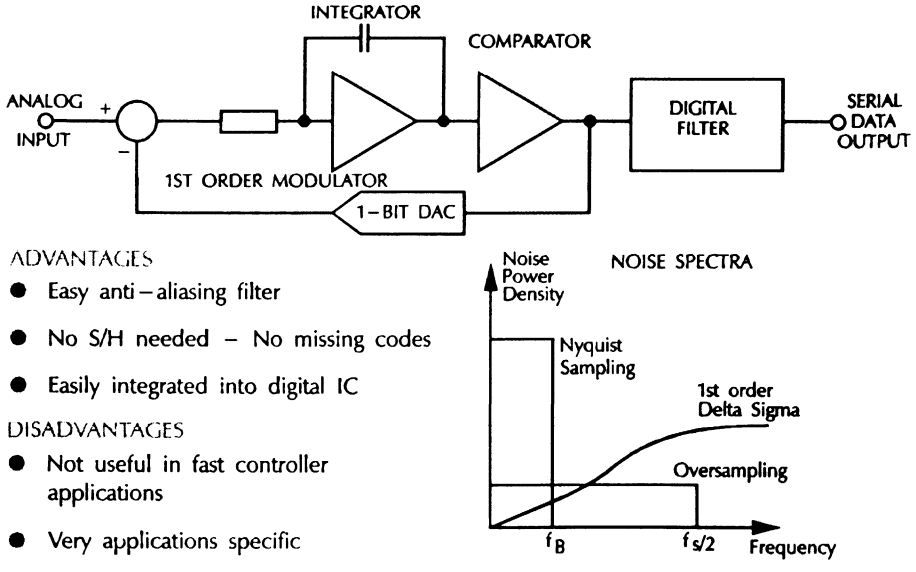


Figure 2.14 - ***Delta-Sigma ($\Delta\Sigma$) Conversion***

2.5. Delta Sigma Converters

Digital converters utilizing the delta-sigma conversion technique are notable not only for their impressive specifications (12-20 bit resolution), but also because they provide a stronger link to the digital IC realm and especially to digital signal processing (DSP).

The basic principle is not new but silicon realizations first started to be cost-competitive with the advent of 1-2æm technologies due to the huge chip area occupied by the required post digital filter. Further reduction in semiconductor geometries below 1æm will make this type of converter even more attractive.

2.5.1. Delta-Sigma structure

The basic 1st order delta-sigma converter contains two major blocks; a closed-loop integrating modulator and a digital filter. The modulator as shown, consists essentially of a 1 bit DAC, a difference node (hence delta), an analog integrator (hence sigma), and a clocked comparator. Practical converters have more stages, thus 2nd or 3rd order modulators.

Input signals are digitised on the comparator output and a bit stream is fed to the digital filter and to the 1 bit DAC. The output of the DAC which is controlled from a precision reference is summed at the

difference node with the input signal. The job of the signal from the 1 bit DAC - a train of positive or negative constant width, constant amplitude pulses - is to keep the charge on the integrating capacitor, as close to zero as possible. This is accomplished by balancing or nulling the charge.

A positive voltage applied to the input of the modulator begins to appear as charge on the integrator's capacitor and a voltage at its output. The voltage is sensed by the comparator, producing a train of ones at its output and a train of pulses of opposite polarity to the integrator input voltage, through the 1 bit DAC and summing node. When the pulses from the 1 bit DAC have reduced the charge to zero and begin charging it to the opposite polarity, the comparator will see a negative voltage and produce zeros. The more positive the input voltage, the greater ratio of ones to zeros in the output bit stream. The more negative the input, the greater the ratio of zeros to ones. If the analog input voltage is zero, an equal number of ones and zeros appear in the output.

To get from the one-bit stream of data coming out of the comparator to a data stream with usable N bit information (for an N bit converter) requires digital signal processing. The digital filter then decimates the single bit stream into words of length N bits.

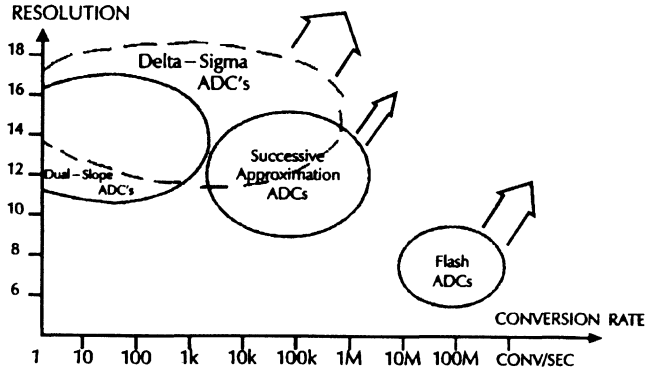
2.5.2. The benefit of oversampling

How can a 1 bit ADC give a high S/N ratio? Sampling with a conventional converter at the Nyquest rate places all the quantization noise within the band of interest. Oversampling spreads the quantization noise over a much wider bandwidth reducing the level of noise in the band of interest. Delta-sigma oversampling further reduces the noise in the bandwidth of interest with the noise shaping of the integrator-loop. However, a sharp roll-off digital post filter is required which basically replaces the analog anti-aliasing input filter required for successive approximation converter types . Delta-sigma converters require only a simple RC filter on the input for anti-aliasing due to a high ratio between the sampling frequency and the maximum frequency of interest.

Although delta-sigma converters are easier to integrate onto digital processes than conventional successive approximation converters which require an anti-aliasing filter, good linear processes are still required for optimum performance of the modulator portion. This design is associated with the usual analog design requirements including high performance op amps and comparators, matched and voltage insensitive capacitors used for switched capacitor realization of the integrators and finally a precision reference.

Areas where oversampling technique seems especially attractive are speech processing in telecom, audio processing and metering applications.

2.6. Resolution and Conversion Rate



- The best ADC depends on the application
- Both resolution and speed are ultimately limited by the process
- High resolution ADC's will be more oriented towards "oversampling" type converters, particularly with development of sub micron technologies

Figure 2.15 - Resolution and conversion rate

Each type of converter has its own application areas. Today the biggest market is for successive approximation converters used in a variety of applications such as automotive, high performance signal processing and general industrial applications. Dual slope converters are mainly used in metering type of applications or for conversion of slowly changing signals like temperature. Delta-sigma conversion technique is expected to replace many of these application over the next decade. The flash converters market is also growing fast due to the increased demand for video signal processing and other applications in the consumer segment of the market.

3. Data Conversion Terminology

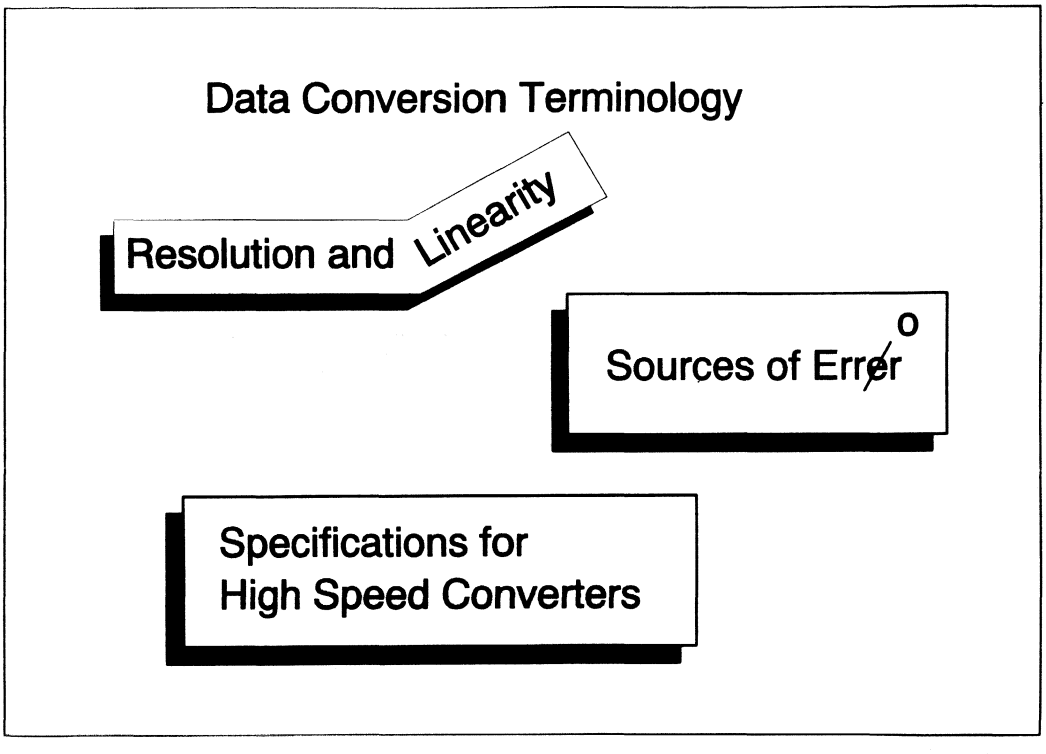


Figure 2.16 - Data Conversion Terminology

This section addresses the way the specifications for a data converter are defined on a manufacturers datasheet. It covers the sources of error that change the characteristics of the device from an ideal function to reality.

3.1. The Ideal transfer function

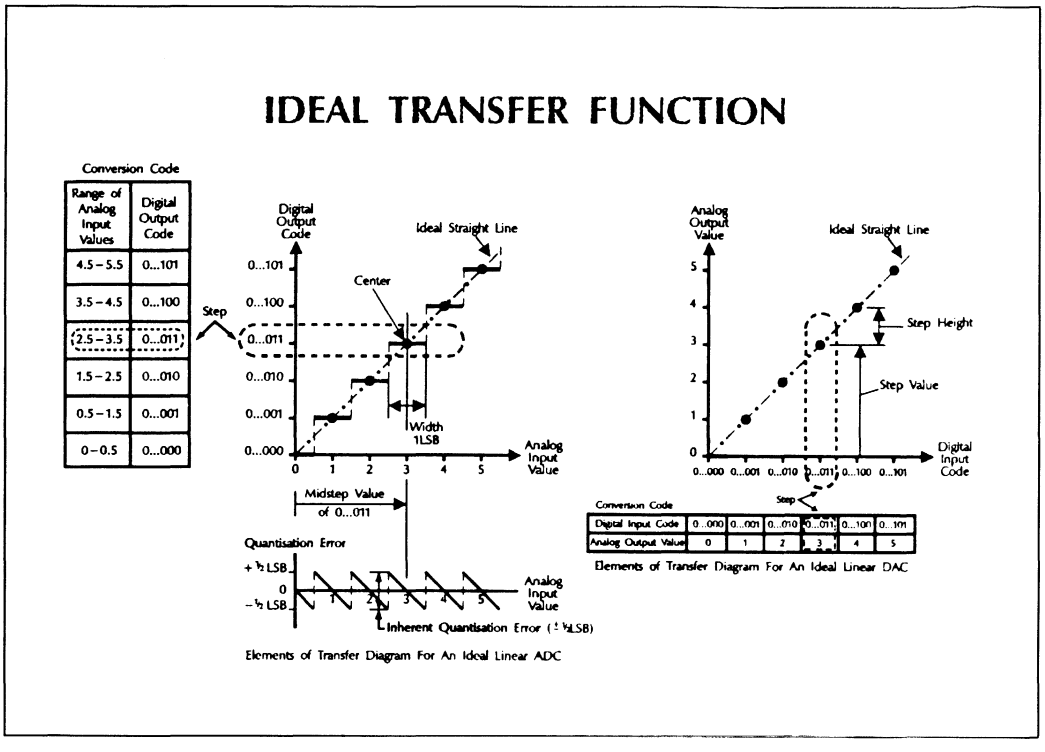


Figure 2.17 - The Ideal transfer function

3.1.1. Analog to Digital Converter (ADC)

An ideal ADC uniquely represents all analog inputs within a certain range by a limited number of digital output codes. The diagram shows that each digital code represents a fraction of the total analog input range.since the analog scale is continuous, whilst the digital codes are discrete, there is a quantisation process that introduces an error. As the number of discrete codes increases, the corresponding step width gets smaller and the transfer function approaches an ideal straight line. The steps are designed to have transitions such that the midpoint of each step corresponds to the point on this ideal line.

The width of one step is defined as 1 LSB (one Least Significant Bit) and this is often used as the reference unit for other quantities in the specification. It is also a measure of the resolution of the converter since it defines how many portions the full analog range is divided into. Hence, 1/2 LSB represents an analog quantity equal to a half of the analog resolution.

The Resolution of an ADC is usually expressed as the number of bits in its digital output code. For example, an ADC with an n-bit resolution has 2^n possible digital codes which define 2^n step levels.

However, since the first (zero) step and the last step have only half the full width, the Full-Scale-Range (FSR) is divided into 2^n - 1 step widths. Hence

1 LSB = FSR / (2^n - 1) for an n-bit converter

3.1.2. Digital to Analog Converter (DAC)

A DAC represents a limited number of discrete digital input codes by a corresponding number of discrete analog output values. Therefore, the transfer function of the DAC is a series of discrete points . For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. A DAC can be thought of as a digitally controlled potentiometer whose output is a fraction of the full scale analog voltage determined by the digital input code.

3.2. Sources of Static error

Static errors, that is those errors that affect the accuracy of the converter when it is converting static (D.C.) signals, can be completely described by just four terms.These are ***Offset*** error, ***Gain*** error, ***Integral nonlinearity*** and ***Differential nonlinearity***. Each can be expressed in LSB units or sometimes as a percentage of the FSR. For example, an error of 1/2 LSB for an 8 bit converter corresponds to 0.2% FSR.

3.2.1. Offset error

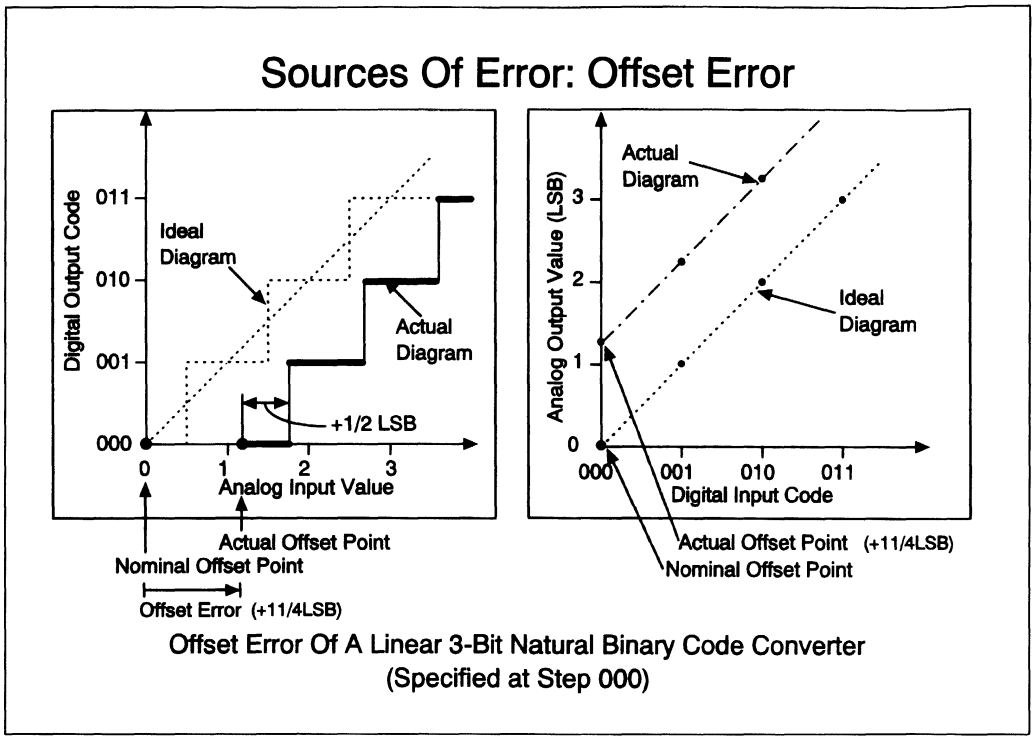


Figure 2.18 - Offset error

The offset error is defined as the difference between the nominal and actual offset points as shown . For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero scale error.

3.2.2. Gain error

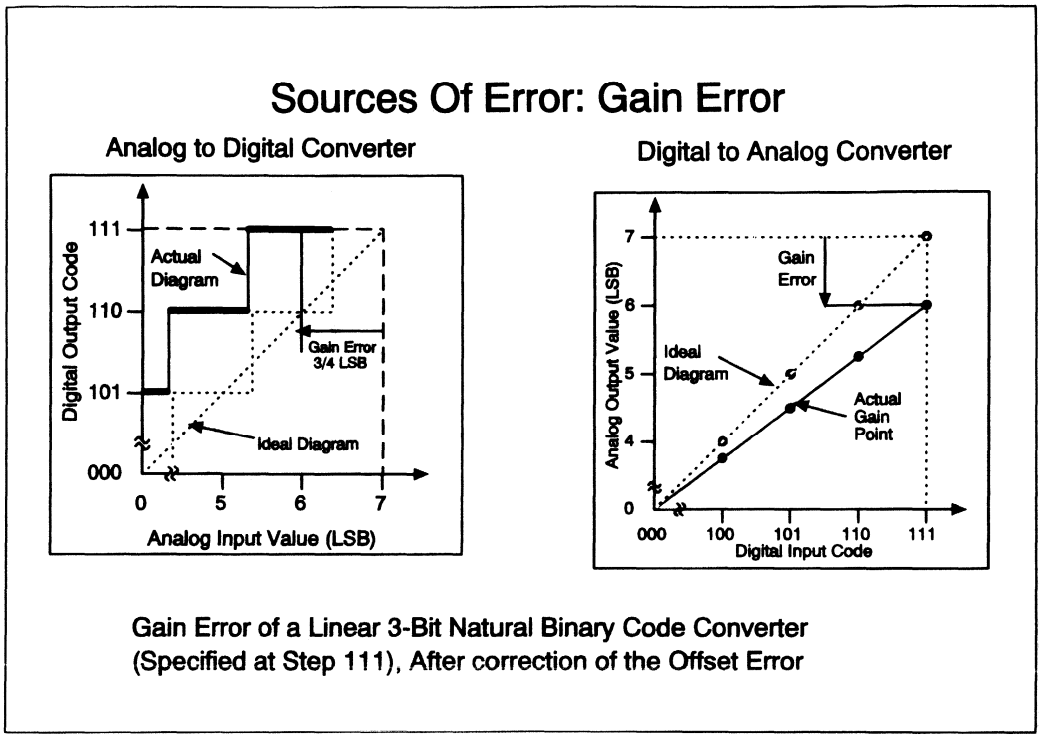


Figure 2.19 - Gain error

The gain error is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

3.2.3. Differential Non-Linearity (DNL) Error

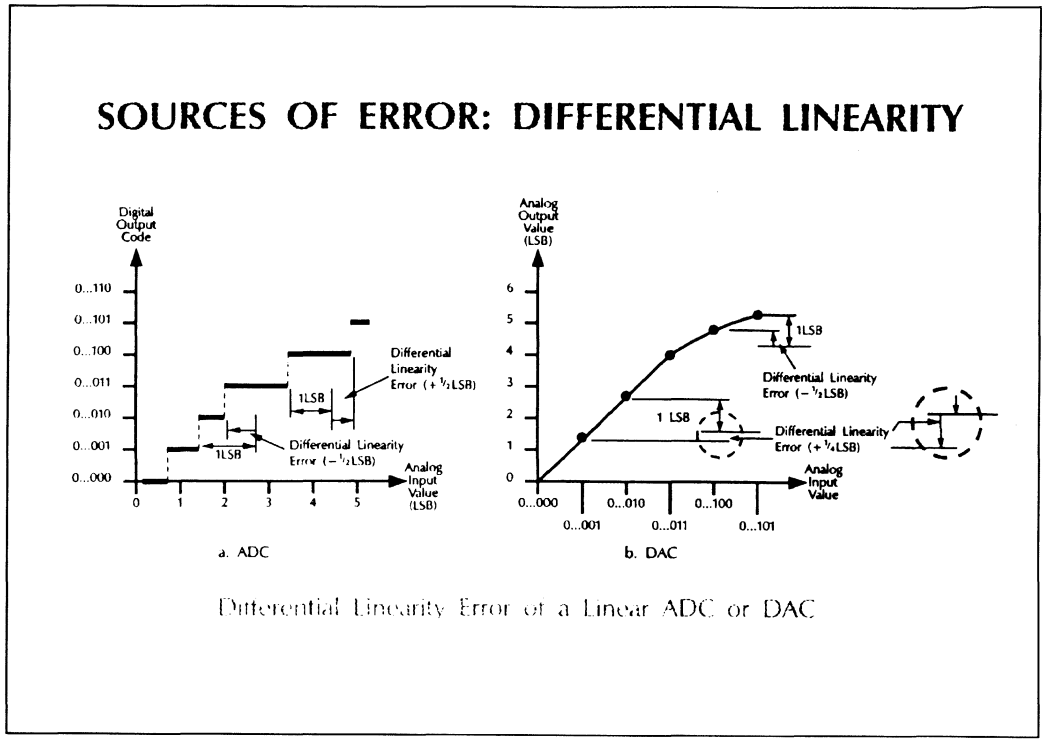


Figure 2.20 - Differential Non-Linearity (DNL)

The differential non-linearity error is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential non-linearity is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter may become non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there will be missing codes i.e. one or more of the possible 2^n binary codes are never output.

3.2.4. Integral Non-Linearity Error (INL)

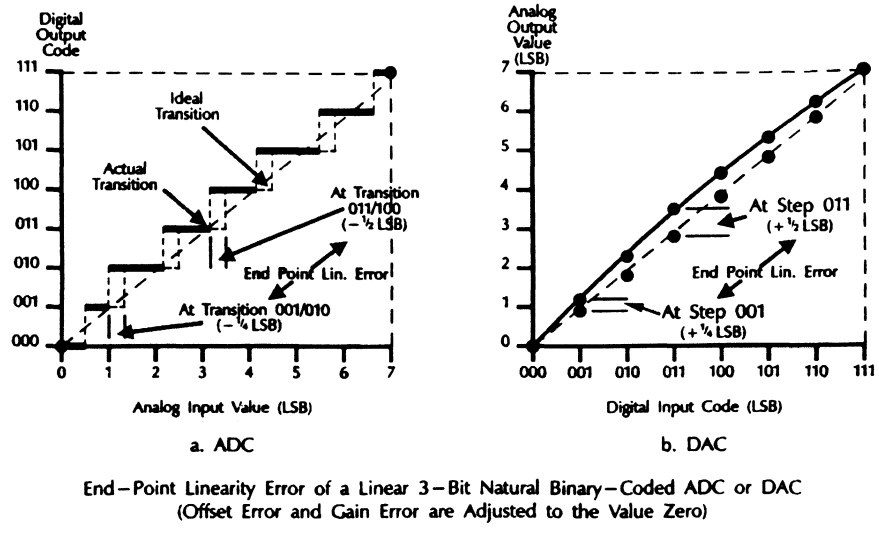


Figure 2.21 - Integral Non-Linearity (INL)

The integral non-linearity error (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a "best straight line" which is drawn so as to minimise these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called "end-point" linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name "integral non-linearity" derives from the fact that the summation of the differential non-linearities from the bottom up to a particular step, determines the value of the integral non-linearity at that step.

3.2.5. Absolute accuracy error (Total Error)

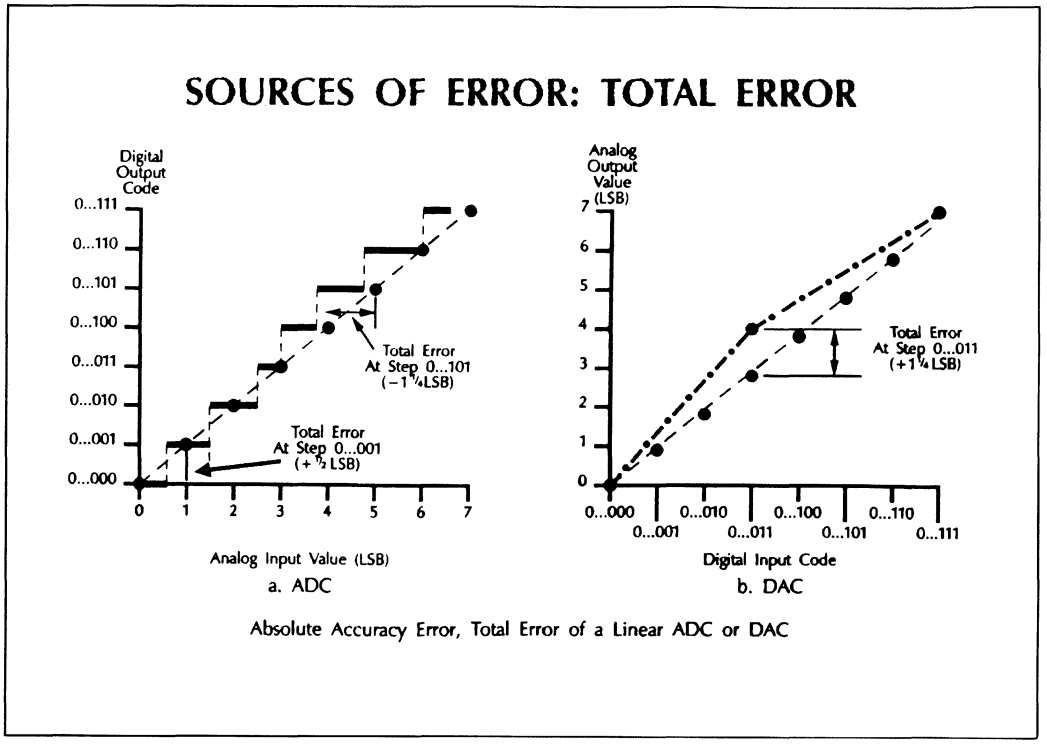


Figure 2.22 - Absolute accuracy error

The absolute accuracy error or total error of an ADC is the maximum value of the difference between an analog value and the ideal midstep value offset, gain and integral linearity errors and also the quantisation error in the case of an ADC.

3.3. Specifications for flash converters

The arrival of flash converters has made it possible to use digital processing in applications that were previously entirely analog. Digital television is a prime example of this. However, with the introduction of these devices came the introduction of new specifications to define their performance. This section defines some of these.

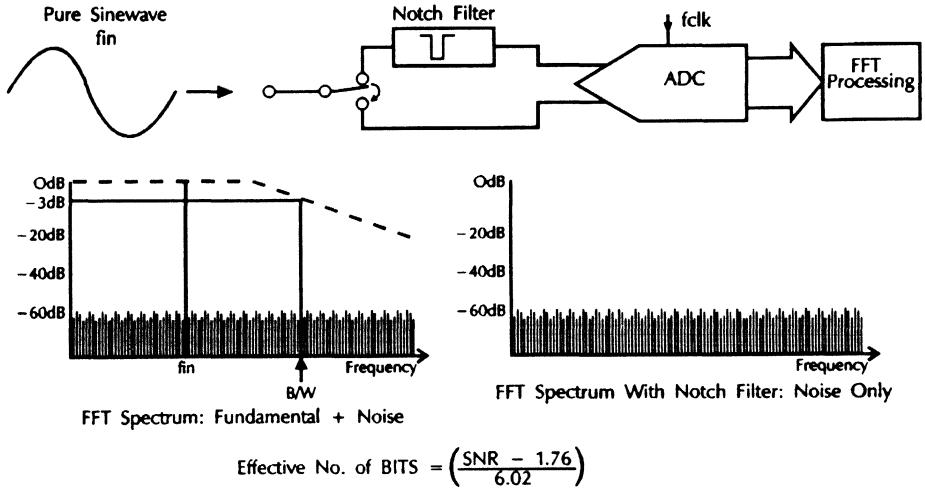


Figure 2.23 - Bandwidth and Signal-to-NoiseRatio

Bandwidth

The bandwidth of a high speed ADC is defined as the frequency of the analog input signal whose output amplitude is 3dB down when the converter is operating at its maximum conversion rate. This can be measured either by reconstructing the output using a reference DAC or else by performing an FFT (Fast Fourier Transform) on the output and comparing the spectrum with the fundamental.

Another factor that limits the bandwidth is the possibility of spurious "speckle" or missing codes. These are caused by the different propagation delays through the comparators measuring the input signal. As the slew rate of the input increases there is an increased comparators all reading "1" up to a point and then the rest reading "0", a so called "bubble" can occur when a "0" is found between two "1"s. When this is decoded, it is a non-recognised code which often is translated to full scale or zero , so producing a spurious code at the output. In some converters, this occurs before the 3dB bandwidth as defined above.

Many flash converters make use of a Gray code in the decoding process to help reduce this effect. The Gray code has the advantage that consecutive can be minimised.

Signal-to-noise ratio and effective bits

For a full-scale sinewave input , the theoretical SNR for an N bit converter is given by

SNR = 6.02N + 1.76 dB (This will be derived later on)

The normal way of measuring the SNR for a flash converter is to digitise a full scale sinewave and then perform an FFT on the output. The rms power of the fundamental is then compared to the noise floor by inserting a notch filter at the input frequency so that the output is purely due to the effects of noise. The ratio of the two is taken to give a direct measurement of the SNR. This measurement can then be used to determine the number of effective bits of accuracy the converter displays at that frequency. For example, a nominal 8 bit resolution ADC may be specified as having 45dB SNR at a particular input frequency. The number of effective bits is defined as

N_{EFF} = (SNR-1.76)/ 6.02 = 43.24 / 6.02 = 7.2 bits

The actual performance of the device is therefore worse than its nominal spec at this frequency.

3.4. Aperture error

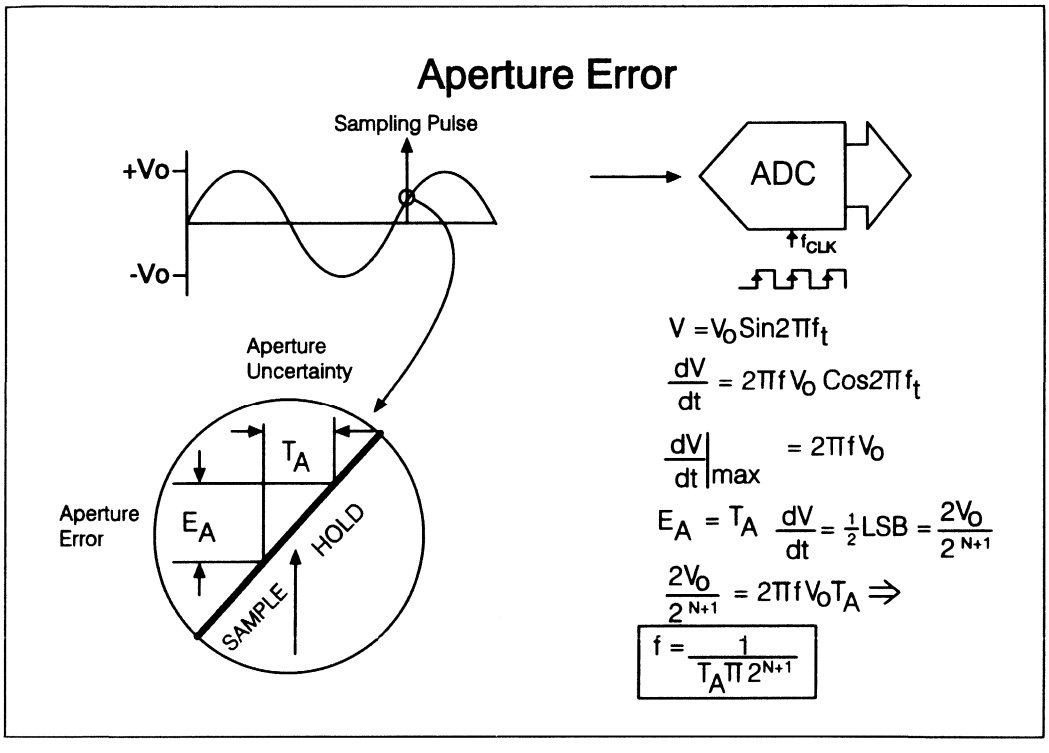


Figure 2.24 - Aperture error

Aperture error is caused by the uncertainty in the time at which the sample/hold goes from sample mode to hold mode. This variation is caused by noise on the clock or the input signal The effect of the aperture error is to set another limitation on the maximum frequency of the input sinewave because it defines the maximum slewrate of that signal. For a sinewave input as shown, the value of the input V is defined as

$$V = V_0 \sin 2\pi ft$$

The maximum slew rate occurs at the zero crossing point and is given by

$$\frac{dv}{dt}|_{MAX} = 2\pi f V_0$$

If the aperture error is not to affect the accuracy of the converter, it must be less than 1/2 LSB at the point of maximum slewrate. For an N bit converter therefore

$$E_A = t_A \frac{dV}{dt} = \frac{1}{2} LSB = \frac{2V_0}{2^{n+1}}$$

Substituting into this gives

$$\frac{2V_0}{2^{n+1}} = 2\pi f V_0 t_A$$

So that the maximum frequency is given by

$$f_{MAX} = \frac{1}{t_A \pi 2^{n+1}}$$

3.5. Differential Phase and Gain

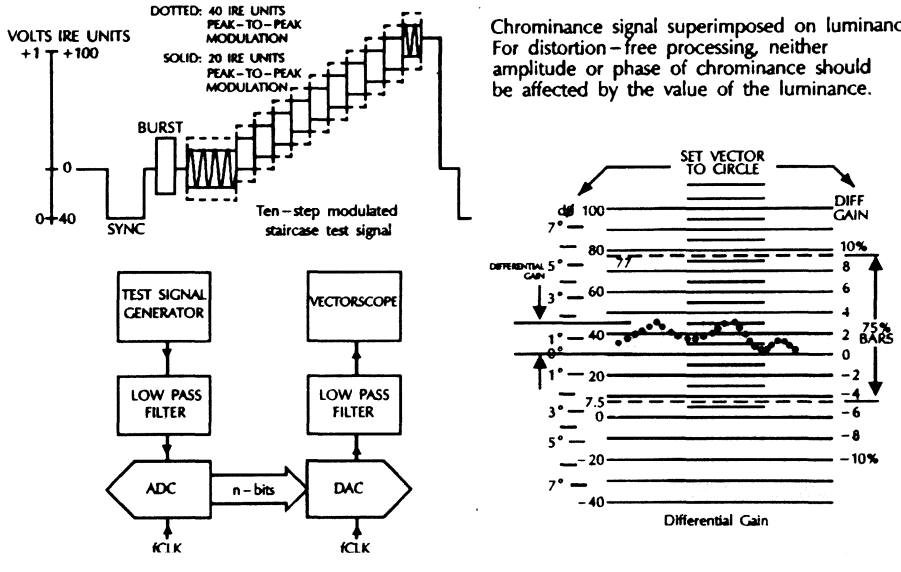


Figure 2.25 - Differential Phase and Gain

Differential gain is defined as "the percentage difference between the output amplitude of a small high frequency sinewave at two stated levels of a low frequency signal on which it is superimposed." Differential phase is similarly defined for the output phase difference in degrees, of the two signals.

These definitions are of direct relevance in video applications. A colour signal is represented by a small amplitude, high frequency Chrominance signal which determines the colour saturation, and a lower frequency Luminance signal which determines the brightness and onto which the chrominance signal is superimposed. For distortion-free processing, it is important that neither the amplitude or phase of the chrominance is affected by the value of the luminance signal.

Measurements of DG and DP are made using the set up shown , using a standard video test signal (NTSC ramp). This can be either a staircase as shown or a continuous ramp. In each case, the device being tested (ADC or DAC) is used in conjunction with a reference device whose DP and DG are already known. The vectorscope makes a direct measurement of the DP and DG but the trace is unclear because of the quantising effects of the DAC. Hence, the measurement is made from the centre of the trace as shown.

4. Designing with data converters

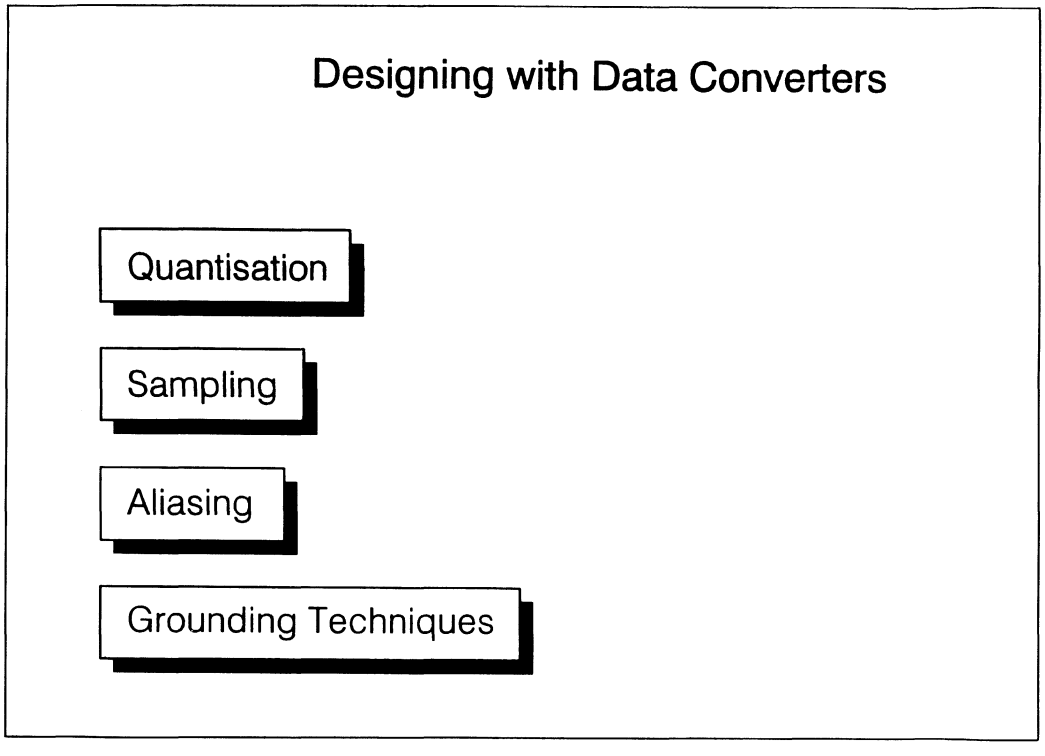


Figure 2.26 - Designing with data converters

This section considers some of the aspects of designing with data conversion products . In each case, the background theory is presented along with examples of how it can be applied to real designs. A design example is presented to conclude the section.

4.1. Data acquisition systems

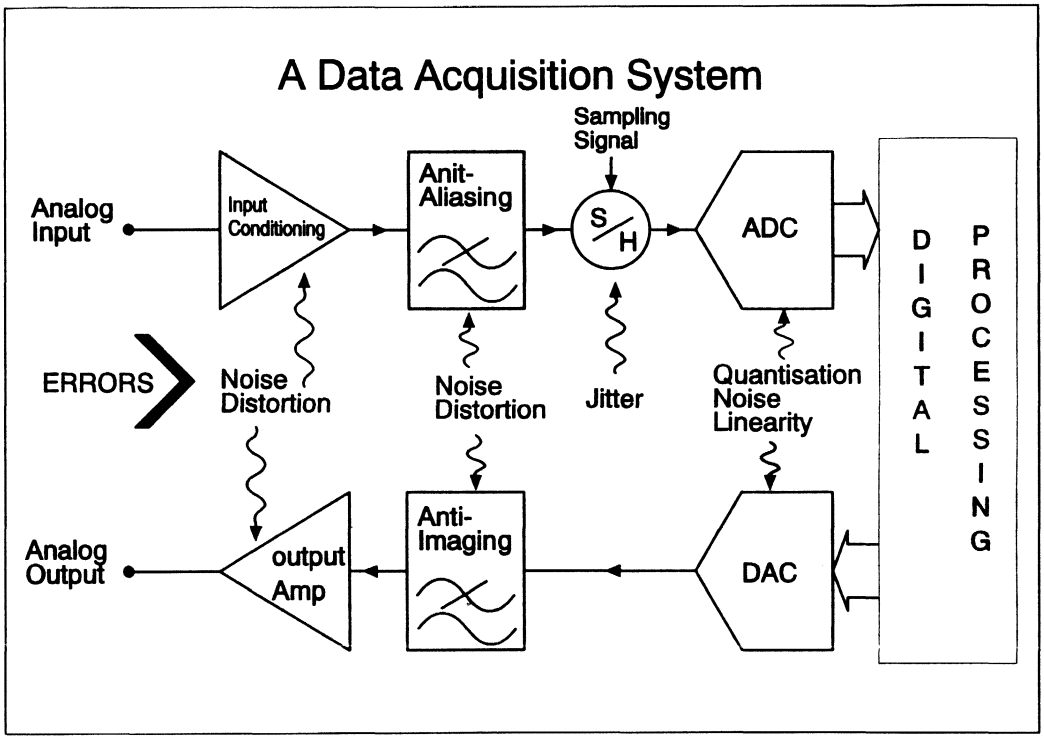


Figure 2.27 - A Data acquisition system

As for any system, a system to acquire data is made up of some key elements supported by secondary functions. The contribution made by each component to the performance of the system must be examined separately , if the performance of the whole is to meet its design goals.

The diagram shows the two basic elements which subdivide the system and convert the real world signals into the digital data for the processor. These are the Input/Output stage and the conversion stage.

4.1.1. Input/Output stage

The input/output stage to the system consists of an analog processing function. This can vary from simple a.c. coupling to remove large d.c. offsets, up to extensive frequency waveshaping to improve the dynamic range of the system.

Normally this analog processing is done with individual op-amps configured to give the required frequency response. since any signal must pass through the I/O stage to reach the conversion section, it is important to recognise that any noise or distortion introduced will become part of the signal that is

converted. Hence , the choice of components for the I/O stage is crucial to the satisfactory performance of the system as a whole.

The concept of bits of accuracy of an op-amp (as detailed in the signal conditioning section) is a useful one in this context. Using an op-amp that has the same bits of accuracy as the number of bits in the converter will introduce a 3dB loss in the SNR of the system . It is hence important to use low noise op amps with high input impedance for the input stage.

The trend to increased system integration means that this filtering is increasingly being carried out using integrated circuits that employ a switched capacitor technique. The benefits of switched capacitor filters in certain applications are numerous. They are easily programmed to give a certain response and track accurately because of good capacitor matching on chip. They provide a compact solution to filter design since large capacitors and inductors are not needed and small values in the range 5 to 20 pF are sufficient.

In summary, the design of the I/O stage is vital to the overall system. The techniques required have already been addressed in the signal conditioning section, and so apart from switched capacitor filters, will not be considered further here.

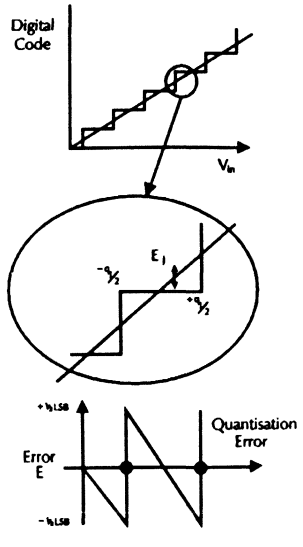
4.1.2. Conversion stage

The next part of the system is the true data-acquisition area which includes the ADC and the DAC. The choice is made here in terms of both resolution and accuracy and the method of conversion required as outlined earlier.

The nature of the quantisation process introduces distortion of the input signal, and the effect of sampling produces the phenomenon called Aliasing . Quantisation and aliasing are the first things we will consider now.

4.2. Quantisation effects

FINITE RESOLUTION QUANTISATION



Error at the jth step

$E_j = (V_j - V_{in})$

Mean square error over the step

$$\bar{E}_j^2 = \frac{1}{q_i} \int_{-\frac{q}{2}}^{+\frac{q}{2}} E_j^2 \, dE = q^2/12$$

Assuming equal steps, total error

$\bar{N}^2 = q^2/12$ (Mean square quantisation noise)

For an input sinewave $F(t) = A \sin\omega t$, signal power

$$\bar{F}^2(t) = \frac{1}{2\pi} \int_0^{2\pi} A^2 \sin^2\omega t \, d\omega t = \frac{A^2}{2}$$

and $q = \frac{2A}{2^n} = \frac{A}{2^{n-1}}$

$$SNR = 10 \log\left(\frac{\bar{F}^2}{\bar{N}^2}\right) = 10 \log\left(\frac{A^2/2}{A^2/3 \times 2^n}\right)$$

$SNR = 6.02n + 1.76$ dB

Figure 2.28 - Quantisation effects

The real world analog input to an ADC is a continous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analog signal that were represented by a different voltage on the input , are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is ***Quantisation noise***.

If we take an ideal staircase transfer function of the ADC, the error between the actual input and its digital form will have a uniform probability density function if the input signal is assumed to be random. It can vary in the range +/- 1/2 LSB or +/- q/2 where q is the width of one step.

$$p(\varepsilon) = 1/q \quad \left(-q/2 \le \varepsilon \le +q/2\right)$$

$$p(\varepsilon) = 0 \text{ otherwise}$$

The average noise power (mean square) of the error over a step is given by

$$E^2(\varepsilon) = \int_{-q/2}^{+q/2} p(\varepsilon)^2 \, d\varepsilon$$

which gives $E^2(\varepsilon) = q^2/12$

The total mean square error, N^2, over the whole conversion area will be the sum of each quantisation levels mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = q^2/12$$

Considering a sinewave input F(t) of amplitude A so that

$$F(t) = A \sin \omega t$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = 1/2\pi \int_0^{2\Pi} A^2 \sin^2(\omega t) dt$$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$SNR(dB) = 10Log\left[\left(A^2/2\right)/\left(q^2/12\right)\right]$$

But $q = 1LSB = 2A/2^n = A/2^{n+1}$

Substituting for q gives

$$SNR = 10Log\left[\left(A^2/2\right)/\left(A^2/3x2^N\right)\right] = 10Log\left(3x2^{n-1}\right)$$

$$\Rightarrow \underline{\underline{6.02n + 1.76dB}}$$

This gives the ideal value for an n bit converter and shows that each extra 1 bit of resolution provides approximately 6dB improvement in the SNR.

In practice, the errors mentioned in section 2 will introduce non-linearities that lead to a reduction of this value. The limit of a 1/2 LSB differential linearity error is a missing code condition which is equivalent to a reduction of 1 bit of resolution and hence a reduction of 6dB in the SNR. This then gives a worst case value of SNR for an n-bit converter with 1/2 LSB linearity error.

$$\text{SNR (worst case)} = 6.02n + 1.76 - 6 = 6.02n - 4.24 \text{ dB}$$

Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR.

4.3. Ideal sampling

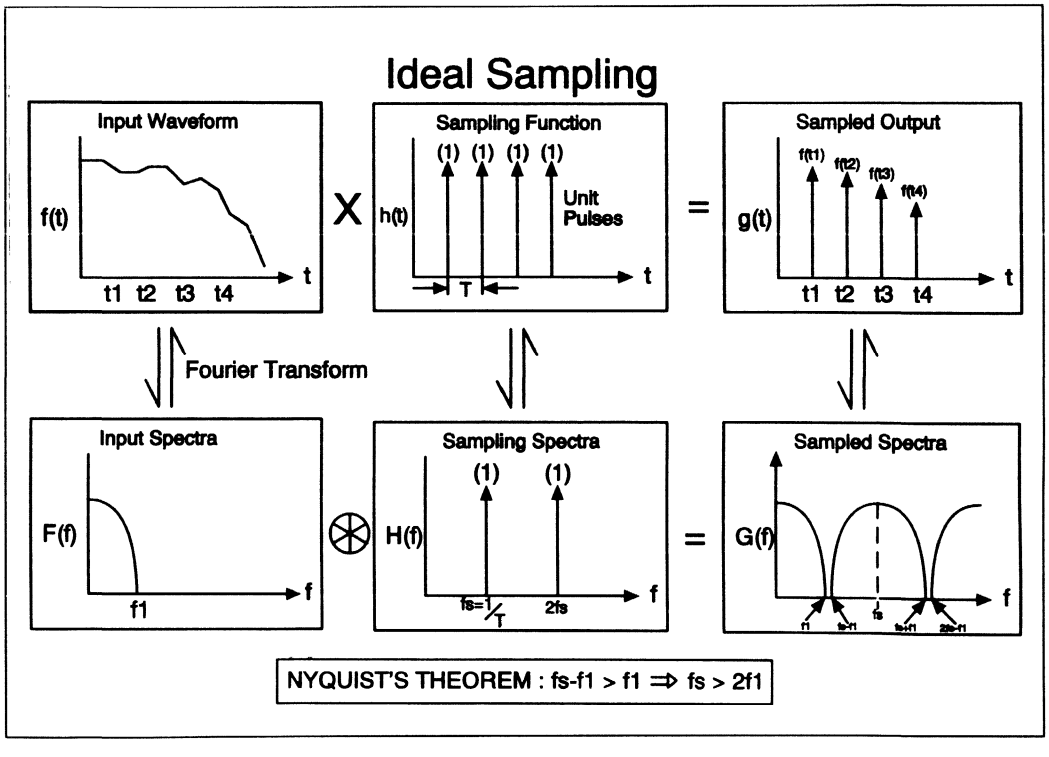


Figure 2.29 - Ideal sampling

In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, sampling takes the form of a pulse train of impulses

which are infinitessimally narrow yet have unit area. The time between each impulse is called the sampling rate. The input signal too is idealised by being truly bandlimited, containing no components in its spectrum above a certain value.

The ideal sampling condition is shown here, represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectra of the input signal with that of the pulse train to produce the combined spectrum shown , with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion which is called Aliasing.

If we assume the input signal is bandlimited to a frequency f1 , and is sampled at frequency f_S it is clear from the diagram that the overlap (and hence aliasing) will not occur if

$$f1 < f_s - f1 \qquad \text{ie.} \quad 2f1 < f_s$$

Therefore if sampling is done at a frequency at least twice as great as the maximum frequency of input signal, no aliasing will occur and all the signal information can be extracted. This is ***Nyquist's Sampling Theorem***, and it provides the basic criteria for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

4.4. Real sampling

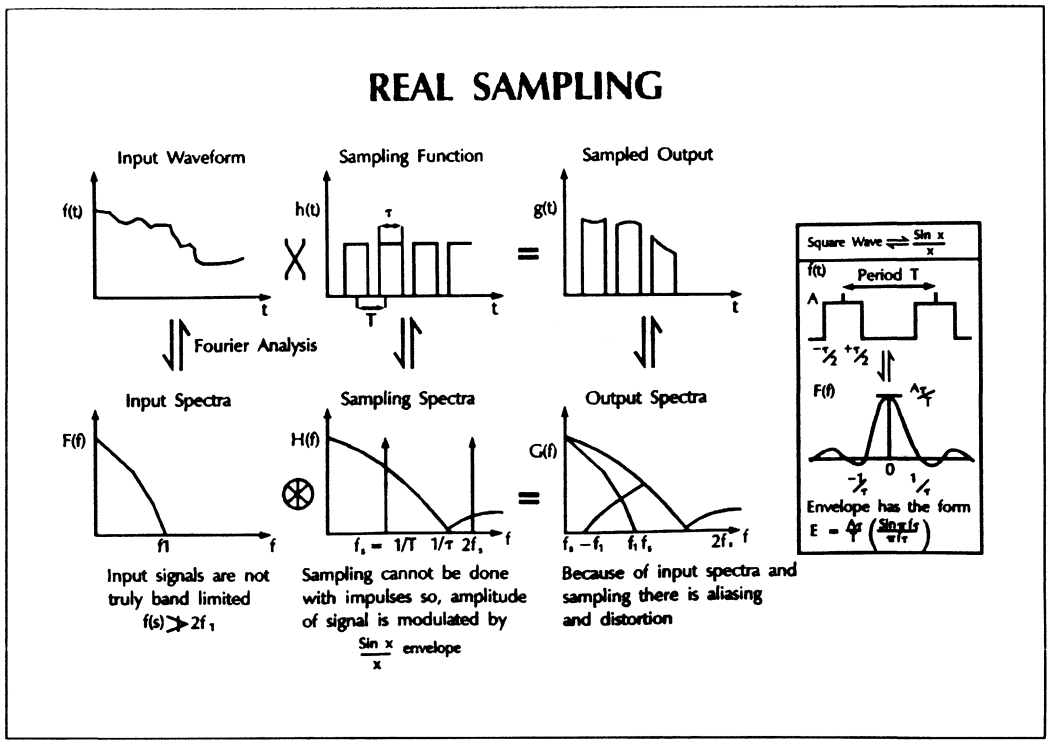


Figure 2.30 - Real sampling

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal will be a series of pulses of period equalling the reciprocal of the sampling frequency. The sample is acquired over a time t which is normally much smaller than the period T. The result of sampling with this pulse train is a series of amplitude modulated pulses.

Examining the spectrum of the square wave pulse train shows a series of discrete frequencies as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by sinx /x (sometimes written sinc(x)) where x in this case is πf_S. For a square wave of amplitude A, the envelope of the spectrum is defined as

$$Envelope = A(\tau/T)[\sin(\pi f_S \tau)] \ / \pi f_S \tau$$

This effect is minimised by ensuring that the sampling time is small in comparison with the sampling rate T.

It is also much more pronounced for DACs due to the fact that, with a DAC, the power output of the codes' widths are transferred to the output of the system. For maximum power in the signal out ,zero order hold DACs are used so that the pulse width normally lasts the whole sampled period. The error resulting from this can be controlled with a filter which compensates for the sinc envelope. This can be implemented as a digital filter, in a DSP , or using conventional analog techniques. (The TLC32044 Analog interface circuit featured in section 4 has an on-chip sinc correction filter after its DAC output for this purpose).

4.5. Aliasing effects and considerations

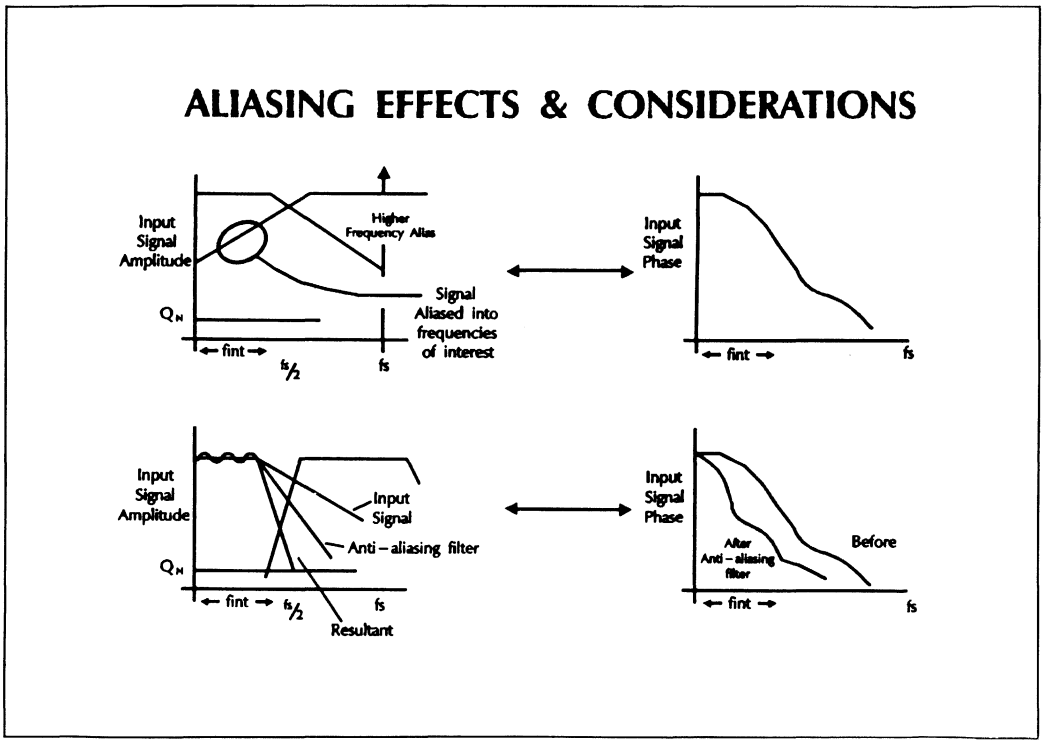


Figure 2.31 - Aliasing effects and considerations

No signal is truly deterministic and therefore in practice has infinite bandwidth. However, the energy of higher frequency components gets increasingly smaller so that at a certain value it can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As we have seen, the amount of aliasing will be affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution then the noise floor is already relatively high and aliasing may not have a significant effect. However,

with a high resolution system , aliasing may increase the noise floor considerably and therefore needs to be controlled more completely.

Increasing the sampling rate is one way to prevent aliasing, as we have seen. However, there will be a limit on what frequency this can be, determined by the type of converter used and also possibly by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analog filters must be used to alter the input signal's spectrum.

4.5.1. Choice of filter

Just as we have already seen with sampling , there is an ideal solution to the choice of filter and a practical realisation that has to make compromises. The ideal filter is a so-called brickwall filter which introduces no attenuation in the passband, and then cuts down instantly to infinite attention in the stopband. In practice , this is approximated by a filter that introduces some attenuation in the passband, has a finite rolloff , and passes some frequencies in the stopband. It may also introduce phase distortion as well as amplitude distortion. The choice of the filter order and type must be decided upon so as to best meet the requirements of the system.

4.5.2. Types of filter

The basic types of filter available to the designer are briefly presented here for comparison. This is not intended to be a full analysis of the subject and the reader should refer to other texts for more details.

Butterworth filter

A Butterworth (maximally flat) filter is the most commonly used general purpose filter. It has a monotonic passband with the attenuation increasing up to its 3-dB point which is known as the natural frequency. This frequency will be the same whatever the order of the filter is . However, by increasing the order of the filter, the roll-off in the passband moves closer to its natural frequency and the roll-off in the transition region between the natural frequency and the stopband becomes sharper.

Chebyshev filter

The Chebyshev equal ripple filter distributes the roll-off accross the whole passband . Hence, it introduces more ripple in the passband but provides a sharper roll-off in the transition region. This type of filter has poorer transient and stepping responses due to its higher Q values in stages of the filter.

Inverse Chebyshev filter

Both the Butterworth and Chebyshev filters are monotonic in the transition region and stopband. By allowing ripple in the stopband it is possible to make the roll-off sharper still. This is the principle of the Inverse Chebyshev, based on the reciprocal of the angular frequency in the Chebyshev filter response. This filter is monotonic in the passband, and can be flatter than the Butterworth filter whilst providing a greater initial roll-off than the Chebyshev filter.

Cauer Filter

The Cauer or (Elliptic) filter is non-monotonic in both the pass and stop bands, but provides the greatest roll-off in any of the standard filter configurations.

Bessel-Thomson Filter

All the types mentioned above introduce non-linearities into the phase relationship of the component frequencies of the input spectrum. This can be a problem in some applications when the signal is reconstructed. The Bessel-Thomson or linear delay filter is designed to introduce no phase distortion but this is acheived at the expense of a poorer amplitude response.

In general, the performance of all of these types can be improved by increasing the number of stages i.e. the order of the filter. The penalty for this of course is the increased cost of components and board space required. For this reason, it may be appropriate to use an integrated solution using switched capacitor filter building blocks which provide comparable performance with a discrete solution over a range of frequencies from about 1kHz to 100kHz They also provide the designer with a compact and cost effective solution .

TLC04 Anti-aliasing Butterworth filter

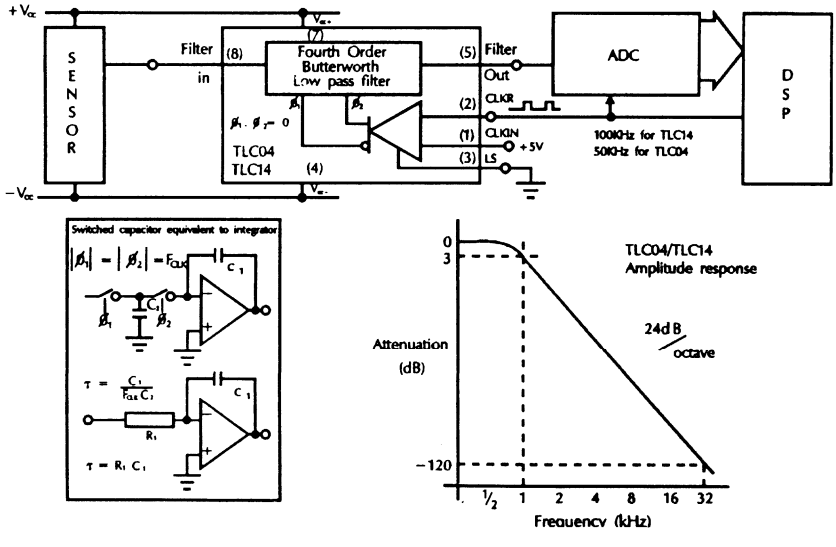


Figure 2.32 - TLC04 Anti-aliasing Butterworth filter

As detailed previously the Butterworth filter generally provides the best compromise in filter configurations and is by far the easiest to design. The Butterworth filter's characteristic is based on a circle which means that when designing filters, all stages to the filter will have the same natural frequency enabling simpler filter design. Most modern designs which use op-amps are based on building the whole transfer function by a series of second order numerator and denominator stages (a

Biquad stage). The Butterworth same natural frequency. This can easily be converted to a switched capacitor filter (SCF) which has very good capacitor matching and accurately synthesized RC time constants.

The Switched capacitor technique is demonstrated in the diagram. Two clocks operating at the same frequency but in complete antiphase, alternately connect the capacitor C2 to the input and the inverting input of an op-amp. During F1, charge Q flows onto the capacitor equal to VinC2. The switch is considered to be ideal so that there is no series resistance and the capacitor charges instantaneously. During F2, the switches change so that C2 is now connected to the virtual earth at the op-amp input. It discharges instantaneously delivering the stored charge Q.

The average current that flows Iav depends on the frequency of the clocks T so that

$$I_{AV} = Q/T = V_{IN} C_2/T = V_{IN} C_2 F_{CLK}$$

Therefore, the switched capacitor looks like a resistor of value

$$R_{eq} = V_{IN}/I_{AV} = 1/C_2 F_{CLK}$$

TLC04 Fourth order Butterworth filter

- **Low Clock to Cutoff frequency error ... 0.8%**
- **Cutoff depends only on stability of external clock**
- **Cutoff range 0.1Hz to 30kHz**
- **5V to 12V operation**
- **Self clocking or both TTL and CMOS compatible**

The advantage of the technique is that the time constant of the integrator can be programmed by altering this equivalent resistance, and this is done by simply altering the clock frequency. This provides precision in the filter design, because the time constant then depends on the ratio of two capacitors which can be fabricated in silicon to track each other very closely with voltage and temperature. Note that the analysis assumes Vin to be constant so that for an a.c. signal , the clock frequency must be much higher than the frequency of the input .

The TLC04 is one such filter which is internally configured to provide the Butterworth lowpass filter response, whose cut-off frequency is controlled by a digital clock. For this device, the cut-off frequency is set simply by the clock frequency so that the clock to cut-off frequency ratio is 50:1 with an accuracy of 0.8%.This enables the cut-off frequency of the filter to be tied to the sampling rate, so that only one fundamental clock signal is required for the system as a whole. Another advantage of SCF techniques means that fourth order filters can be attained using only one integrated circuit and they are much more easily controlled.

The response of an nth order Butterworth filter is described by the following equation.

$$Attenuation = \left[1 + {}^{f}\!/\!_{f_C}\, 2^{n}\right]^{1/2}$$

For the fourth order realisation in the TLC04, this corresponds to the table below.

frequency	**attenuation (factor)**	**attenuation (dB)**	**phase (deg)**
$F_C/2$	0.998	0.02	26.6
F_C	0.707	3	45
$2F_C$	0.0624	24	63.4
$4F_C$	0.00391	48	76
$8F_C$	0.000244	72	82.9
$12F_C$	0.000048	86	85.2
$16F_C$	0.000015	96	86.4

This means that sampling at 8 times the centre frequency gives an input to aliased signal ratio of 67dB, which is less than ten bit quantisation noise distortion.

The TLC10 as an antialiasing Cauer filter.

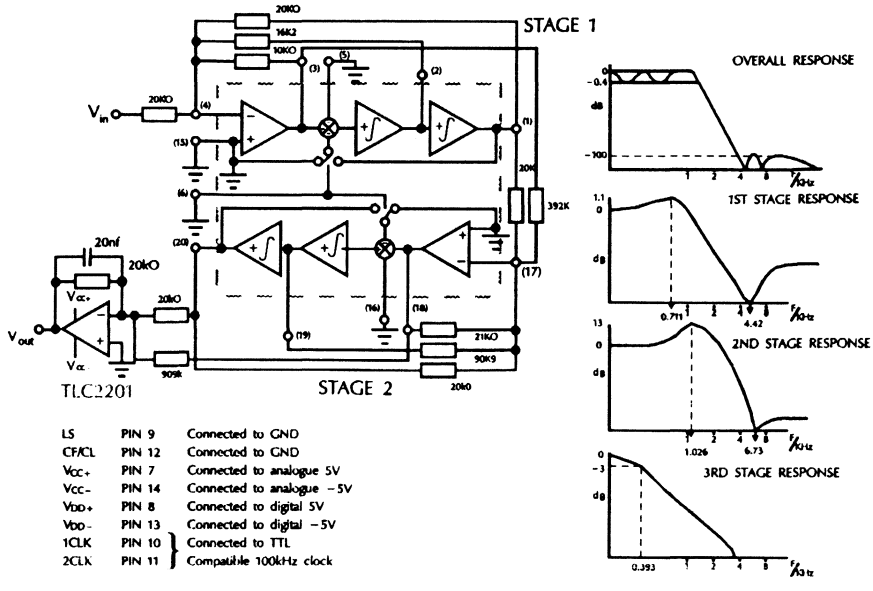


Figure 2.33 - The TLC10 as an antialiasing Cauer filter.

If a smaller roll-off in the passband and a faster roll-off in the transition region is required so that the signals aliased back into the passband are more attenuated, the Cauer filter can be used to provide this with a smaller order filter.

Switched capacitor filters can be used for this too. The TLC10 is a general purpose SCF building block that contains two independent active filter sections, each of which is designed to provide the response of a second order filter. These can be configured to produce any of the filter types listed in foil 20. In this example , it is configured to realise the Cauer filter configuration.

The Cauer filter has non-monotonic response in both the passband and the stopband. In this application , it is built up from two notch filters and a final low pass filter. The two halves of the TLC10 are used to build the notch filters which are realised as a combination of a low pass filter and a high pass filter . For the first stage, these two components are summed at the input of the second stage. Likewise, for the second stage, the high and lowpass functions are summed using an external summing amplifier built around the TLC2201. This also provides the benefit of further filtering so that the combination becomes a fifth order filter.

TLC10 Universal Dual Switched-capacitor filter

- **Low Clock to Cutoff**
- **frequency error ... 0.6%**
- **Cutoff depends only on stabílity of external clock**
- **Cutoff range 0.1Hz to 30kHz**
- **+/-4V to +/-6V operation**

As in most filters the lowest Q factor stage is placed first so as to minimise overshoot caused by high frequency elements in the input signal. To enable the op-amps to function properly and without excess distortion, the smallest resistor value is set to be 10k to minimise the current loading.

The fifth order Cauer filter shown is designed to have the following characteristics:

Passband ripple: 0.5 dB
Cut-off frequency: 1 kHz
Stopband frequency: 4 kHz
Stopband attenuation: 97.5 dB

The zeroes and poles are set in the following positions:

1st stage	f1=0.7112KHz	Q1=1.1403	Z1=4.4199
2nd stage	f2=1.0260KHz	Q2=4.4386	Z2=6.7342
3rd stage	f3=0.3933KHz		

4.6. Grounding techniques

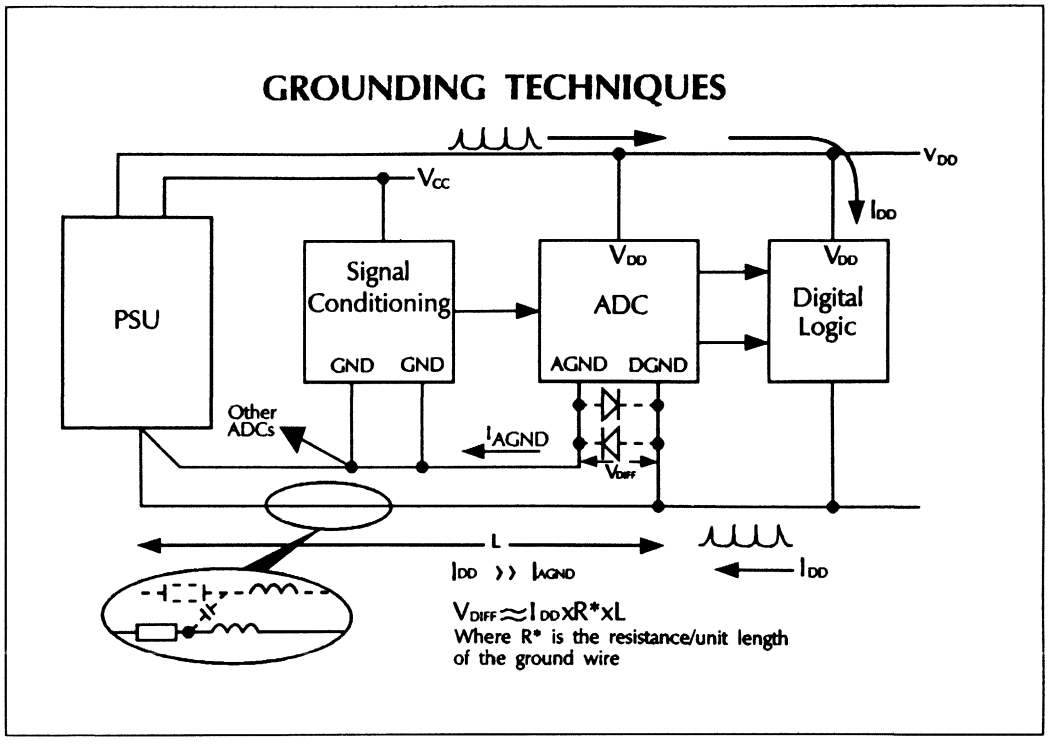


Figure 2.34 - Grounding techniques

One more area that needs careful consideration is the system of grounding used. It must be remembered that every wire or track on a PCB has a small but finite series resistance and inductance plus some equivalent shunt capacitance.

Principle: Think where the currents will flow!

In a mixed analog and digital system, it is likely that the digital processor and associated logic will draw the majority of the current . If the return paths for the digital and analog portions are linked into the same ground rail, the large dc current may cause significant "IR" voltage drops so that the voltage at the various ground points is different. In a high resolution converter such as the 10 bit TLC1540, 1/2 LSB at 5V reference corresponds to only 2.5mV, which can easily be exceeded.

Linking the digital and analog grounds together also introduces the possibility of current spikes from the high speed switching feeding through to the analog ground.It is therefore recommended as a minimum that the analog and digital grounds should be kept separate and should be terminated at the ground of the Power supply unit (PSU). Even better is to provide separate return paths for all currents , tied together only at a single analog ground reference point.

However, this causes a potential hazard in that the level of the analog and digital grounds at the ADC may be different. This creates the potential situation whereby the internal diodes may become forward biased and hence cause damage to the device. To prevent this, the analog and digital grounds at the ADC should be tied together using "nose on tail" diodes. This creates a maximum differential of 1 Vbe drop between the rails, or 0.4V if Shottky diodes are used.

5. Analog Interface Circuits for DSP Applications

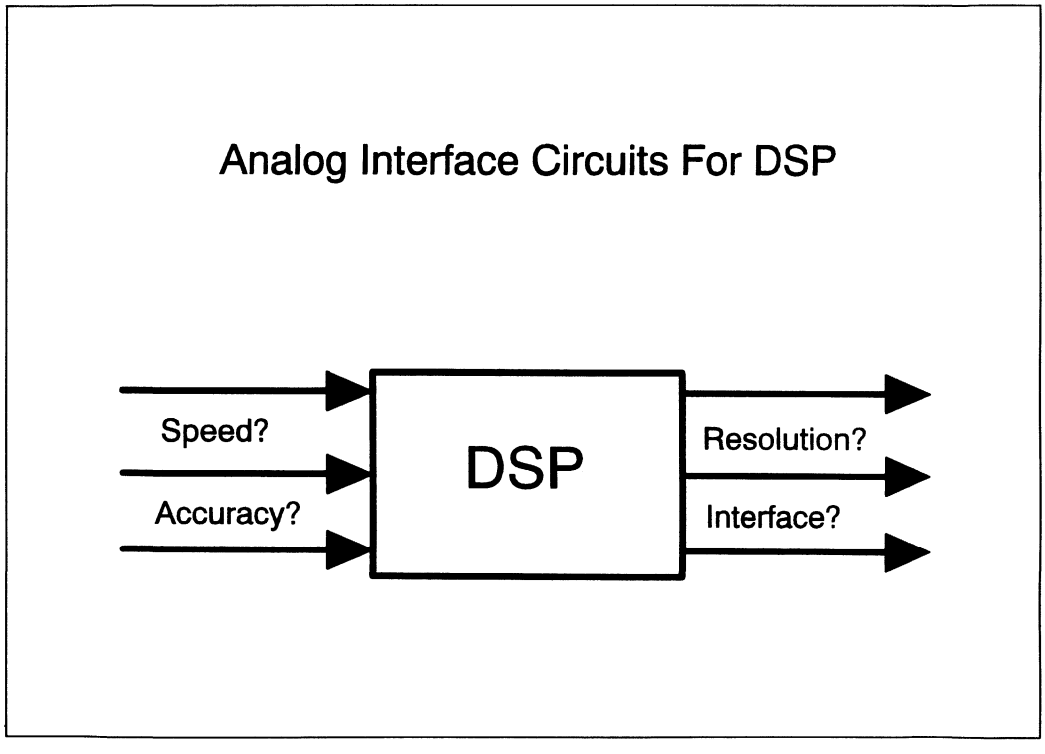


Figure 2.35 - Analog Interface circuits for DSP

This section looks at the growing area of applications using Digital Signal Processors (DSP) as the "intelligence" in process control. These applications clearly require an interface between the digital and "real world" analog signals. Texas Instruments has a number of devices designed to perform this task and they will be examined in the next few foils.

5.1. DSP in process control

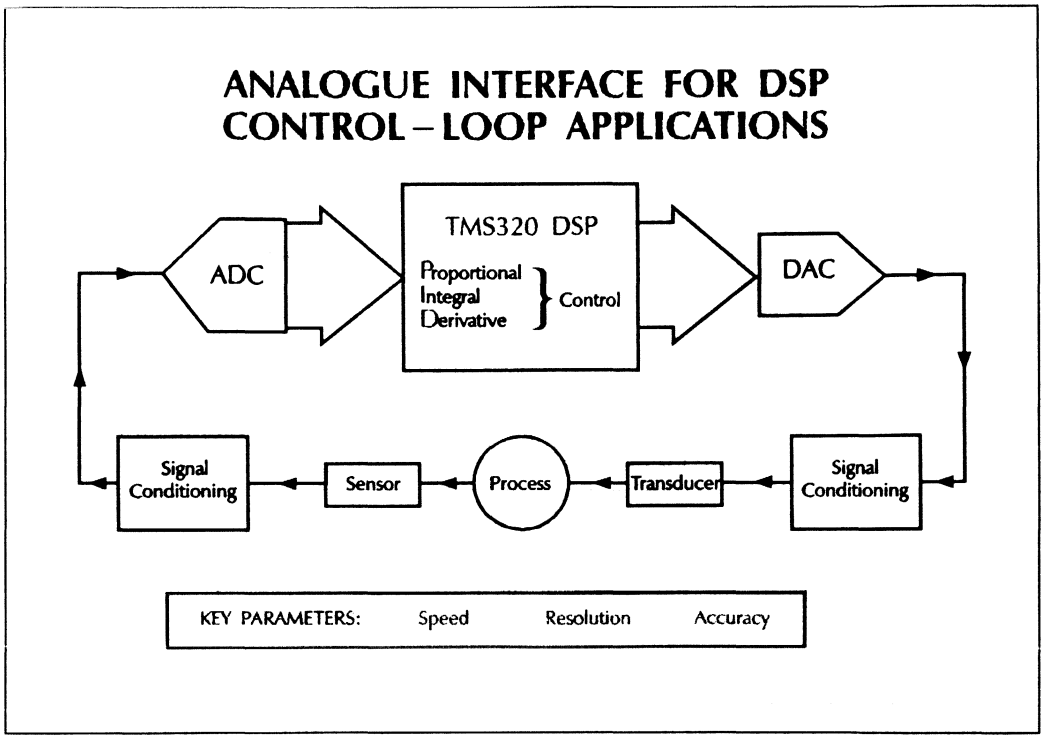


Figure 2.36 - DSP in process control

The use of a microcontroller or DSP as the core of a control system is a continuously growing field. As the cost of digital processing reduces, it becomes increasingly attractive for an increasing number of applications ranging from high speed digital processing for radar down to the control systems for white goods. To implement such applications , data conversion devices are required to capture data in its analog form and convert it to binary digits, and then to take the digital control outputs and convert them back to an analog signal to influence the process.

Such systems have requirements that impose conditions on the performance of the ADC and DAC; firstly there is the ability to capture data and make decisions in real time which dictates a certain minimum Speed requirement . The precision of control is decided by the Resolution of the converters and finally the accuracy of control is directly dependent on their Accuracy . These three parameters are the basis of any choice of converter for this type of application.

The diagram shows a system designed to operate using Proportional, Integral, Derivative (PID) control. In addition to the data conversion devices, there is a need for pre and post signal conditioning which usually takes the form of multiplexing, filtering and buffering the signals.

5.2. A Control System using the TLC1550 and TMS320C14

Electromechanical control systems are used in automobiles, appliances, industrial controls and many other systems. Today most control system designs are digital signal processor (DSP) based. A DSP based system, such as the one below, typically consists of one or more sensors, an analog-to-digital converter (ADC), a DSP and an actuator system.

DSP-based systems offer several advantages over conventional control systems. For example:

- **Replacing large look-up tables with mathematical equations reduces ROM requirements.**
- **Use of software models reduces the need for expensive linearized sensors.**
- **A DSP calculation result can be more accurate than a linear interpolation.**
- **The high processing power of a DSP enables use of advanced control algorithms.**
- **Using a DSP and a single ADC reduces the need for additional precision components.**
- **DSP implementation of real time system diagnostics can improve system reliability and reduce cost.**

To give design engineers the full advantage of a DSP-based approach, TI has designed the TMS320C14 DSP microcontroller and the TLC1550 10-bit ADC. These components can be used to simplify designs and increase performance.

TLC1550 A/D Converters

The TLC1550 features high speed (6 us conversion) combined with a 10-bit parallel data bus, making it possible to use a single ADC with multiple sensors. The parallel bus also allows for easy interface the the TMS230C14. The control system schematic includes the signal conditioning and multiplexing necessary to utilize multiple sensors.

TLC1550 / TMS320C14 System Benefits

- **Fast Operation**
- **Accurate control**
- **CMOS technology reduces system power requirements**
- **Design Flexibility**
- **Simple A/D & DSP Interface**

TMS320C14 DSP Microcontroller

The TMS320C14 combines a digital signal processor with microcontroller peripheral functions. The DSP core provides the processing power of a hardware multiply and 32-bit ALU. This processing power combined with a clock frequency of 25 MHZ makes possible the use of advanced control software. The peripheral functions provide interfaces to other system functions with a minimum of external components. This enables the TMS320C14 to be used in a variety of control applications.

The TLC1550 and the TMS320C14 are both implemented in CMOS technology, minimizing system power dissipation and requiring only a single 5V power supply. This further simplifies the design requirements for the system that follows.

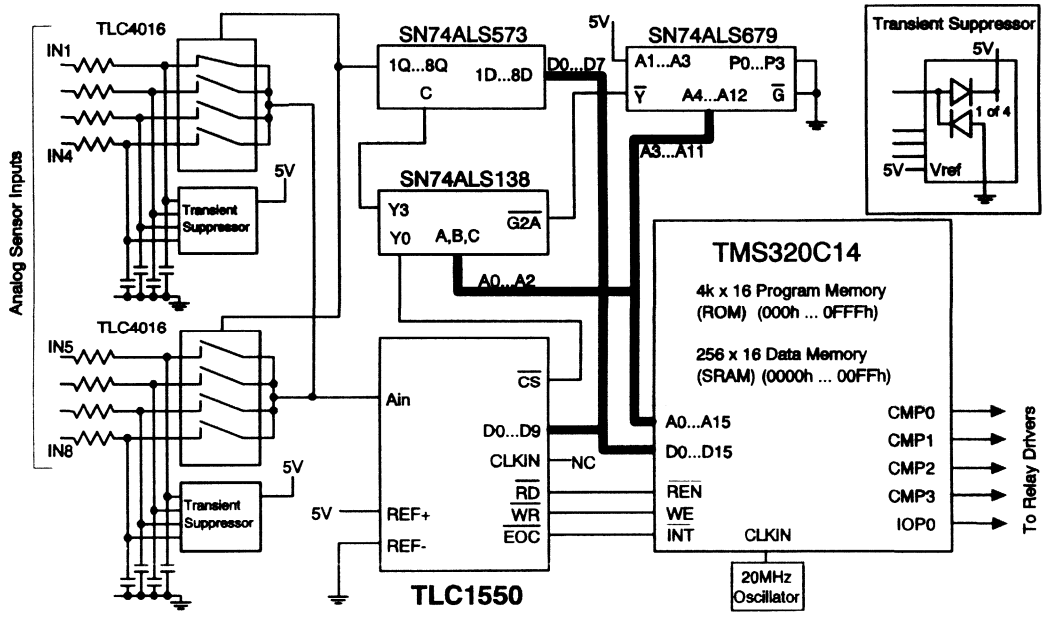


Figure 2.37 - TLC1550, TMS320C14 Control System

Design Considerations

Since most control applications require more than one analog input, two 4-channel analog switches (TLC4016) are interfaced as multiplexers to the analog input (A_{in}) of the TLC1550. The selection of one of these eight analog inputs is done via the transparent latch (SN74ALS573) with an OUT instruction to I/O port address PA3 and the appropriate data. Each of the eight analog inputs has a separate circuit for transient suppression and filtering. The resistor and capacitor network provide a simple low pass filter. The diode circuit labeled "transient suppressor" is used to conduct transients to ground or 5V, thus protecting the input circuitry.

The TMS320C14 can address the TLC1550 as an external memory. In order to use the simple IN and OUT instructions of the DSP-controller, the TLC1550 is mapped into the I/O port address range 1111 1111 1xxx. This is accomplished by simply decoding the 9 address lines (A3 - A11) using the SN74ALS679. The decoder output Y enables the 3-line to 8-line decoder SN74ALS138, to chip select CS of the analog-to-digital converter. In this configuration, the TLC1550 can be selected via I/O port PA0.

The write (WR) and read (RD) signals are only valid when CS is active low. An OUT instruction on PA0 sets CS low, permits sampling to begin with a WR low signal and initiates the hold mode with a WR high signal.

After entering the hold mode, the internal clock controls the conversion automatically. When the conversion is complete, the end of conversion (EOC) goes low, indicating that the digital data has been transferred to the output latch. Lowering CS and RD resets EOC and transfers the result to the data bus for the TMS320C14 read cycle.

Analog Channel Addressing

0000	0000	0000	0001	(1H)	=	Channel IN1
0000	0000	0000	0010	(2H)	=	Channel IN1
0000	0000	0000	0100	(4H)	=	Channel IN1
0000	0000	0000	1000	(8H)	=	Channel IN1
0000	0000	0001	0000	(10H)	=	Channel IN1
0000	0000	0010	0000	(20H)	=	Channel IN1
0000	0000	0100	0000	(40H)	=	Channel IN1
0000	0000	1000	0000	(80H)	=	Channel IN1

Channel Selection Routine

```
lack    4               ; load accumulator with 4
sacl    four            ;store 4 into four
out     portadr,bsr     ;select band FFFF (hex) - ports PA0 - PA6
out     four,PA3        ;select analog channel IN3
```

Note: To avoid analog I/P conflicts, only one logic high should be written to the octal D-latch.

A to D Conversion Routine via Polling

```
init    ldpk    0           ;
        larp    0           ;
        dint                ; disable all interrupts
sel     lack    1           ;load accu with 1
        sacl    one         ;store 1 into one
        zac                 ;clear accu
        sub     one         ;0000h-0001h=FFFFh
        sacl    portadr     ;FFFFh->portadr
        out     portadr,bsr ;select bankFFFFh (ports pa0 - pa6)
        out     one,pa3     ;select analog channel IN1
        nop                 ;these nop instructions
        nop                 ;allow the I/P voltage
        nop                 ;to settle
conv    out     dummv,pa0   ;start conversion
        call    wait        ;
        in      advalue,pa0 ;read conversion result
        lac     mask        ;load mask 03FF for 10 bits
        and     advalue     ;mask conversion result
        sacl    advalue     ;store 10-bit conversion result
        b       conv        ;
wait    lark    0,value     ;
wait l  nop                 ;delay loop of 6us to allow conversion
        banz    wait l      ;
        ret                 ;
```

5.3. An ADC for ABS systems

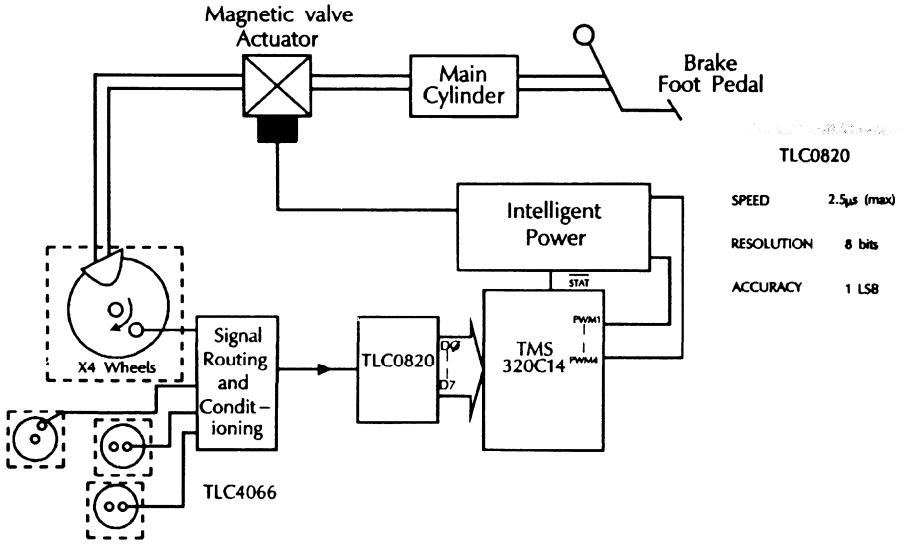


Figure 2.38 - An ADC for ABS systems

DSP solutions are being increasingly used in automotive applications. These include engine management, active suspension and the system featured here - an Anti-lock Braking System (ABS). The automotive environment is electrically very noisy and the need for a high speed ADC is evident to ensure there is sufficient oversampling to extract the real signal from the noise. The basis of the ABS system is to ensure the wheels never go into a skid condition by monitoring their speed when the foot pedal applies the brakes, and alternately applying and releasing the brakes under the control of the DSP . In this way, the wheel is prevented from locking up in a skid condition.

The speed of each wheel is monitored by a sensor that produces a pulse train in the range of 0 - 5kHz depending on the rotational speed. All four channels are routed together via a TLC4066 multiplexer which selects each signal in turn to pass to the ADC. High frequency noise is then removed by a Bessel LP filter which preserves the phase relationship of the signal. It is then fed to the TLC0820 ADC which converts the signal into 8 bit words . The primary factor in choosing this part is the speed of conversion required. In order to correctly reconstruct the underlying signal it is desirable to oversample at least 4 times. Hence, for 4 multiplexed signals operating up to 5kHz this gives:

$$4x5kHz\ x4 = 80kHz \Rightarrow 12.5\mu s \text{ CONVERSION TIME}$$

The TLC0820 has a semi-flash architecture which provides a conversion time of just 2.5uS max, so that it can operate in this system at up to 16 times oversampling if required. The semi-flash construction also provides a device with power consumption of just 75mW.

TLC0820 semi-flash ADC

- **Conversion time 2.5uS max**
- **8-bit resolution**
- **Total unadjusted error 1 LSB**
- **Single rail 5V supply**
- **Low power consumption .....50mW typ**
- **Differential reference inputs**

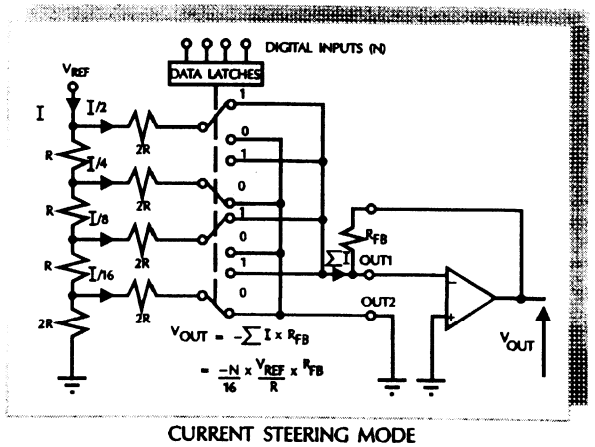
Once converted, the binary data is processed by an advanced tracking filter in the DSP. This filter "tracks" the frequency of the input , to correlate it with an ideal pulse train at a particular frequency. In this way, it provides a "perfect" bandpass filter to determine the frequency and hence the speed of the wheel. Deviations from the desired control model are then measured and an output of PWM pulses is produced to control the length of time for which the brake should be applied. These are interpreted by intelligent power devices which provide the drive for the valve actuators that actually apply the brakes.

5.4. TLC7524,TLC7528,TLC7628 Multiplying DACs

TLC7524 – SINGLE DAC
TLC7528 – DUAL DAC
TLC7628 – DUAL DAC

- 100ns Settling time
- 5V to 15V Operation
- Data set up times ‹40ns – Direct DSP Interfacing
- Guaranteed voltage mode operation

TLC7524 SCHEMATIC



CURRENT STEERING MODE

Figure 2.39 - TLC7524,TLC7528,TLC7628 Multiplying DACs

Many microprocessors operate with instruction cycle times that are too fast for direct interface to data converters. This necessitates the use of buffer logic with increased costs in devices required and in board area used. The TMS320C25 with a 10MIPS rate (100nS instruction cycle time) is one such example of this. The TLC7524 DAC provides a solution to this problem with a settling time to 1/2 LSB of just 100nS. It can also be operated from a single 5V supply with a power dissipation of only 5mW.

The TLC7524 is a multiplying DAC fabricated in CMOS technology. The term "multiplying" comes from the fact that the value of the output is proportional to the input reference voltage multiplied by fraction of full scale represented by the input digital code. It uses an inverted R-2R ladder to steer current from the reference input to the output via switches controlled by the digital input bits. This current output is changed to a voltage by an external op amp configured as a summing amplifier. However, this inverts the signal, so that this mode of operation requires a dual supply .

Also available in this family of devices are the TLC7528 dual DAC and the TLC7628 which is intended for applications running from a 15V supply but still requiring TTL level digital signals. Both feature excellant DAC to DAC matching so that they track together precisely.

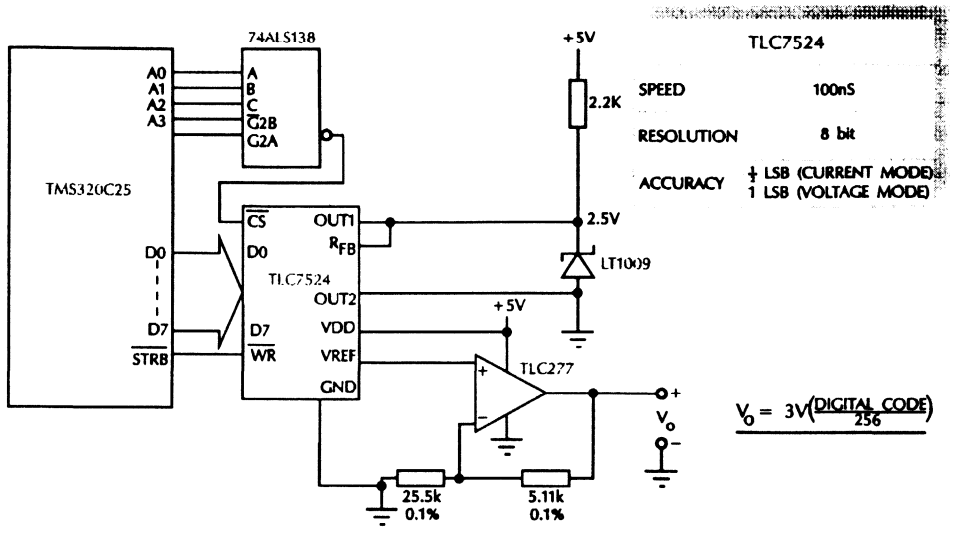


Figure 2.40 - TLC7524 - Voltage mode operation with DSP.

Single supply operation can be achieved by operating in voltage mode as shown here. In this configuration, the reference voltage is applied to the output pin OUT1 and the output is taken from the usual input pin V. In this mode of operation, the output is a voltage with the same polarity as the input so that single supply operation is possible.

TLC7524 multiplying DAC

- **Settling time to**
- **1/2LSB....100nS max**
- **8-bit resolution**
- **Linearity error 1/2 LSB**
- **Single rail 5V to 15V supply**
- **Low power consumption .....5mW max at 5V**
- **Guaranteed voltage mode operation**

There are some points to note in this mode. Firstly, the impedance seen by the input voltage is not constant, but varies depending upon the input code. Therefore it is sometimes necessary to buffer the input with a voltage follower. In this case , the output impedance of the LT1009 is less than 1ohm so

that it is not overloaded even under worst case conditions when the input impedance is 5k ohm. The LT1009 is chosen here for its high precision and low drift . Its initial tolerance is +/-5mV at 25^{o}C on a nominal reference of 2.5V, which is equivalent to 1/2 LSB.

Secondly, the switches in the DAC no longer have the same source-drain voltages, and as a result their on-state resistance is altered. This degrades the linearity of the part from the 1/2 LSB normally specified. Nevertheless, the device is guaranteed to meet 1 LSB linearity for an input of 2.5V at 5V VDD .

The output is buffered and amplified by the TLC277 op amp which is chosen for its offset voltage of just 500uV max. The resistor chain provides sufficient gain to boost the output swing to 0V to 3V.

5.5. The TLC3204X family of Analog Interface Circuits

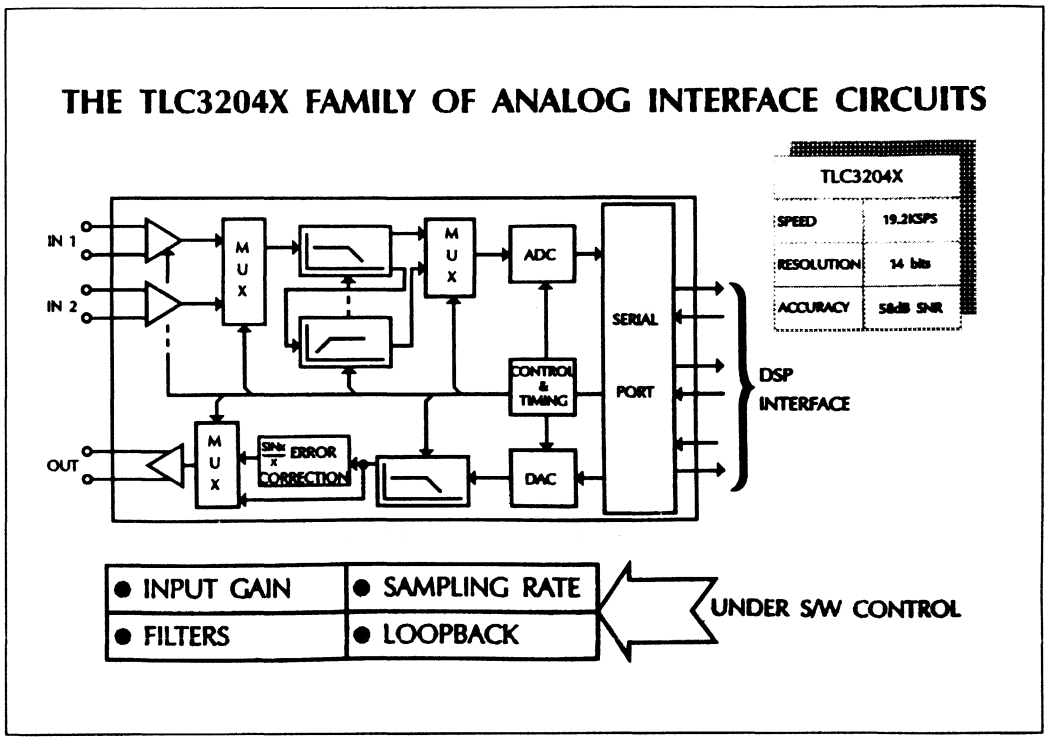


Figure 2.41 - The TLC3204X family of Analog Interface Circuits (AIC)

One of the largest users of DSP based applications is in the Telecom segment of the market. This segment has clearly defined limits for the frequency of operation , with the audio bandwidth of up to 4kHz being the usual range of interest for the analog signals.

To address the needs of this market, Texas Instruments developed the TLC3204X family of devices to provide the complete analog interface for DSP in a single chip. All five members of the family are highly integrated with A/D, D/A, pre- and postfilter stages and an input/output stage on-chip. They have been developed mainly for high performance voiceband system applications which require high resolution, a high degree of programmability , and an integrated design that conserves board space.

5.5.1. AIC building blocks

The AIC is divided into a transmit and a receive section which are controlled from a central timing block. On the receive side, an analog signal is fed into either a main or auxilliary fully differential input which are selected by a multiplexer. The input stages have programmable gain so that the signal level can be optimised for maximum resolution. It is then passed to an antialiasing filter consisting of a LP followed by an optional HP which can be selected or bypassed as required. These are both

switched capacitor filters (SCF) driven from a sub-multiple of the central master clock. This frequency is nominally set to 288kHz and all the datasheet specifications are derived from this value, but it can be easily altered to adjust the corner frequencies of the filters.

The ADC itself is also driven from a further sub-multiple of the same clock which ensures the sampling is synchronised with the SCF filter. The sampling rate is programmable up to 19.2kHz , and encompasses the standard modem sampling rates (7.2kHz, 8.0kHz, 9.6kHz , 14.4kHz). The output from the ADC is a 14 bit word which is then passed out of a serial port to a DSP.

In the transmit section, data and control information is transferred from the DSP into the DX pin of the serial port. This is transmitted to a 14 bit DAC which is controlled in the same way as the ADC. The sampling rate for both can be tied together in Synchronous operation but they can be run independently in Asynchronous mode. The output from the DAC is fed to a LP SCF and then to a sinx/x correction filter . It is finally transmitted out of a differential output buffer.

TLC3204X AIC

- **14 bit ADC and DAC**
- **Programmable sampling rates up to 19.2kSPS**
- **Programmable switched capacitor filters**
- **Direct serial interface to DSP**
- **Synchronous and Asynchronous operation**

The advantage of using the AIC in a system design , is the degree of flexibility that results because parameters can be controlled by software and do not require costly hardware modifications. Applications like FAX and secure telephony both dictate a high speed data rate with low bit error rate figures (BER). This in turn demands a flexible system with high resolution. Both these parameters are met by the AIC with its 14-bits of resolution and up to 19.2 Ksamples/s data rate.

5.5.2. Interfacing the AIC to the TMS320 DSP

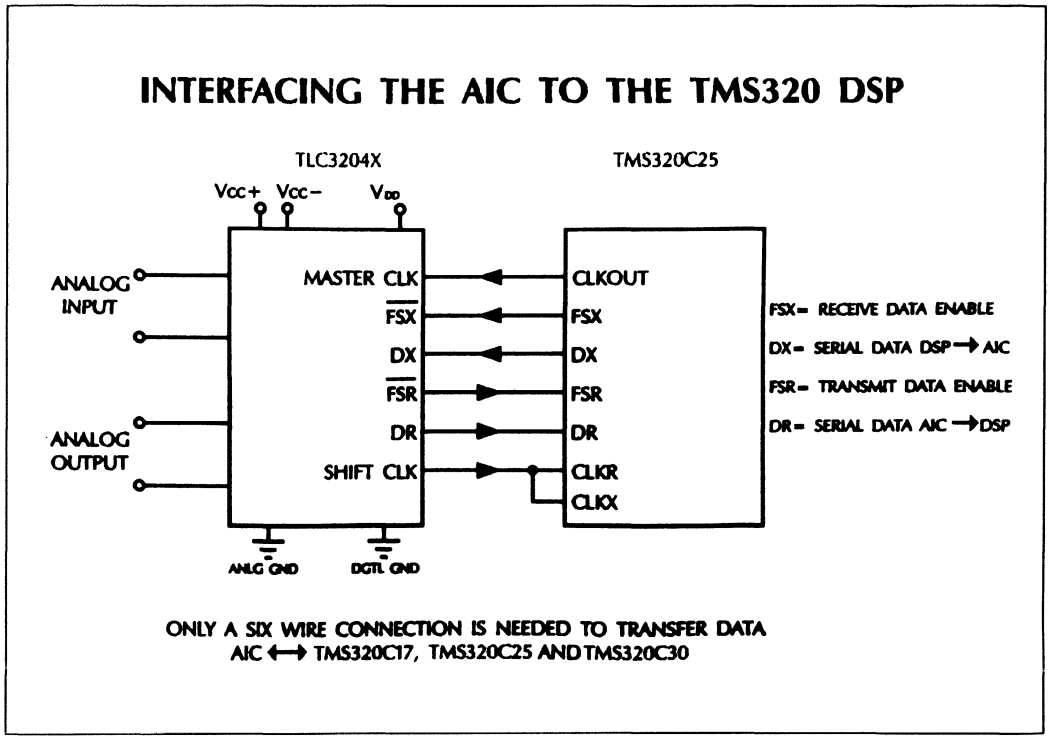


Figure 2.42 - Interfacing the AIC to the TMS320 DSP

The interfacing part of the AIC is built on a serial data format concept aimed at interfacing the device directly to the serial I/O of the TMS320C25 digital signal processor. As such, the core of the system consists of these two chips alone, rather than being supplemented by a number of interface devices commonly found in many applications.

The intercommunication between the AIC and the DSP is based on just six lines. These are outlined in the following list:

MASTER CLK : The AIC is built on a single master clock input which is divided by the contents of control registers to determine the conversion rates and filter characteristics.

FSX : Initiates the AIC to prepare for a data transfer from the host processor.

DX : When the FSX has initiated the AIC,a transfer of data will take place to the AIC from the host along this line.

FSR : Initiates the serial input of the host to receive output data from the AIC.

DR : When the FSR serial input has been activated, the AIC will transfer data from the A/D to the host along this line.

SHIFT CLOCK : Dictates the speed of data transfer between the AIC and the host.This clock shifts the data into and out of the AIC.

6. Video Interface Palettes

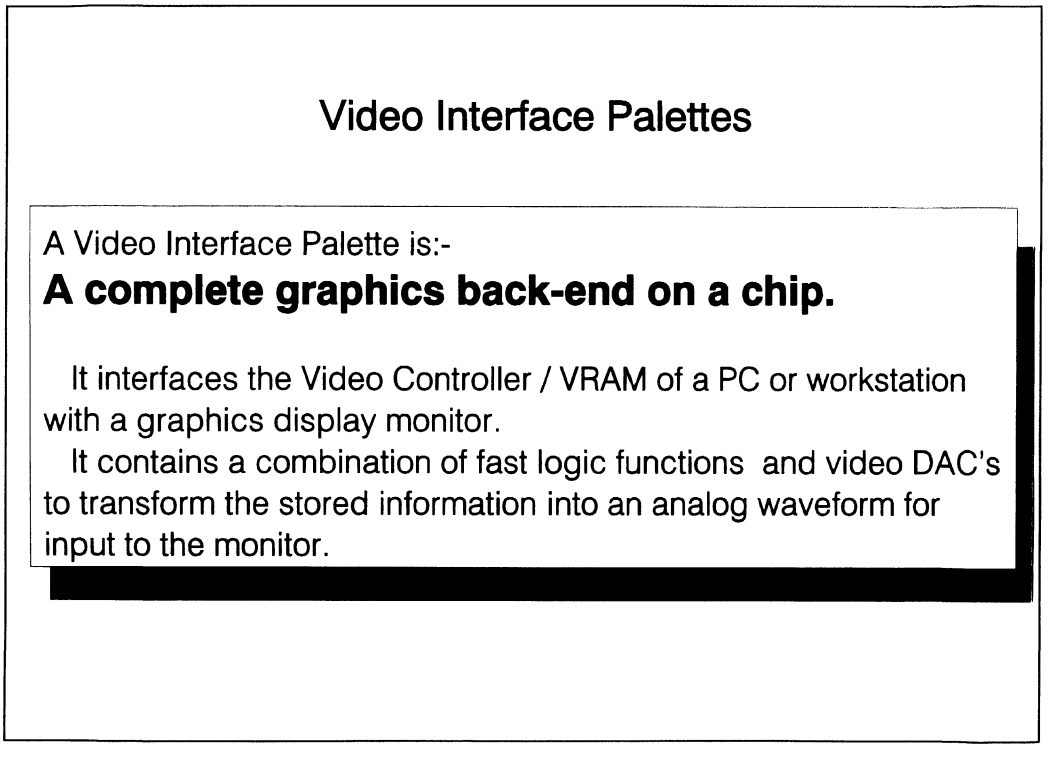


Figure 2.43 - Video Interface Palettes - Introduction

6.1. Introduction

Today's computer systems make an ever increasing use of graphics, both in the user interface (eg. Windows TM[1]) and in the applications S/W such as desktop publications, CAD, etc. In order to service these requirements, high resolution monitors are required together with the circuits that drive them.

[1] **Windows is a trademark of the Microsoft corporation**

6.2. Image Composition

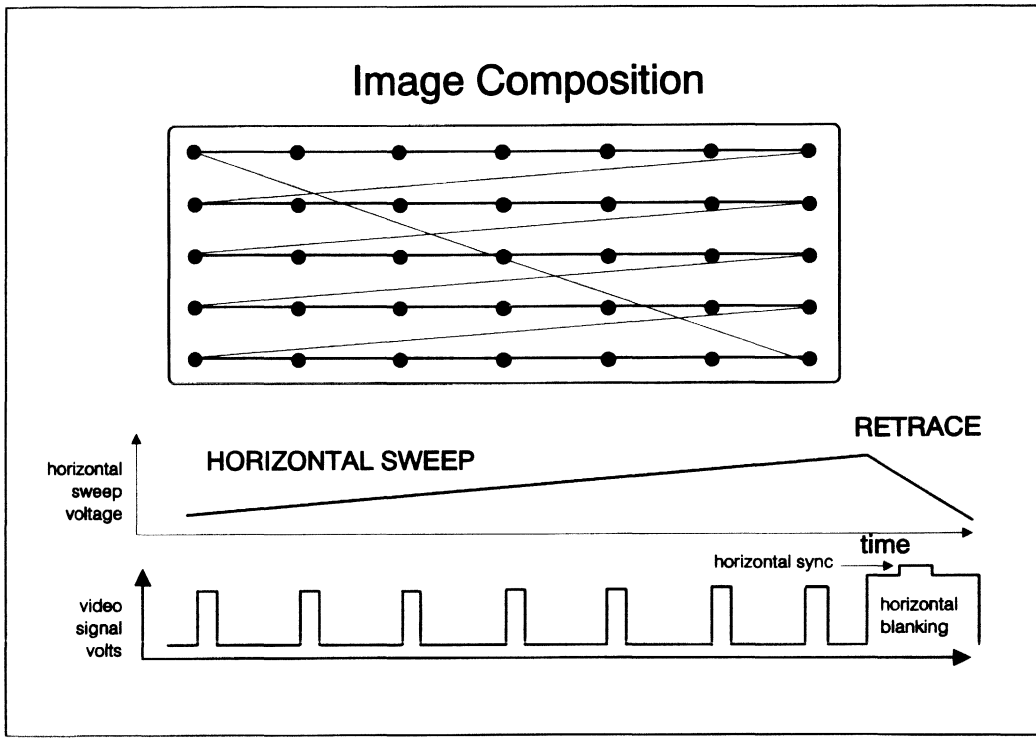


Figure 2.44 - Image Composition

An image is made up from individual picture elements (pixels). Images are formed on a CRT screen when the electron beam sweeps horizontally across the screen and vertically down, illuminating the pixels one at a time, until it has swept through the entire array. Return of the beam from right to left occurs during the horizontal retrace time and from bottom to top during the vertical retrace time. During the retrace time the screen is blanked by horizontal and vertical blanking pulses. This horizontal and vertical sweeping of the beam is called raster scanning. It is the most widely used display method and facilitates the use of bit-mapped graphics.

The Hsync and Vsync pulses, which occur during the appropriate blanking period, assure the proper beam start position for each scan. During the beam scanning, the individual pixel data is sequentially timed with the beam position by the pixel clock so that the image appears in the proper position on the screen.

Each pixel is made up from red, green and blue intensity information, and a color monitor, typically , has inputs for each of these. The inputs drive 3 separate electron guns which illuminate the appropriate color phosphor at the appropriate time, determined by the sync signals. By varying the intensity of each

of these primary colors, any secondary color can be obtained. (Equal red, green and blue intensities would produce white to gray, depending on the overall intensity of the signals applied).

6.3. Graphics Display System

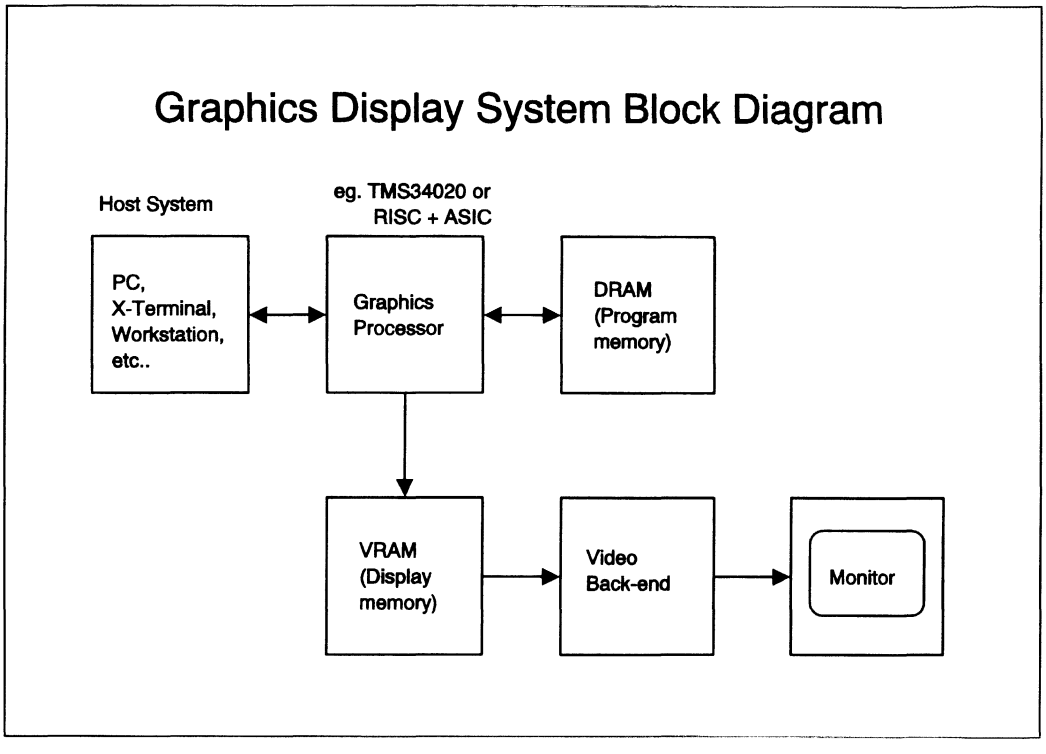


Figure 2.45 - Graphics Display System Block Diagram

The generation and manipulation of bit-mapped images in memory is the primary function of a Graphics Display System. A graphics processor carries out the routine display tasks by handling the data updates, bit manipulation and synchronising functions for the screen display. This relieves the host system processor of these functions, making the overall system much faster. A typical graphics display system consists of:

- **Graphics processor**
- **Program memory**
- **Display memory**
- **Video back-end**
- **Display monitor**

There are two ways to handle the graphics processor: Either use a hardware engine by getting the parameters from the host processor, or use a dedicated high speed graphics processor, such as the TMS34020. The Graphics processor is the graphics front-end and will not be considered further here.

The video interface for driving a monochrome display is typically a DAC to change the stored digital data into analog voltages to drive the CRT. When a color display is used , the display interface is known as a "Color Palette" or "Video Interface Palette" (VIP) and it performs many more functions than a DAC.

6.4. Graphics Back-End Functional Blocks

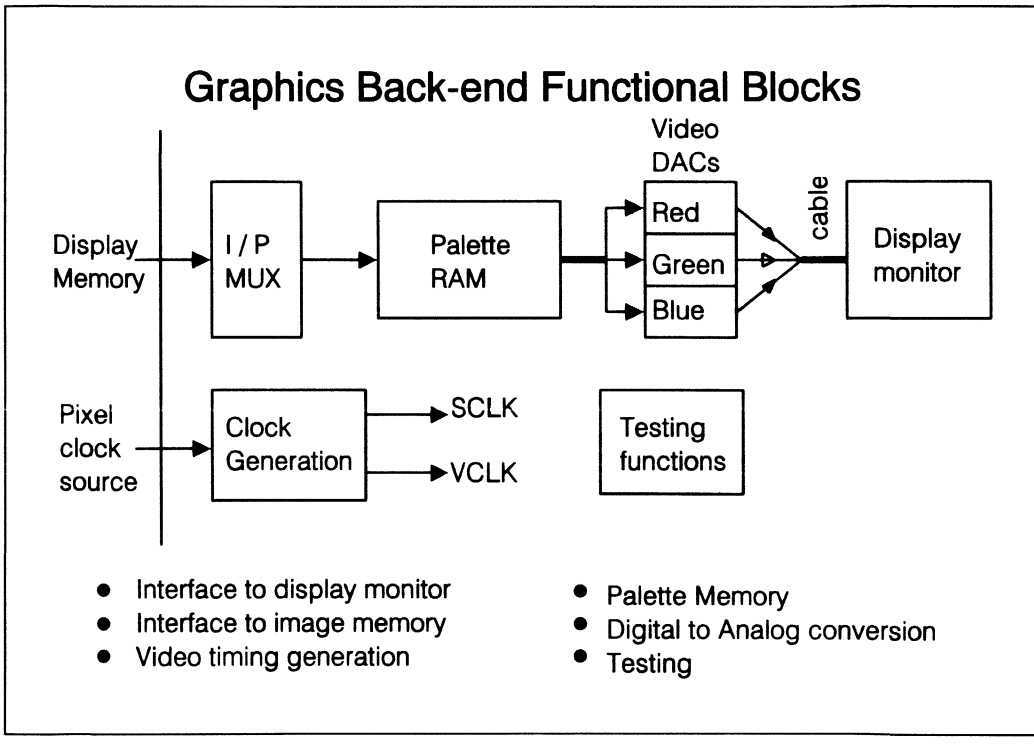


Figure 2.46 - Graphics Back-End Functional Blocks

The graphics back-end is defined as the circuitry between the memory and the display monitor and consists of the following functional blocks:

- **Interface to the display monitor**
- **Interface to the display memory**
- **Video timing generation**
- **Palette memory**
- **Digital-to-analog conversion**
- **Testing circuitry**

6.5. A Complete Graphics Back-end on a chip -- The TLC34075

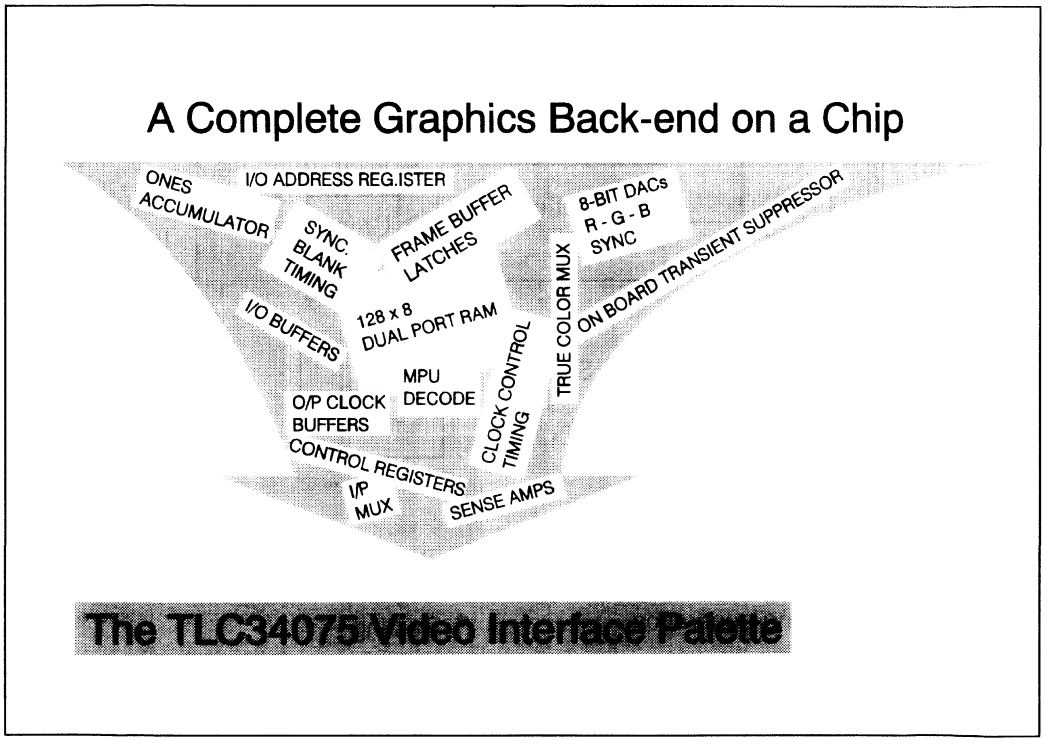


Figure 2.47 - A Complete Graphics Back-end on a chip - The TLC34075

The TLC34075 combines all these functions onto a single chip which interfaces directly to the Graphics Processor, the VRAM display memory and the display monitor.

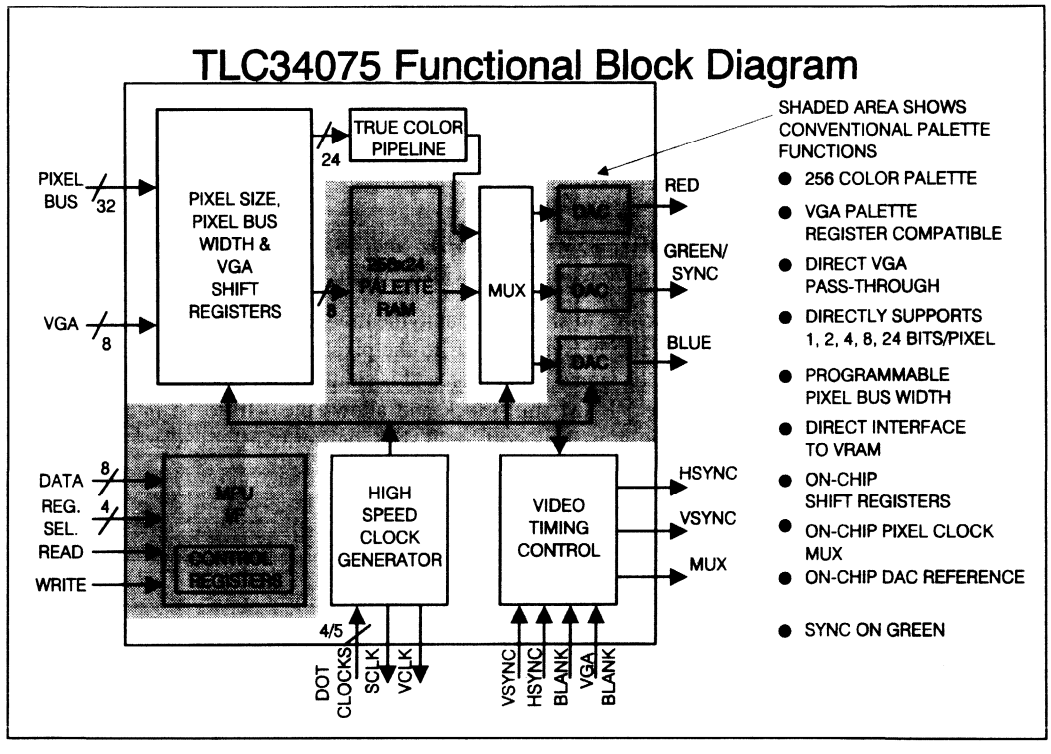


Figure 2.48 - TLC34075 Functional Block Diagram

High resolution displays such a VGA and beyond use 8 bits per color for intensity data. The 256 x 24 bit palette RAM within the TLC34075 allows upto 256 colors to be resident at any one time with the 24 bits being composed of 8 bits each of red, green and blue data. This means that over 16 million (2^8 x 2^8 x 2^8) colors are available, 256 at a time. The 256 colors chosen are downloaded by the host depending on the application.

Over the years IBM VGA (Video Graphics Array), which has a resolution of 640 x 480, has dominated the overall graphics board design. However, as the technology advances, and with the introduction of IBM XGA, resolutions of 1024 x 768 and higher become the general design target.

There is also a requirement for higher refresh rates, to eliminate the annoying flicker effect. The current European Community standard is 72Hz, but more designers are now considering 76Hz as promoted by SUN Microsystems.

This combination of high resolution and high refresh rate demands a very fast pixel clock.

6.6. Calculation of Required Pixel Clock Frequency

The required pixel clock frequency is determined by the resolution and refresh rate of the system. It is given by:

$$f_{pixel} = (N^{o} \text{ of pixels per line }) \times (\text{No of lines per frame}) \times (\text{refresh rate}) \times 1.25$$

The last term allows an extra 25% for blanking during horizontal and vertical retrace.

eg. for a 1024 x 768 resolution display at 72 Hz refresh rate, the pixel rate would be:

$$f_{pixel} = 1024 \times 768 \times 72 \times 1.25 = 71\text{MHz (approx)}$$

The TLC34075 is available in 66MHz, 85MHz, 110MHz and 135 MHz speed versions and the TLC34075-85 (85MHz) satisfies the above requirement with a reasonable safety margin.

Pixel clock is the fundamental clock source to shift data out to the monitor through the DACs. All other data path and video control logic have to be synchronous to the pixel clock but at lower frequencies. $\mathbf{V_{clk}}$ is typically used for sync and blank signal generation and is simply pixel clock divided by 1, 2, 4, 8, 16 or 32 plus disable. Sclk is the VRAM shift clock and allows the VIP to be interface to the VRAM without any external glue logic. It will support "split shift register transfer cycles" which allow more efficient use of the VRAM.

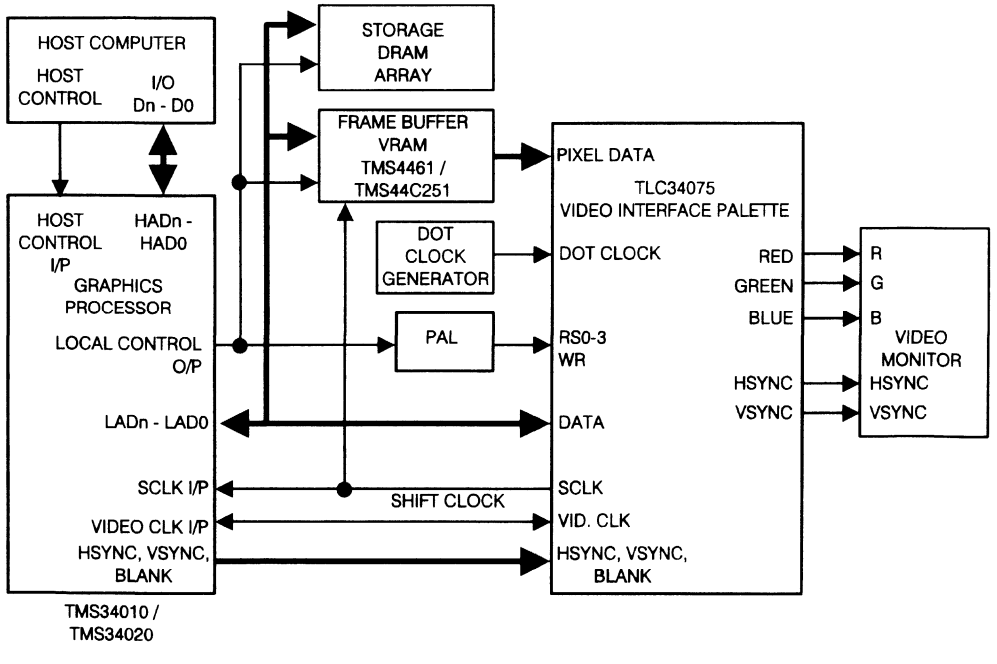


Figure 2.49 - Color Graphics System Block Diagram

This shows the simple interface between the TLC34075 and TMS34010/20 and VRAM.

6.7. Color Depth and Memory Size Relationship

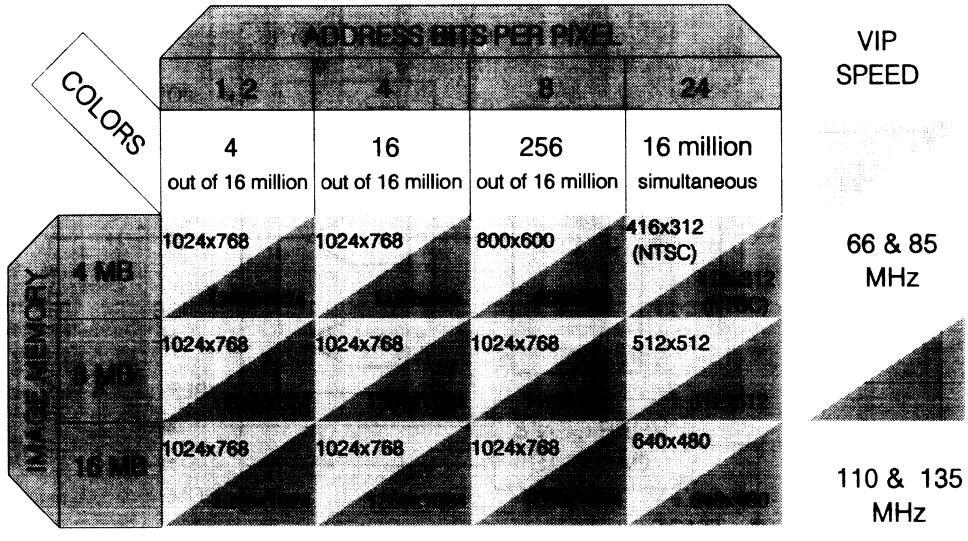


Figure 2.50 - Color Depth and Memory Size Relationship

The TLC34075's various pixel multiplexing options allow for 32, 16, 8 and 4 bit pixel bus widths to be accommodated without any circuit modifiactions, enabling the system to be easily reconfigured for varying amounts of available video RAM. A palette page register provides additional bits of palette address when 1, 2 or 4 bit transfers are used, allowing screen colors to be changed with only one MPU write cycle. A true color mode transfers 24 (3x8) bits of color information directly to the DACs, the remaining 8 bits of the Palette's 32-bit bus being available for an overlay function.

The device features a separate VGA bus that allows data from the feature connector on a PC to be taken directly to the palette without the need for any external multiplexing. This allows a replacement graphics board to remain downwards compatible by using the existing graphics circuitry which is often located on the mother-board.

6.8. TLC34075 Analog System

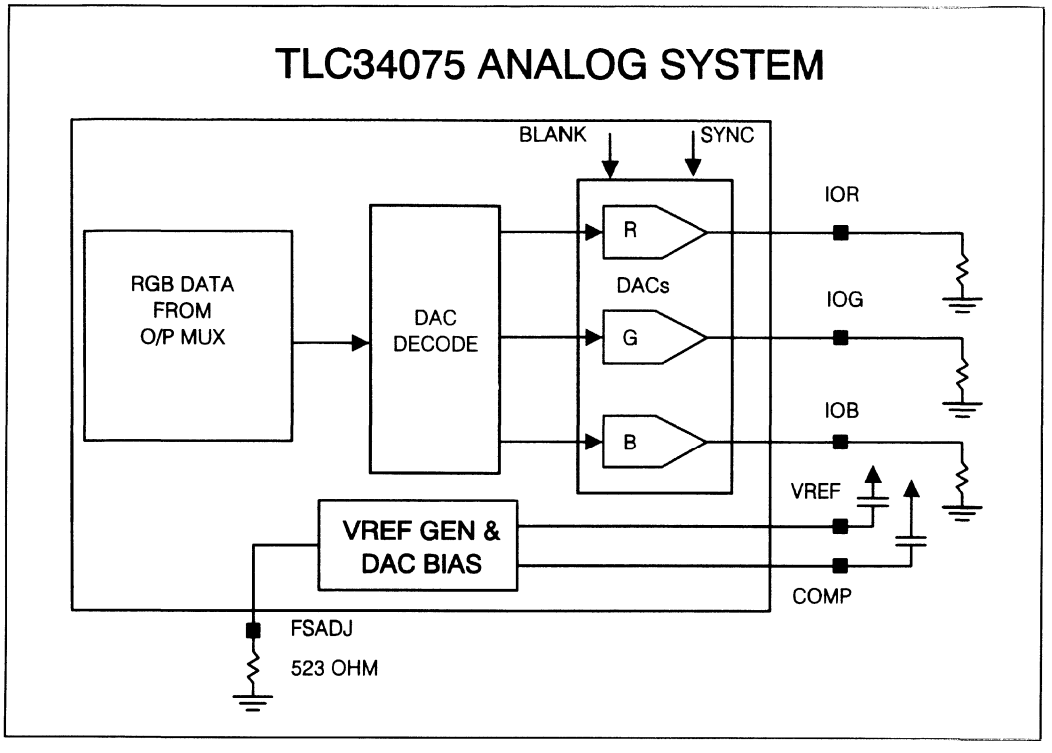


Figure 2.51 - TLC34075 Analog System

Color and brightness information are sent to the monitor as a continuously variable voltage. Therefore the digital information stored in the frame buffer or palette RAM must be converted to voltage levels that can be used by the monitor. This is the function of the output DACs and since color is represented by a mix of the three primary colors, red, green and blue, there is a DAC for each of these.

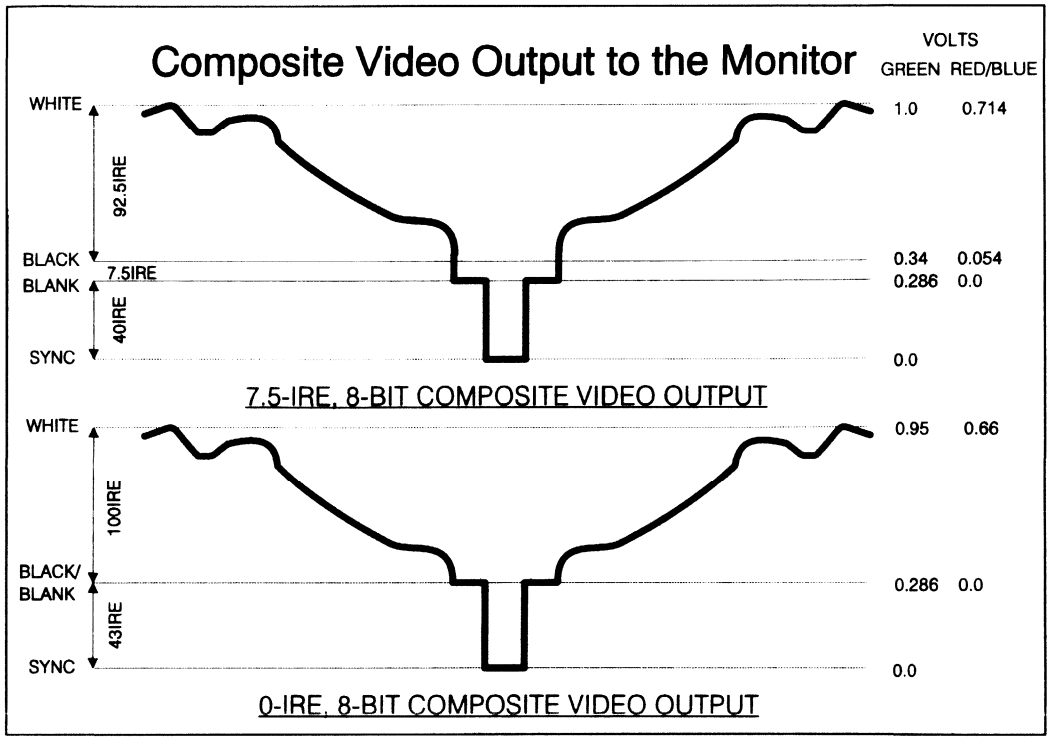


Figure 2.52 - Composite Video Output

Most RGB monitors have a 75 ohm input impedance and the analog output circuits must be able to drive this from a 75ohm source impedance (for a properly balanced line). The TLC34075 integrates this video output stage, being capable of driving video signals into a doubly balanced 75ohm line conforming to the RS-343A specification. Sync generation is incorporated into the green output for monitors which require sync-on-green. Figure ?? shows the composite video output on the green drive.

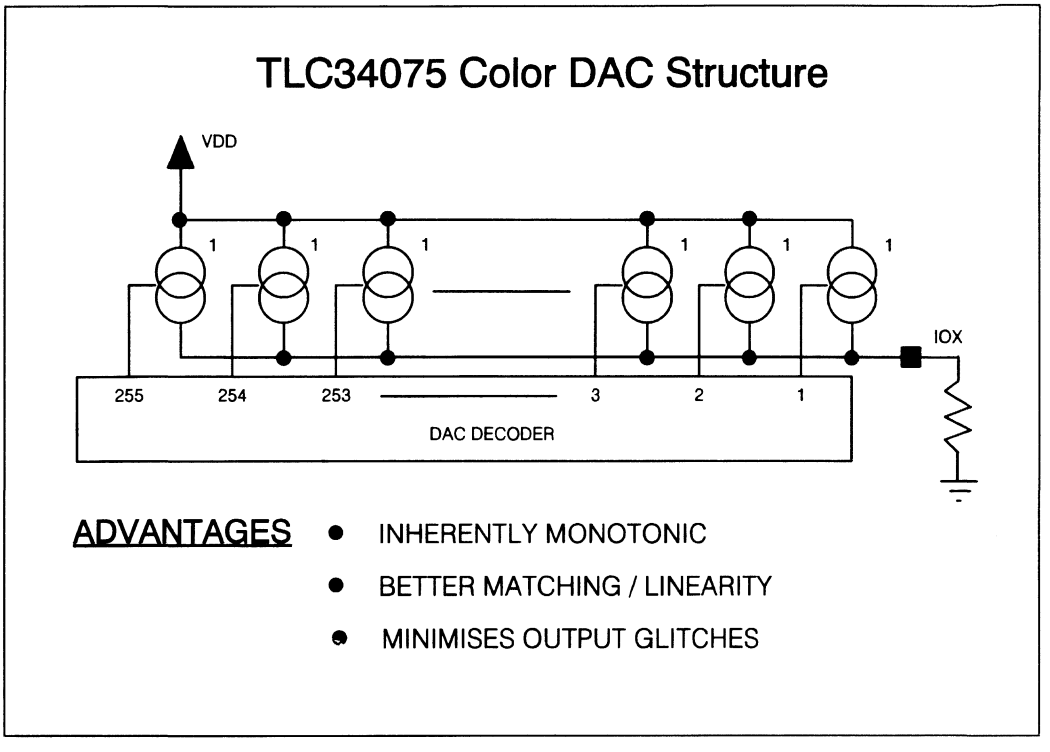


Figure 2.53 - TLC34075 Color DAC Structure

At the maximum palette speed of 135MHz there is only 7.4 ns available to settle to the new analog output value, so careful attention has to be paid to the design of the DACs. Instead of the normal, 8 binary weighted current sources, the TLC34075 has 255 equally weighted current sources. This system is inherently monotonic, has better linearity and matching and reduces output glitches, particularly around half scale.

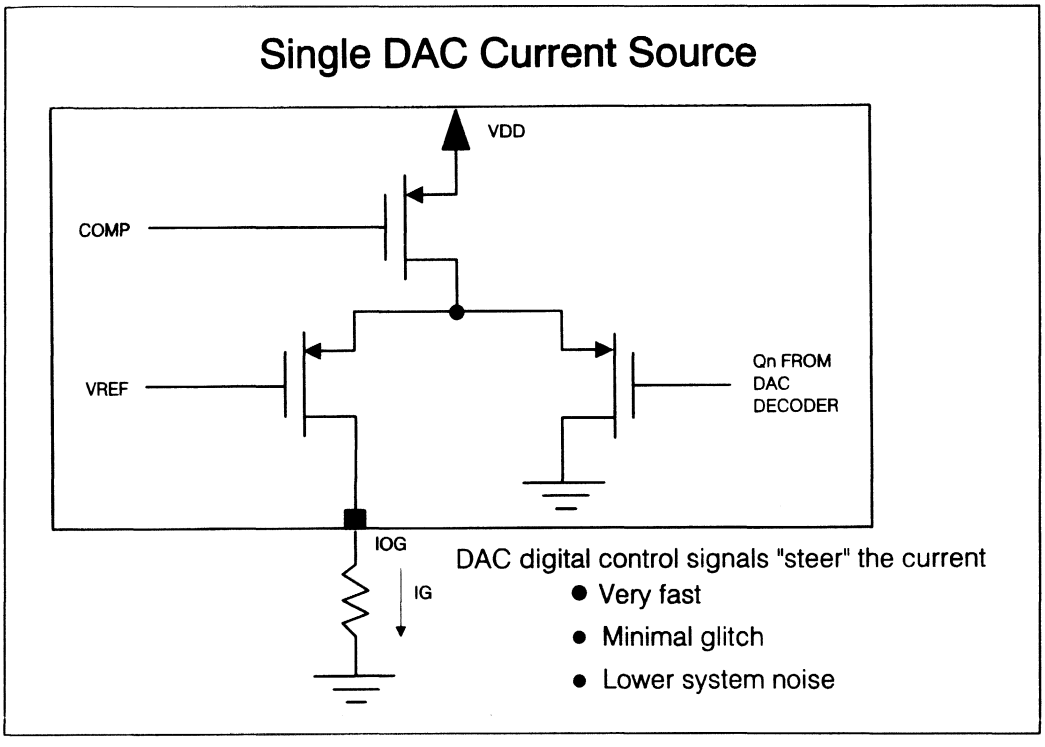


Figure 2.54 - Single DAC Current Source

Also, to reduce noise and glitches, the current sources are always "on" and the current is steered either through the load (the monitor input stage) or to ground. This has the advantages of being very fast, having minimal glitch and low system noise.

6.9. Video Interface Palette Roadmap

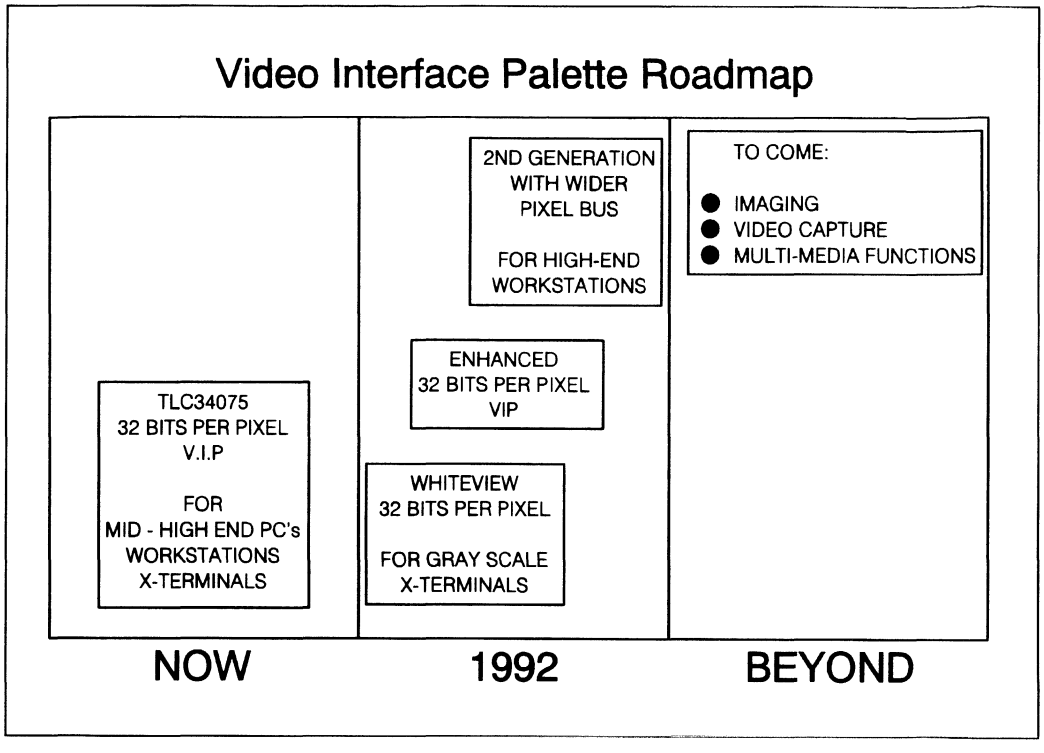


Figure 2.55 -Video Interface Palette Roadmap

7. Advanced Data Acquisition Products - Selection Guide

ANALOG INTERFACE CIRCUITS

PART No	RESOLUTION	FEATURES	FILTER B/W	MAX.SAMPLE RATE (KBPS)	VOLTAGE REFERENCE	DIRECT I/F TO DSP	ON-CHIP (SIN X)/X CORRECTION	APPLICATIONS
TLC32044CN	14 BITS	VOICE-BAND AIC	150-3800 Hz	19.2	INTERNAL	YES	SELECTABLE	SPEECH,MODEMS, DATA ANALYSIS
TLC32045CN	14 BITS	LOW COST VERSION OF TLC32044	150-3800 Hz	19.2	INTERNAL	YES	SELECTABLE	SPEECH,MODEMS, DATA ANALYSIS
TLC32046CN	14 BITS	EXTENDED BANDWIDTH AIC	300-7600 Hz	25	INTERNAL	YES	SELECTABLE	SPEECH,MODEMS, DATA ANALYSIS

GENERAL PURPOSE ADC

PART No	BITS	SPEED	LINEARITY	FEATURES
TLC1540CN	10	21 us	0.5LSB	12-CHANNEL MUX,SAMPLE/HOLD, SERIAL OUPUT
TLC1541IN	10	21 us	1.0LSB	1 LSB VERSION OF TLC1540
TLC1550IN	10	6 us	0.5LSB	SAMPLE/HOLD, PARALLEL OUTPUT, INT/EXT CLOCK
TLC1551IN	10	6 us	1.0LSB	1 LSB VERSION OF TLC1550
TLC1225IN	12 + SIGN	12 us	1.0LSB	SELF CALIBRATING,TRUE DIFFERENTIAL I/P, SAMPLE/HOLD
TLC1125IN	12 + SIGN	12 us	2.0LSB	2 LSB VERSION OF TLC1225
TLC0820B	8	2.5us	0.5LSB	ON-CHIP TRACK/HOLD, PARALLEL O/P, SEMI-FLASH

MDAC

PART No	BITS	SPEED	LINEARITY	FEATURES
TLC7524IN	8	100ns	0.5 LSB	5V -15V OPERATION, CURRENT O/P
TLC7528IN	8	100ns	0.5 LSB	DUAL MDAC, ON-CHIP DATA LATCHES

DUAL SLOPE ADC

PART No	BITS	SPEED	LINEARITY	FEATURES
TLC7135CN	4 1/2 DIGIT	12 CONV/SEC	1 in 20,000	DIFFERENTIAL I/P, 50-ppm ACCURACY. ZERO DRIFT < 0.5uV/°C I/P CURRENT <10pA

FLASH ADC

PART No	BITS	SPEED	LINEARITY	FEATURES	PROCESS
TLC5503-5CDW	8	10MHz	0.4%	5V I/P RANGE	LINEPIC
TLC5503-5CDW	8	10MHz	0.4%	2V I/P RANGE, DIFFERENTIAL GAIN AND PHASE SPECIFIED	LINEPIC
TL5501CN	6	20MHz	0.8%	LOW COST VIDEO	ALS

VIDEO DAC

PART No	BITS	SPEED	LINEARITY	FEATURES	PROCESS
TLC5602CN	8	20MHz	0.2%	1V O/P RANGE, LOW POWER	LINEPIC
TL5601CN	6	20MHz	0.8%	1V O/P RANGE, LOW COST	ALS
TL5602CN	8	20MHz	0.2%	1V O/P RANGE	ALS

VIDEO INTERFACE PALETTES

PART No	SPEED	FEATURES
TLC3058-80FN TLC34058-110FN	80MHz 110MHz	3 OFF 8 BIT VIDEO DACS, 256 x 24 COLOR LOOKUP TABLE
TLC34075-66FN TLC34075-85FN TLC34075-110FN TLC34075-135FN	66MHz 85MHz 110MHz 135MHz	3 OFF 8 BIT VIDEO DACS, 256 x 24 COLOR LOOKUP TABLE, 24-BIT TRUE COLOR MODE , DIRECT VGA PASS-THROUGH, PROGRAMMABLE DOT RATE, INTERGRATED HIGH SPEED TIMING LOGIC, PROGRAMMABLE PIXEL BUS WIDTH

Section 3
Sensor-Processing Systems

Section Contributions by:
Armin Lichtblau

Contents Section 3.

1. Sensor Signal Processor Family

1.1. TSS400 Family Overview

The following sections focus on a range of Sensor Signal Processors and Bus Drivers which are designed to support Sensor Processing and Meter-Bus applications. This is an overview of the different family members.

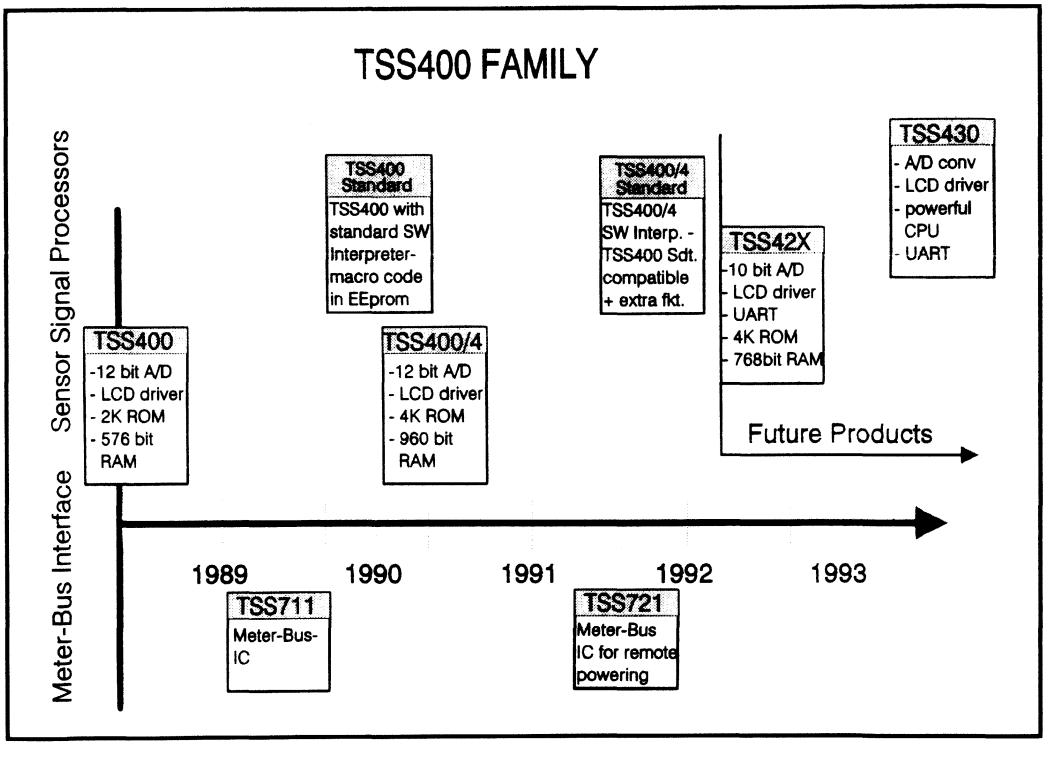


Figure 3.1 - TSS400 Family Overview

The TSS400 was the first product of this Family which will continuously be expanded. It was specially developed for battery driven meter applications such as electronic Water-Meters, Gas-Counters, Heat-Volume Counters or Electricity Meters. The requirements for these applications are very low power consumption and high A/D converter resolution. The TSS400 is a customer specific mask-device and meant for high volume applications.

For low and medium volume quantities a device called TSS400 Standard was developed. This device is an already pre-programmed TSS400 mask-device. It holds a software interpreter which receives user program instructions from external connected EEproms. The Standard device is designed to serve a wide range of different Sensor Applications. Well tested software routines inside the interpreter allow an adapting of customer specifics. This is an off-the-shelf product which can be bought in any quantity.

Following the successful introduction on the TSS400 there was a requirement for more ROM size to realize more complex applications. The TSS400/4, a mask device, with 4 K instead of 2 K ROM followed.

This new device was very helpful to improve the TSS400 Standard Version. The 2 K ROM was not big enough to implement all requirements from the market. The TSS400/4 Standard is a version which is compatible with the TSS400 Standard but implements some additional functions and a Bus-System.

The two Bus-Drivers, the TSS711 and TSS721 were designed to build up Meter-Bus Systems. The Meter-Bus was developed to transmit data accumulated by different battery-driven meters via long distances to a central station. In order so save battery power special requirements for this bus were identified. The TSS721 can even be used to provide remote powering. Hereby also mechanical meters can be connected to the Meter-Bus-System.

The development of the family is an ongoing task. New devices like the TSS42X are coming up. This device will have a UART implemented on board, which is helpful for bus communications. The TSS430 will serve applications which require more calculation power.

1.2. TSS400(/4) Mask-Version

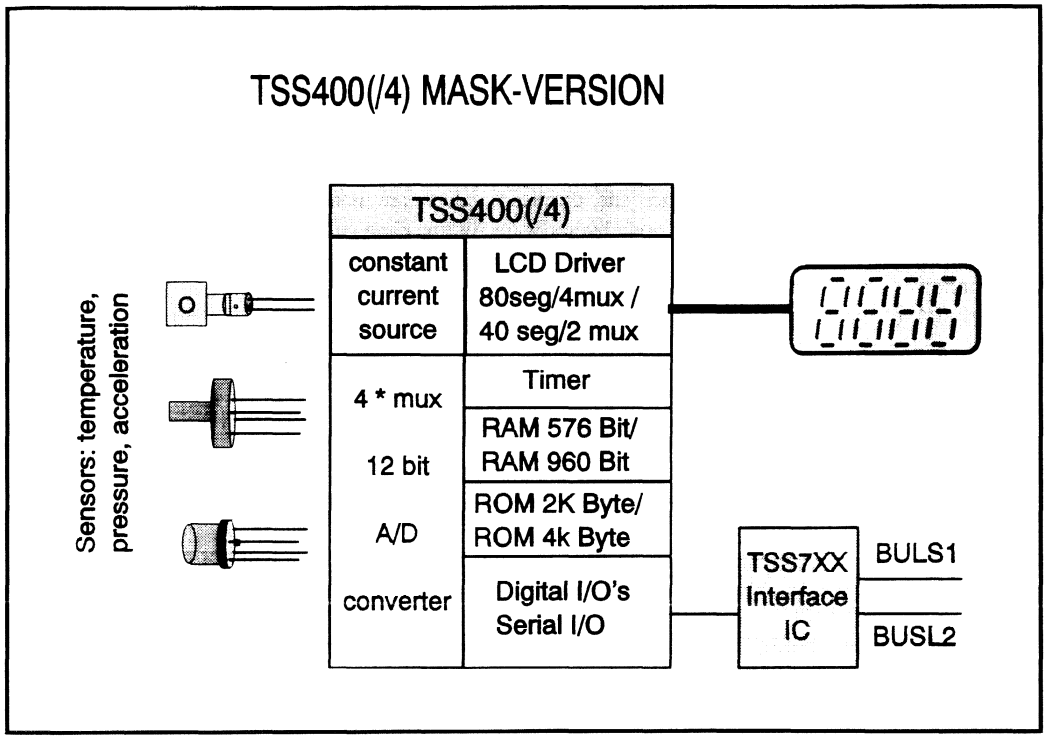


Figure 3.2 - TSS400(/4) Mask-Version

The TSS400 is a mask-programmable Sensor Signal Processor to receive analog values, process them, display them and probably communicate with other processor systems. The different mask options offers the user a wide range of flexibility. The device is available in three different packages, a 28 pin Dual-In-Line package, a 40 pin DIP, or a 44 pin PLCC package. The user can also select an individual pin configuration which helps to optimise the PCB layout.

This mask device is the optimum solution if the application runs in quantities higher than 10 000 units per year. For all applications running in lower volume a different solution, the TSS400 Standard was generated. This device will be discussed in details later on, but all hardware features which will be described for the TSS400 mask version are also true for the TSS400 Standard.

The key features of this micro-controller, which makes it quite unique, is the super-low power consumption in connection with a 12 bit A/D converter. A typical power consumption of a TSS400 application is 12 to 15 µA.

The 12 bit A/D converter integrated in the Sensor Signal Processor works after the successive approximation method. It has four multiplexed inputs. One out of four voltage input ranges can be selected. This input voltage range is defined by a mask option. This feature allows the direct connection of most passive sensors to the TSS400. Since a programmable current source is built-in, passive sensors can be driven in constant current or constant voltage mode.

After an analog value has been converted into a digital value the 4 bit CPU computes physical data which then can be displayed. Since the digitised values are necessarily processed anyhow, the calibration of the sensors is usually done by software routines and calibration data that is stored in the TSS400 RAM. The 2 K version (TSS400) offers 2 K instructions of ROM to store assembler instructions and 576 bit of RAM organised in nibbles (due to the 4 bit CPU). The 4 K version (TSS400/4) offers 4 K ROM and 960 bit RAM. Up to three subroutine levels are available.

The LCD driver can be configured to drive any 2-times or 4-times multiplexed LCD. Up to 80 segments can be driven in 4 mux mode, or up to 40 segments in 2 mux mode. A 2-mux LCD normally shows a better contrast over the whole temperature range, but also requires much more pins to drive it. The Common/Segment combination can be configured.

A timer circuit which is driven by an externally connected 32 768 Hz quartz is used for accurate timing functions. This oscillator is also used by the LCD driver unit. If accurate timing is not required, the quartz can be changed to an RC network to reduce the system price. This requires a special hardware option. This external oscillator is the only external part except for the power supply required to run the Sensor Signal Processor. The 32 768 Hz oscillator does not generate the CPU clock frequency, this is done by an internal independent MOS-oscillator. This oscillator runs nominally at 700 kHz.

4 K-lines, which are digital input/output lines, and 8 R-outputs, which are digital outputs, can be used for application inputs and outputs like a keyboard, controlling outputs, a buzzer or, via a transistor, external motors, lights, LED's etc. A special input/output line called I/O is reserved for serial data communication. This data communication might be used for calibration or to transmit pre-computed values to a host system. This can also be done over long distances when an additional driver is used. The protocol on this bus line is defined by the user software.

1.3. Potential Applications

The TSS400 can be used for various applications. The following is a brief overview of some already existing or possible designs in the Automotive, Industrial and Medical sector.

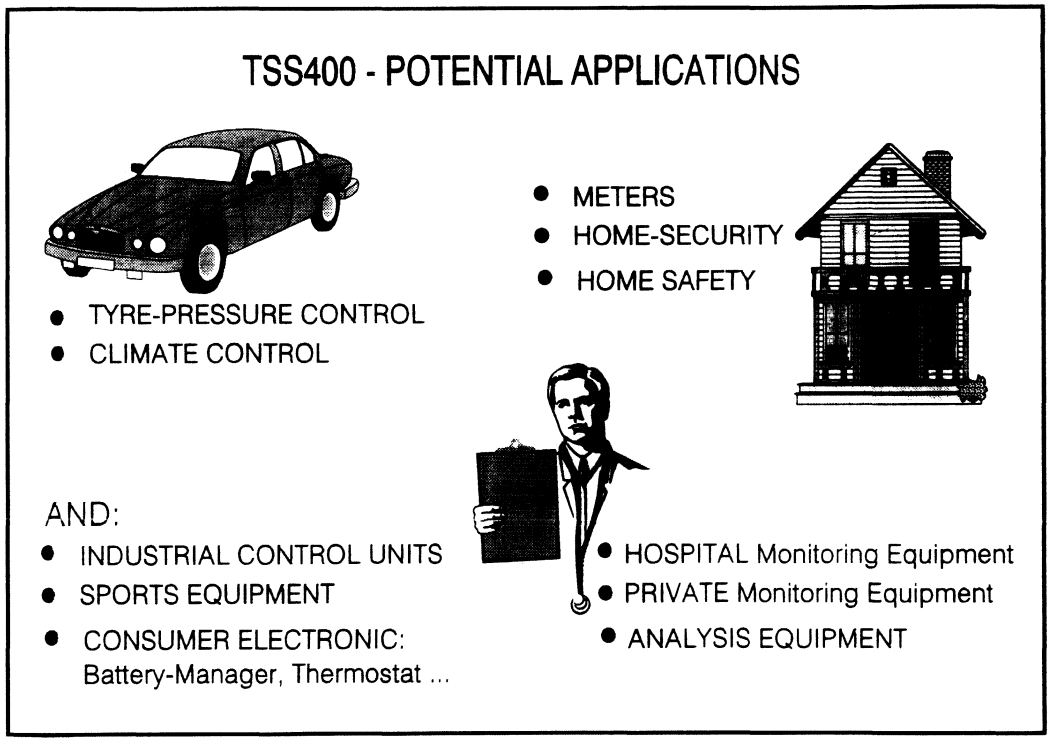


Figure 3.3 - Potential Applications

1.3.1. Industrial Applications

All kinds of Meters are typical applications for the TSS400 family. Electronic Meters have several advantages over mechanical, (traditional Meters)as they are normally more accurate. Electronic Gas-Meters for example use the gas temperature and the gas pressure to calculate the gas energy used. Purely mechanical meters can not perform this. Since all energy is getting more expensive the end-customer is interested in an accurate measurement.

Due to the low power consumption the device is also ideal for alarm systems. Smoke Detectors, temperature control units or gas detectors often work on batteries or on remote power systems. In both

cases a low power consumption is mandatory. Home security systems are also possible applications for similar reasons.

1.3.2. Automotive Applications

Applications like Tyre Pressure Control units or car climate control units produce analog values. These analog values have to be digitised and analysed. This requires a good A/D converter to provide a Host computer with the necessary information. The CPU capability of the TSS400's allows pre-processing of the measurements and enables standardisation of sensor data.

1.3.3. Medical Application

All kinds of monitoring equipment used in either hospitals or private homes to scan body functions are other ideal applications for the family. Usually the A/D converter accuracy is very important for these applications. Complex controlling monitors in Hospitals, Blood Pressure units and Blood analyser units for diabetic patients are some possible systems. For personal use battery operation is always a key feature which the TSS400 family serves very well.

There are many more opportunities for this unique family, most industrial control and measurement units are potential applications. Even for sophisticate consumer products like Battery-Management units the Sensor Signal Processor is a very efficient solution. Sports equipment like Alti-Meters for Mountain hikers or Para-Sail and Para-Gliders or Divers Watches are just some examples of the diverse applications already utllising the TSS400.

1.4. TSS400(/4) A/D Converter

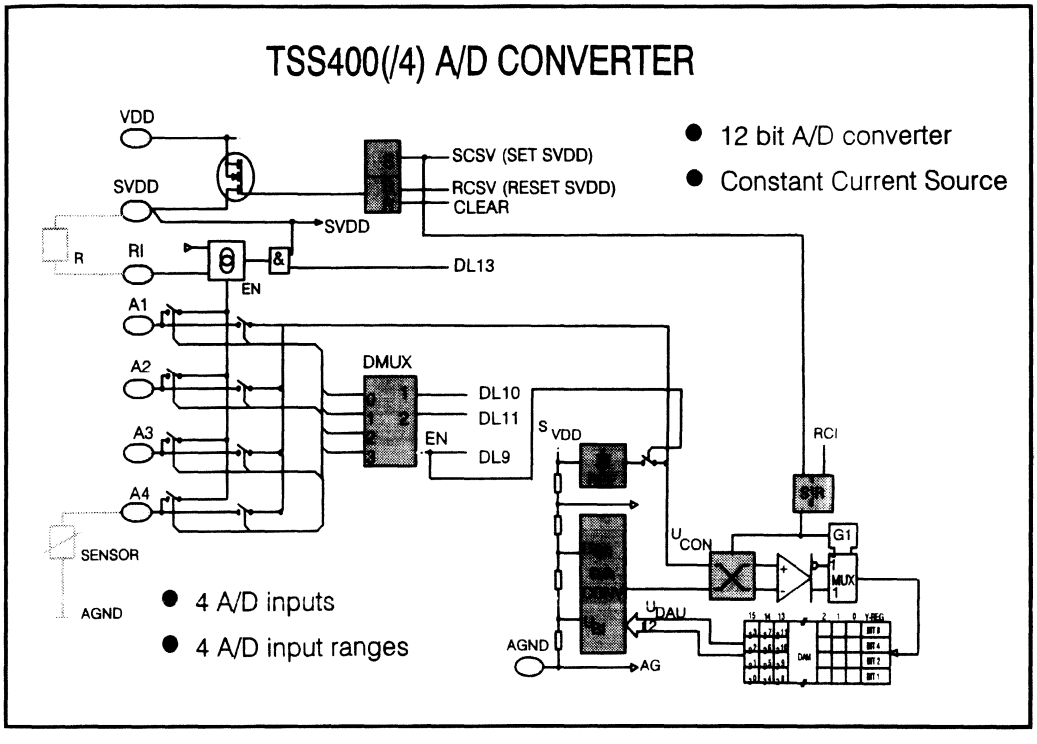


Figure 3.4 - TSS400(/4) A/D Converter

The TSS400(/4) A/D converter uses a successive approximation technique. This means a internal D/A converter network is loaded with a digital value supplied by a special RAM bank. The D/A converter is generates an analog voltage which is then compared with the voltage to be measured. This is done bit by bit, starting with the most significant bit, 12 times. The analog input voltage is compared with the D/A network output and the RAM content is adjusted to the result of the comparison. The input voltage needs to be constant during the comparison time.

One of the following four input ranges can be selected by a mask option:

Range SMALL	0.237986 · SVDD to 0.400839 · SVDD
Range LARGE	0.107939 · SVDD to 0.487977 · SVDD
Range MEDIUM LOW	0.107013 · SVDD to 0.395857 · SVDD
Range MEDIUM HIGH	0.239355 · SVDD to 0.493731 · SVDD

The optimal range for an application is defined by the sensors connected to the system.

One of the four analog inputs is selected by the multiplexer DMUX. If the external sensor is driven in constant current mode the internal current source part is activated. The current source is programmed by a resistor on the pins RI and SVDD. The current is then provided on the selected input AX. The sensor generates a voltage dependent on the resistance, which is dependent on the physical parameter it is measuring. The programmed constant current can be supplied to any of the A/D inputs.

The current source is activated with a special digital signal DL13 and SVDD switched on. The current passed via an analog input to a sensor is calculated:

$$I_{An} = \frac{V_{Rext}}{R_{ext}}$$

The current flowing through a sensor (e. g. resistive temperature sensor), generates a voltage drop at the sensor which is calculated:

$$V_{in} = I_{An} \cdot R_{in} \quad \text{with } R_{in} \text{ as the sensor's resistance}$$

$$V_{in} = V_{Rext} \cdot \frac{R_{in}}{R_{ext}}$$

This voltage is compared with a voltage generated by a D/A network and the digital equivalent is stored in the TSS400 RAM. The comparator will have an offset, however this offset is eliminated by performing two complete 12 bit A/D conversions, one with switched comparator inputs. Therefore the offset is added up once positively, once negatively and effectively is eliminated.

The sensor is connected to SVDD either directly in constant voltage mode, or via R on RI in constant current mode. This is also true for the D/A converter network which generates the comparison voltage. Therefore a ratiometric measurement is performed. This is important for battery driven sensor systems. During the lifetime of the application the battery voltage is changing with temperature and discharging. Since both, the sensor as well as the A/D converter are supplied by the same source, a constant A/D conversion result can be guaranteed independently of the supply.

All external analog parts as well as all internal A/D converter parts are connected to SVDD. SVDD is a switch able power source. It is connected to VDD and can be turned on and off by a software command. It is only switched to active mode during an A/D conversion. Most of the time the most power-consuming analog part of the application remains un-powered. This is one of the main power saving features of the Sensor Signal Processor family.

1.4.1. Battery Check:

The A/D converter part of the TSS400 includes also a constant voltage reference. This reference is almost independent from VDD or SVDD and temperature. This reference can be used to check the

condition of the battery or other power supplies. The reference can be connected to the comparator via an extra internal input of the multiplexer. As the battery voltage goes down a higher A/D value must be fed into the D/A network to reach the constant voltage level of the reference. A critical level can be calibrated and controlled via the user program. If this level is reached a warning, like a blinking display, can be activated and a battery change performed.

This internal reference is almost constant. It is specified with ±100 mV, which is certainly good enough to check a battery, but a judgement is necessary in case it will be used for other purposes.

1.5. TSS400(/4) Run Modes

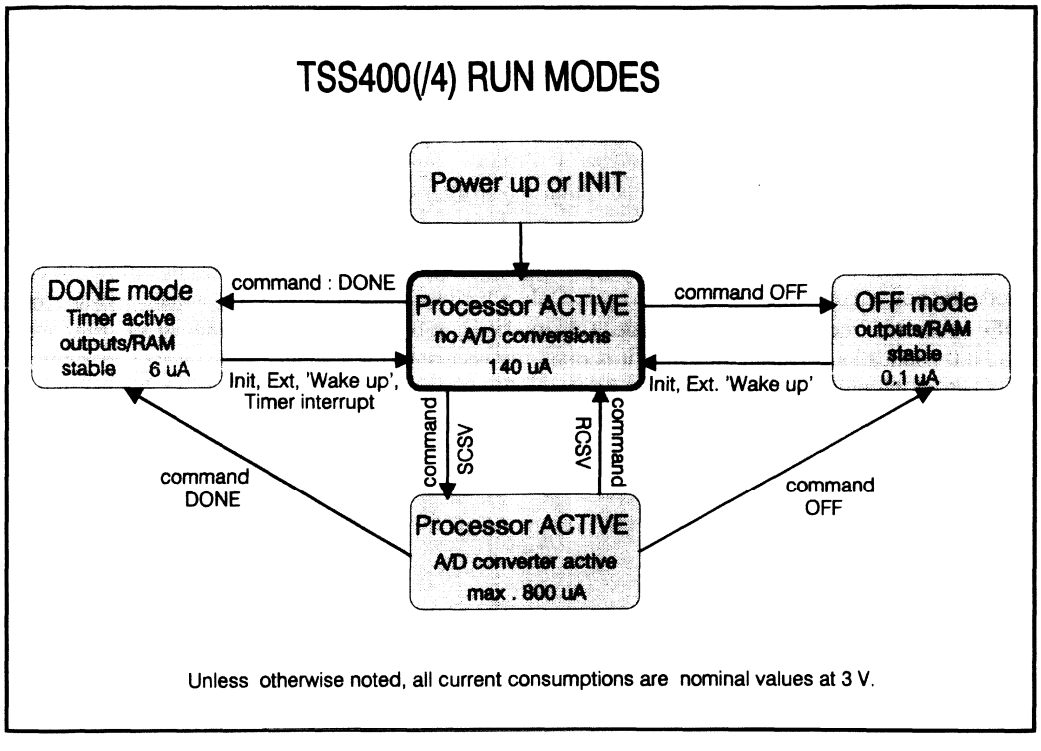


Figure 3.5 - TSS400(/4) Run Modes

The TSS400 has four different RUN modes. Each one has its own typical power consumption. Software commands and hardware signals are used to swap between the different modes.

After a Power-up or a INITN the processor enters 'Processor ACTIVE' mode. All parts of the CPU are switched on except for the A/D converter and the external analog components connected to it. The

typical power consumption is 140 µA. Usually, after a few initialisation routines the User program is performing a A/D conversion. Via a software command the processor switches to a mode where the A/D converter is also switched on .

During an A/D conversion, which is only about 1 ms, the power consumption reaches a peak. Depending on the externally connected components the processor consumes a maximum of 800 µA for this short time. Another software command switches back to 'Processor ACTIVE' mode without the A/D converter active.

Further calculations are done with the A/D conversion result. Additions and Multiplications using the calibration data are executed and finally a corresponding physical value is displayed on the LCD. Since sensor values are slow changing values it is not necessary to perform a measurement constantly. Once a second or even once every 5 seconds is usually quite sufficient. During this time it is not necessary for the processor to stay active. A software command switches it into 'DONE mode'.

In this mode the CPU is switched off, but the timer is active, the LCD part is active, the outputs are stable and a wakeup circuit is activated. The nominal power consumption in this mode is 6 µA. This is the mode where an application stays most of the time, typically 75%. Either a timer, e. g. once a second, or an external wakeup triggered by a hardware signal, swaps back to 'Processor ACTIVE' mode. The User software then controls the actions taken after such a wakeup.

There is a fourth mode, the so called 'OFF mode' available in the TSS400. In this mode all parts except the RAM refreshing unit are switched off. The outputs remain stable, but the LCD is turned off. In this mode the power consumption is only 0.1 µA. Only a hardware signal or a INITN initiate a swap from 'OFF mode' to 'Processor ACTIVE' mode. This mode might be used to stock assembled and calibrated TSS400 applications. During this time it is often not necessary for a application to perform anything. Just before the unit is delivered or used by the end customer a button can be pressed and the unit is activated. This feature is maximising the life-time of the battery.

1.6. TSS400(/4) Standard

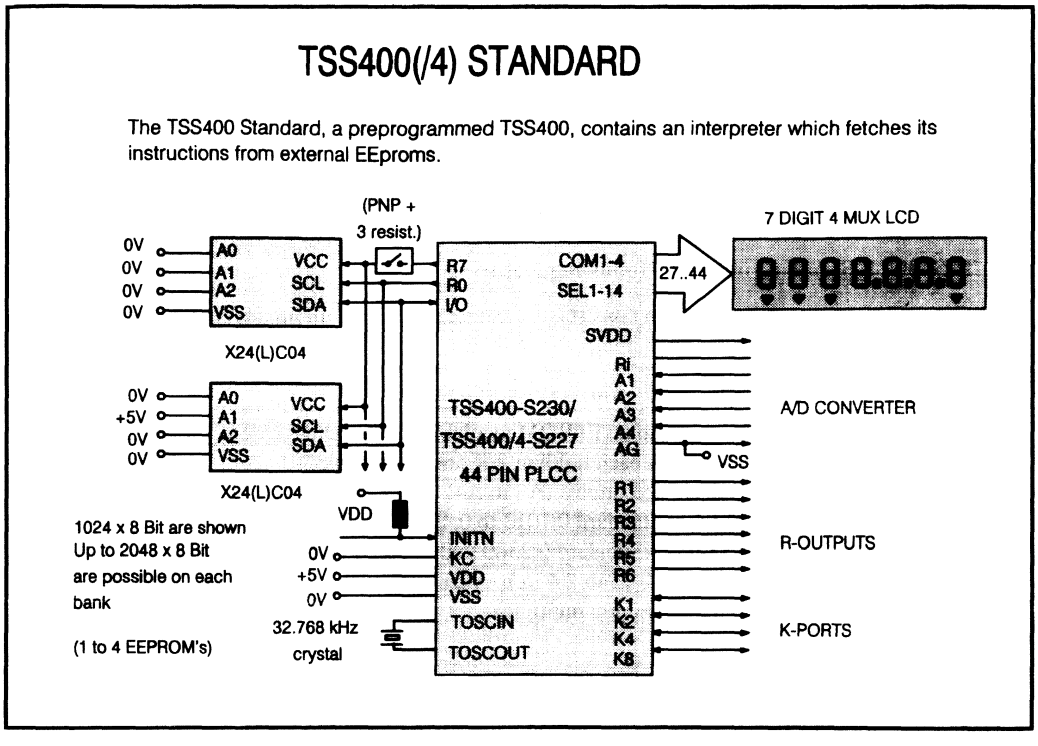


Figure 3.6 - TSS400(/4)

The TSS400 Standard was developed to suit a wide variety of applications where the cost of a ROM mask is not appropriate. Proven software routines are stored in a pre-programmed TSS400 and can be accessed according to a user's need.

Up to four EPROM's, which store the user program and program data, can be connected to the TSS400 Standard. This is equal to 2 K of instructions and built one bank. There are two versions of the Standard available, a pre-programmed TSS400 with 2 K ROM and one with 4 K of ROM. Up to 64 banks can be connected to the TSS400/4 Standard.

TSS400 Standard	TSS400-S230 -2 K ROM
TSS400/4 Standard	TSS400/4-s227 - 4 K ROM

The signal RO is used to provide the clock signals, R7 controls the EPROM supply voltage via a PNP transistor and the I/O pin is used to perform data communication in both directions.

After initialisation the interpreter program will access the EPROM'S to read out macro instructions. The instructions are interpreted and the internally stored Software routine is executed. The power supply for the EPROM's is switched off during a command execution to minimise the power consumption. Therefore the average power consumption of a Standard application is only slightly higher than on a mask version. All the power saving run modes of the TSS400 mask version, are available in the Standard versions.

The interpreter language is ranked between assembler and compiler language, therefore very easy to learn and includes very powerful commands. The software development time is reduced to an absolute minimum.

The TSS400(/4) Standard offers the following features:

- Minimum component count: System consists of 2 devices only, in a minimum configuration:
  - TSS400(/4) with pre-programmed interpreter software
  - EPROM with user's program
- 512 instructions (8 bits wide) in each EPROM. Up to four EPROM's are possible (2048 byte maximum) in one bank. There is also an EPROM available holding 2048 byte in one package. On the TSS400(/4) up to 64 banks each holding 2 K are addressable.
- 12 bit A/D converter with 4 delectable inputs (A1 to A4)
- A/D converter range : TSS400 Standard 0.1013 to 0.4946 · SVDD
  TSS400/4 Standard 0.2380 to 0.4008 · SVDD
- Programmable current source from 0.15 to 2.4 mA · VDD/V for all A/D converter inputs.
- LCD driver with 7 digits using 4 common multiplex.
- 576/960 bits of static RAM.
- Three levels of subroutine.
- Time keeping from an on-chip quartz oscillator (32 768 Hz).
- Done Mode for reduction of power consumption with active timers and RAM. Wake-up is possible via 2 timers (input frequencies 1 Hz and 16 Hz) or by input changes.
- Off Mode for very low power consumption with active RAM. Wake-up by input changes only.
- Internal MOS oscillator: nominal 700 kHz
- 6 freely usable push-pull outputs (R1 to R6).
- 4 bit I/O port (K-Port).
- Program control by EPROM or host computer (Slave Mode).

The TSS400/4 Standard is an extended version of the 2 K Standard. Since the ROM is twice as big some extra commands, a bank switching and a Bus-System have been built in. The devices are fully pin compatible. All commands running on the 2 K version will work on a 4 K version. Up to 64 banks can be addressed by using the R-outputs. A large amount of external EPROM space may be addressed to store data (e. g. in a data logger) or interpreter programs. The bus system will be explained later on.

1.7. TSS400 Typical Applications

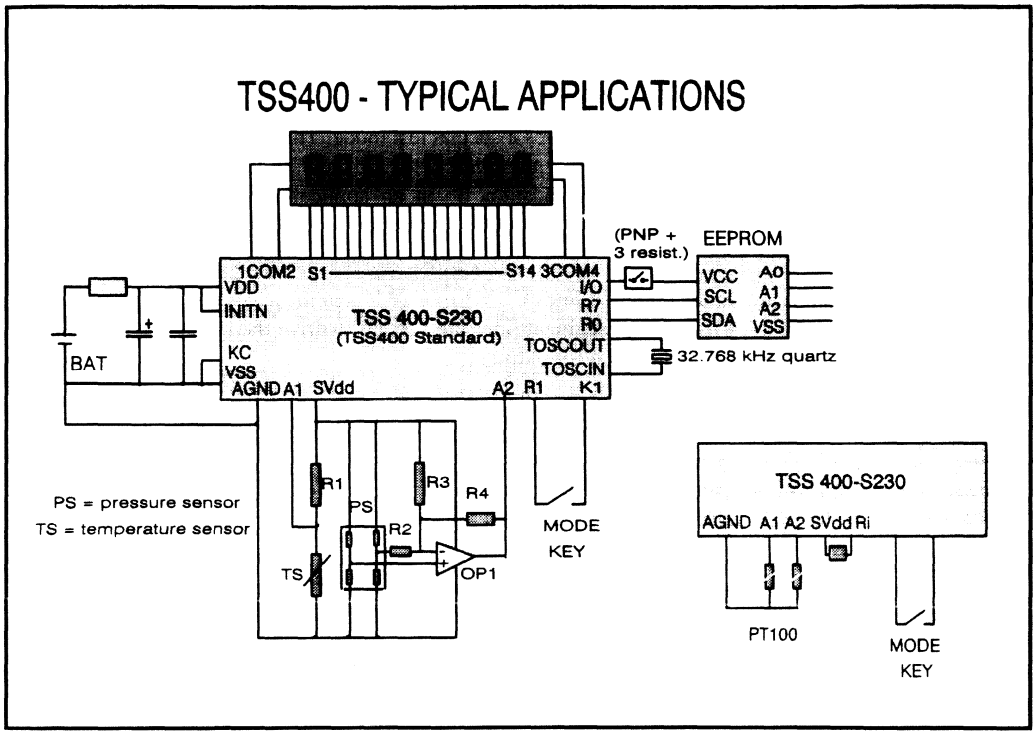


Figure 3.7 - Typical Applications

The block-diagram shows a typical TSS400 application. The application is measuring pressure and temperature and is displaying a calculated value on a LCD. This could be an Altimeter or a Divers-Watch or an industrial pressure control unit. Any TSS400, TSS404 or TSS400(/4) Standard application can be realised with a minimum component count.

This pressure application described using a TSS400(/4) Standard, since a EPROM for the program code is connected. (In principle the application would look exactly the same on a mask device.) On a mask device a external EPROM is normally not necessary, and therefore these outputs may be used for different purposes.

This application is battery driven. The battery voltage is buffered by a capacitor and a electrolytic capacitor. Since the TSS400 is a CMOS device this is advisable to immunise the system against electrostatic discharges. It is important to attach the capacitors on the PCB as close as possible to the VSS and VDD pins, of the power supply for the processor.

A resistor may be included in the power supply path to check the power consumption of the TSS400 application for test purposes. This could be used to track the power consumption in the different run modes or to calculate an average power consumption.

The pin INITN is used to start a defined initialisation. During normal operating mode it is not used. Nevertheless it is important to supply this signal as a defined level. Since INITN is a low-active signal a logical high needs to be supplied. If the INITN pin is used in a application for a defined re-start, and can be accessed via a button, it should be connected via a pull-up resistor.

The KC pin is for test purposes only, as it activates a special test mode. This test mode is used to check the IC during production. (All parts of the IC, regardless whether they are used in an application or not, are tested and checked against the specification.) In an application this signal is not used, however it is a mandatory input signal and should be connected to a defined level. KC must be connected to digital ground VSS.

An LCD is simply connected to the common lines COM1 to COM4 and the necessary Segment lines. If a TSS400(/4) Standard is used and not all segment lines are needed to drive the LCD, these extra lines may be left unconnected (uncritical situation for outputs).

EEPROM's for storing user macro instructions and/or calibration data are connected via the lines I/O, R7 and R0. A 32 768 Hz quartz should be connected to the TOSCOUT and TOSCIN pins on a TSS400(/4) Standard. This oscillator is used to generate a accurate timer signal. The quartz requires no additional capacitors, as often necessary in other processor families. Also the LCD uses this oscillating source to generate the LCD signals. Every LCD needs to be supplied with as much positive charge as negative charge over life-time. This is important otherwise the electrolytical liquid in a LCD is destroyed. In a TSS400 mask version it is possible to replace the quartz by a simple RC network if accurate timing is not important. This requires a special hardware adaption which can be performed with a mask option only.

All analog parts of the application are supplied by SVDD, a switch able VDD, allowing the analog electronics to be powered when in use only. Since the TSS400 is not equipped with differential inputs, a bridge-type silicon pressure sensor needs to be connected to a differential amplifier. This amplifier generates a measurable voltage and adapts the voltage as well as the offset level of the pressure sensor to the A/D converter input range. Note that SVDD supplies the pressure sensor and the differential amplifier. A2 is used to convert the pressure signal. The pressure signal of a pressure sensor is almost linear over a wide pressure range, but needs to be calibrated, since every sensor shows a unique offset and slope.

Since a silicon pressure sensor is very temperature sensitive, temperature compensation is necessary. This may be done by a silicon temperature sensor. The output signal of such a sensor can be easily linearized over a certain temperature range by a resistor. Input A1 is used to digitise the temperature value. It is also necessary to calibrate the offset and the slope of this sensor, too. The power supply for the temperature sensor is again SVDD.

To initiate a A/D conversion with this hardware connection it is simply necessary to turn on the power supply for the analog part (switch SVDD on). Allow the external parts some time to settle and supply a stable output to the A/D converter. To compute pressure and temperature values from the digital results software calibration may be used. Instead of using external resistor networks, as is common in pure analog circuits, the calibration data of a sensor can be stored in the RAM of the TSS400 or in a external connected EPROM.

1.7.1. SW Calibration of a Temperature Sensor:

The output of a liniarized temperature sensor shows a unique slope and offset:

$$T_A = A/D_{temp} * T_S + T_{OFF}$$

T_A = temperature
A/D_{temp} = temperature sensor A/D result
T_S = calibration data temperature slope
T_{OFF} = calibration data temperature offset

To calibrate this sensor the TSS400 goes into a special user software controlled run mode, in which a normal A/D conversion on A1 is performed and the result is displayed or communicated to a external host system. Once a measurement is done with two exactly known temperatures, T_S and T_{OFF} of this sensor can be calculated.

When the two calibration temperatures are fixed (using constant temperature baths) or if they are entered into the TSS400 (keyboard) a self-calibration cycle without any external computing can be performed. During any calibration not only the sensor but also the whole system is calibrated. The A/D converter for example comes with a process dependent offset. Other offsets may be added by PCB configurations, long lines or filters. All these influences are calibrated with the method explained above and this is a major advantage over an analog hardware calibration.

1.7.2. SW Calibration of a Pressure Sensor:

The output of a pressure sensor can be considered as linear within a certain measurement limit, but shows a slope and offset. This slope and offset are also highly temperature dependent:

$$P = A/D_{pressure} * (P_S + P_{TS} * T_A) + P_{OFF} + P_{TOFF} * T_A$$

P = pressure
$A/D_{pressure}$ = pressure sensor A/D result
P_S = calibration data sensor slope
P_{TS} = calibration data sensor slope temperature dependence
T_A = temperature
P_{OFF} = calibration data sensor offset
P_{TOFF} = calibration data sensor offset temperature dependence

The calibration data can be calculated similar to the calibration data of the temperature sensor. For a pressure sensor two different known pressures have to be converted at two different known temperatures. From these four A/D converter results the calibration data can be calculated.

1.7.3. Constant Current Supply

The sensors in the pressure application are supplied by constant voltage. If constant currents are supplied to the sensors the analog part of the application has to be modified. The sensors used in constant current mode are connected to the analog inputs directly. The constant current is 'programmed' by an external resistor connected to the pins SVDD and RI. The current is only flowing through the sensor when SVDD is switched on. To activate the constant current source a special software command is necessary. This allows a control over the current source, therefore sensors used in current mode and sensors used in voltage mode can be mixed and used together in one application.

Note: It is important that an external connection between analog ground AGND and digital ground VSS is made. Otherwise the A/D converter may produce unstable conversion results.

1.8. TSS400 Standard - SDT400

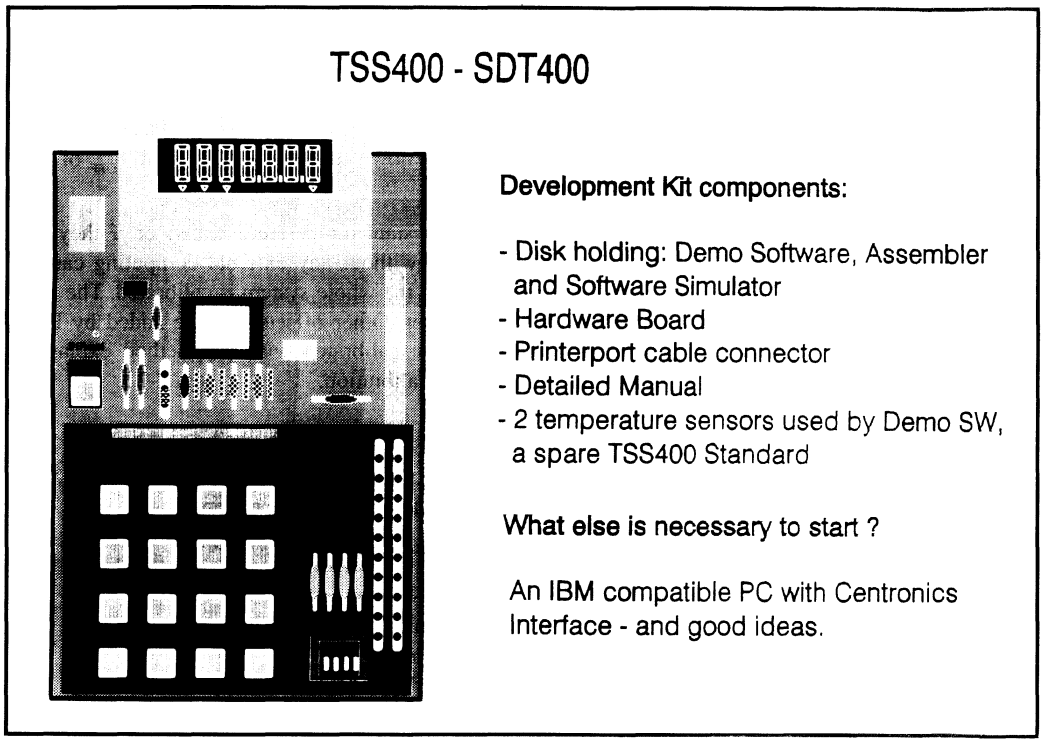


Figure 3.8 - TSS400 Standard - SDT400

The Standard Development Tool 400 is a inexpensive emulating tool to develop and test TSS400(/4) Standard Software. The Development Tool comes ready equipped with all software and hardware necessary to start the user software development. It consists of a Software Simulator and a Hardware-board.

The macro language is decoded with any editor. The ASM400, delivered with the SDT400-Kit, is used to translate the source file into an object file. This object file can be used by the Software Simulator.

The Software Simulator is a window-driven software package which runs on all IBM-AT compatible Personal Computers and allows a fast and easy development. All functions, with exception of hardware communication on inputs and outputs, are possible. Inputs and outputs are controlled via the

keyboard. For development and test of the program algorithms no hardware is necessary. All internal registers, input-states, output-states and flags are shown simultaneously on one screen and may be modified whenever needed, also during run mode, by the PC's keyboard. Several debug functions like breakpoints or single step can be executed.

Once a Macro program is checked with the simulator and all bugs are eliminated a real-time run may be performed on the Development Board. The Board is connected to the CENTRONICS interface of the PC with the connector cable supplied. The tested user program is burned into the EEPROM's on the board, with the appropriate Simulator instruction. After a reread for verification the Hardware is ready for tests. The PC connection is not longer needed.

The Development Board is not equipped with debug features. It is a test board to check the user program under real-time conditions. Nevertheless, debugging may be performed by inserting software breakpoints into critical parts of the user program. Several possibilities exist to halt or check at those locations:

- jumps into loops
- waiting for a key to be pressed
- displaying of registers in the LCD
- entering register values via the keyboard

The Development Board is equipped with an LCD, a predefined keyboard, an adjustable voltage regulator, the burn-in logic and several connectors for sensors and digital signals. TI has set-up the hardware in a way that an easy and fast application start-up is possible. The final application PCB and hardware looks very different, most likely much simpler of course.

The Development Kit includes a Demo-Software. Together with the temperature sensors supplied a thermometer can be built up. This might be helpful to get familiar with the macro instructions as as with the handling of the development tool.

2. Meter Bus

2.1. Meter-Bus Concept

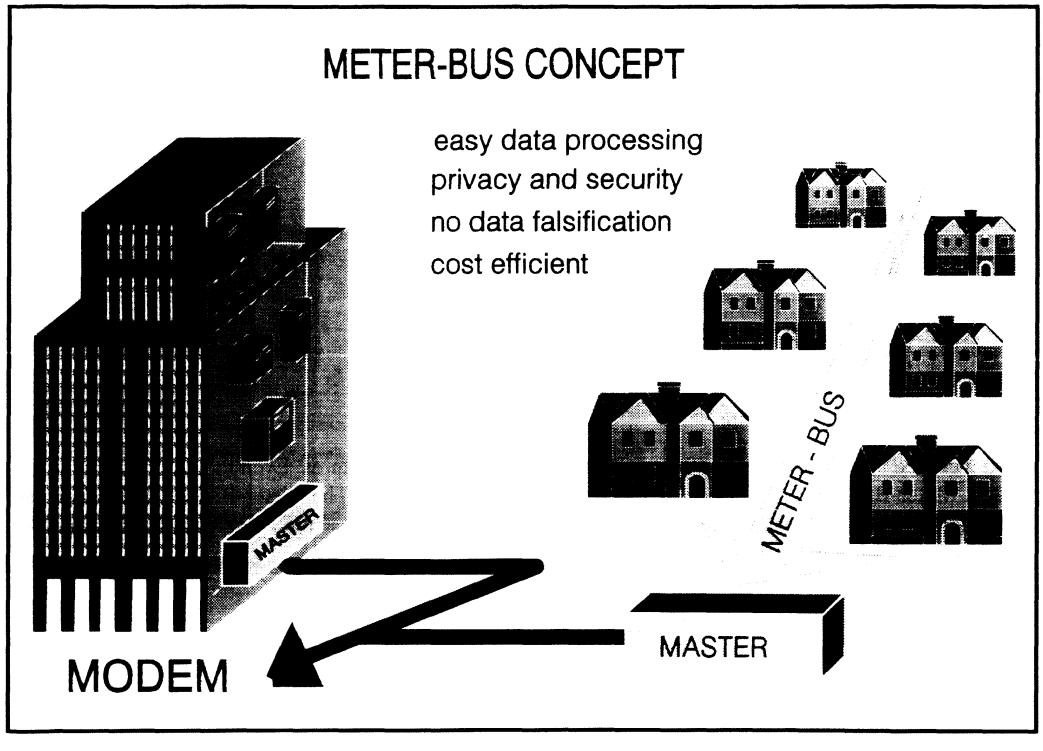


Figure 3.9 - Meter-Bus Concept

The TSS400 is a very easy-to-use device for meter applications. Because energy is becoming more and more expensive and environmental awarness is building up, accurate energy measurement becomes important. Electronic meters are much more accurate than mechanical or electro-mechanical meters. Modern Gas Counters take gas pressure and gas temperature to calculate the gas energy. This is an

impossible task for a mechanical meter. Electronic meters are as reliable as mechanical meters and have a major advantage, they can communicate with other electronic systems.

Once electronic meters are installed in private and commercial buildings the need for a bus system is very clear. A bus system for electronic meters offer a lot of advantages. Data processing can be done very easily. Computer systems can exchange information as often as necessary and erroneous read-outs are minimised. If all meters are read-out fully automatically privacy and a maximum of security are guaranteed for the end- user. No meter-reader has to access private homes which is also a major cost reduction.

Meters can be installed in huge apartment blocks. Many meters may be installed in such buildings and it is a major effort to do a manual readout of these meters. A bus system can connect these meters with a central Master Unit. A similar system can be used for private homes. Single or multiple homes in one street can be connected to one master system. The data collected, which is stored in the master stations, can be transmitted via modems and telephone lines over long distances. Where such systems are not installed, or for areas where this topology is inappropriate a meter reader can collect the consumption values via a transportable readout unit. This saves time and costs and guarantees a minimum of readout errors.

To implement an acceptable bus system many special requirements must be fulfilled:

- standard wiring material
- a maximum of slave count
- battery systems connectable
- remote power supply
- adaptable to existing protocols
- medium transmission distances
- adaptable to different processor types
- polarity independent

TI developed a bus system called Meter-Bus which offers all this features. Even though the name of the bus is Meter-Bus it may be used for several different applications. The Meter-Bus has been excepted by Meter producing companies already. The bus was also accepted for standardisation. An international ISO will be announced soon.

2.2. Physical Layer

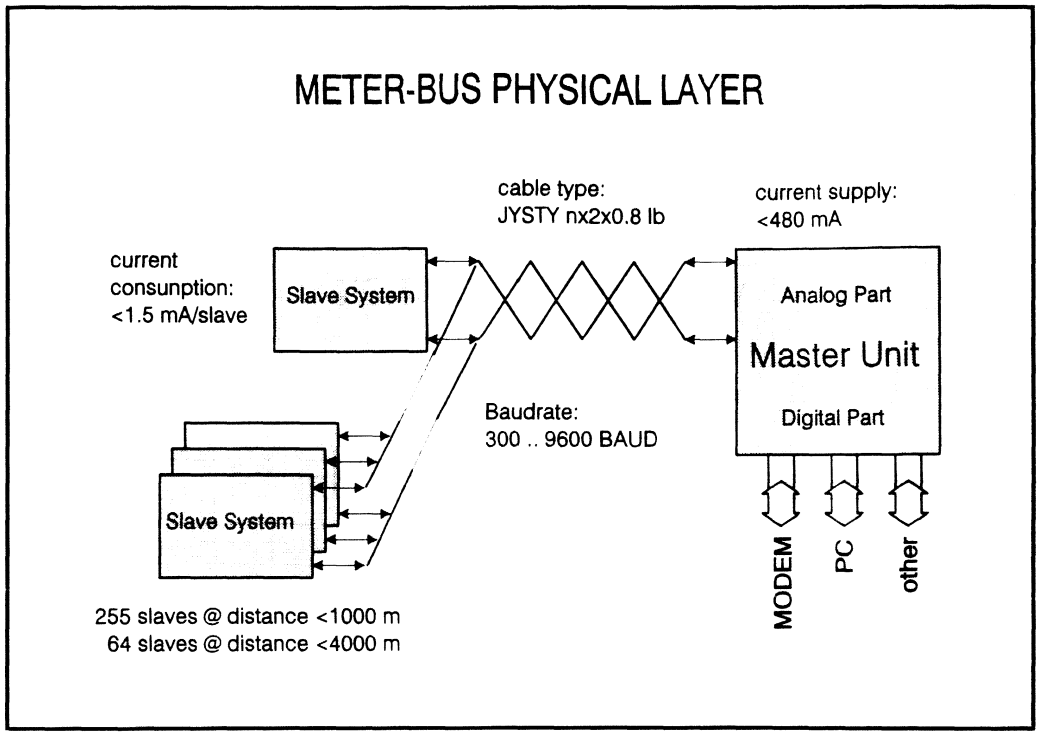


Figure 3.10 - Physical Layer

The Meter-Bus uses a Master Unit which controls the protocol on the bus as well as supplying the power for the data transmission. It consists of an analog part which is modulating the bus and detecting information sent from the slaves systems.

The slaves, which are typically Meters are connected via a bus-driver unit to ordinary twisted pair telephone wiring material (called JYSTY nx2n0.8 lb). To do the connection a the bus-driver TSS721 is used. Up to 255 slaves can be connected to one Master Unit over a maximum distance of 1000 m. This distance can even be expanded to 4000 m if not more than 64 slaves will be connected.

Each slaves is identified by its unique address. The communication is bi-directional. The transmission rate is defined with 300 to 9600 Baud. The power supply for the TSS721 is provided via the bus lines. Some of the energy supplied on the bus lines 1.5 mA/slave can be used to provide remote powering to a connected slave.

The digital part of the Master Unit controls the level on the analog part, which is handling the bus signals. It is also controlling the bus protocol and is handling data collision. The Master Unit can hold any kind of processor. The protocol used, which is not at all defined by the Meter-Bus, defines the hardware requirements of the digital part. A Master Unit typically is equipped with an interface to other data processing or transmitting systems (like PC, Modem, Handheld Terminal, other Bus Systems).

2.3. Modulation

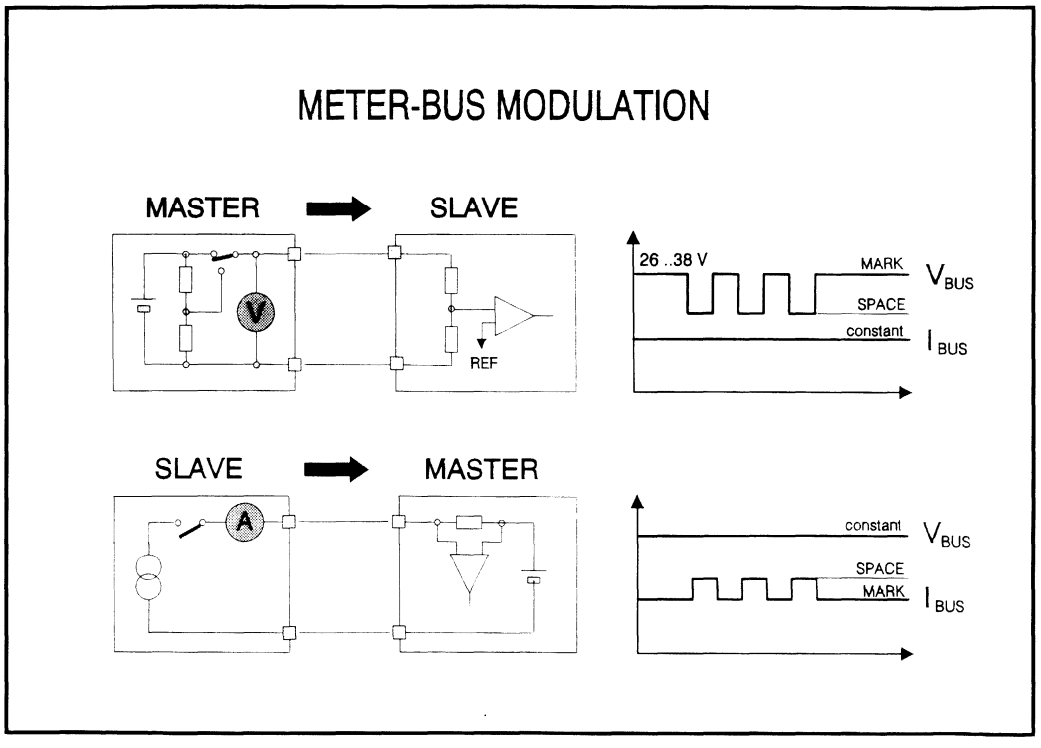


Figure 3.11 - Modulation

Since the Master Unit needs to supply the power for the driver units as well as for driving information a current loop seems to be ideal. A typical current loop works with 20 mA levels. But 255 systems connected to a bus each working on 20 mA is too much power on a ordinary telephone line. A pure voltage modulation would require a lot of power from the salve supply system to drive the information through the lines to the Master. A remote supply would be impossible.

The Meter-Bus uses both versions. The communication from the Master to the slave is done via different voltage levels. The communication from the slave to the Master is done by different current levels.

2.3.1. Master to Slave

Depending on the number of slaves connected to the system and depending on how much power is used for remote power supply a certain idle current level is defined. The idle mode, the mark state is defined by a voltage level between 20.6 and 38 V. A space state is defined by a voltage drop of 12 V. Whatever the mark state in the given window is, the space state is 12 V less down to 0 V. 0 V is an invalid state since the power supply on the bus would break down. The current remains almost unchanged during this modulation.

2.3.2. Salve to Master

Any slave is sending data to the Master by modulating the current consumption on the bus. Only one slave system can sent at one time. Bus collision must be handled by the protocol and Master Unit. The TSS721 driver unit activates a built-in current sink to modulate the current on the bus lines. The idle mode, mark state is 0 to 1.5 mA signal level. Space state is a maximum 20 mA signal level. The signal level is defined as the current flowing without idle current used to supply the TSS721 units and the remote powered slaves. The voltage level remains unchanged during this data transmission.

Since the bus is always powered during normal run mode a connected slave can sent requests at any time the bus is unused and the remote power feature can be used to supply connected salves without thier own power.

Next to the TSS721 TI also developed the TSS711 driver unit. This driver unit uses the same method to transmit the data in both directions but the TSS711 does not support the remote powering feature. The TSS711 bus system can handle also up to 255 slaves per segment. The logical levels for transmission from the master to the slaves are : 6 to 27 V for mark, 0 to 1.5 V for space. This means 0V on bus-lines are a valid state in a TSS711 system. The transmission levels for slave-to-master transmission are identical with the TSS721 transmission.

2.4. Master Unit & Repeater

As already described one Master Unit can handle up to 255 TSS721 units over a maximum distance of 1000 meters. Whenever more than 255 units are connected to the bus or distances are longer than 1000 meters, Repeaters are necessary. A TSS721 Master Unit supplies all connected slaves with power for the Driver units as well as power for the communication and , if used, with remote powering for the micro-controller system.

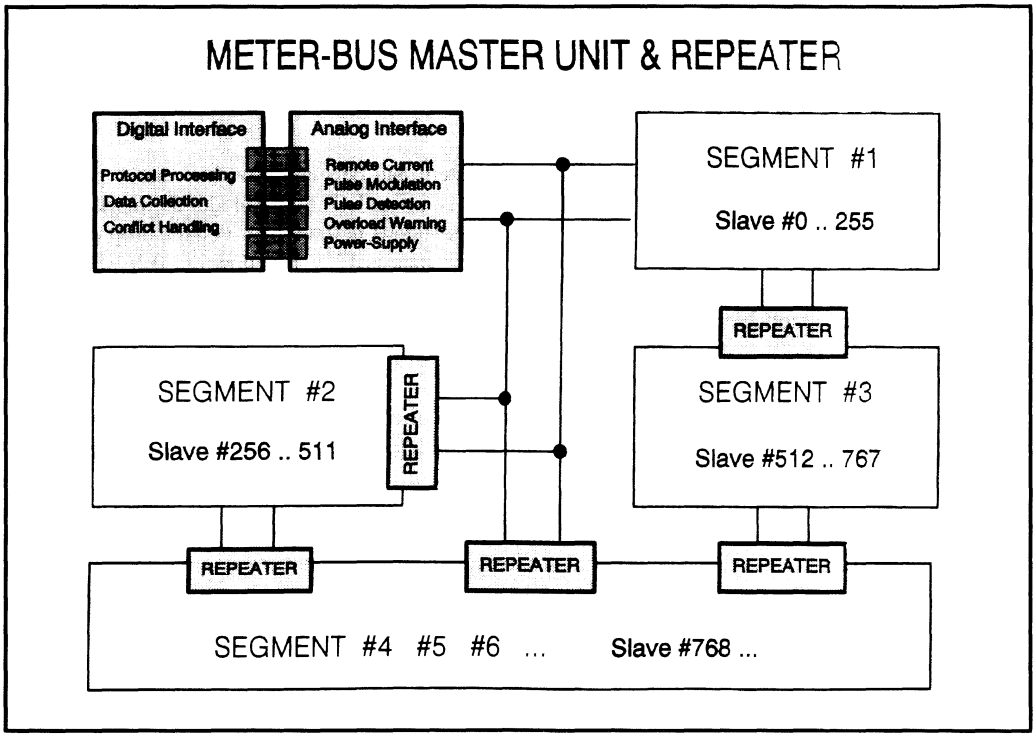


Figure 3.11 - Master Unit & Repeater

Each Repeater can handle a maximum of 255 slave units and a bus-distance of 1000 m. As many repeaters as necessary can be used in a Meter-Bus system. A Repeater serves a segment. Up to 255 segments can be connected to one Master Unit via 255 Repeaters, and even that can be expanded if necessary. In each segments up to 255 slaves can be attached to the bus lines. A Repeater works similar to a Master Unit for the served segment. The input works as an input in a slave system. It detects different voltage levels and transmits these voltage levels to the connected slaves. To a Master Unit a Repeater simulates one slave load. A Repeater uses it's own power supply to provide the slave systems in its segment with power and information.

A current signal on the bus lines in a segment is transferred by the Repeater to the main-bus lines connected to the Master Unit. Similar to a TSS721 driver unit the Repeater uses a current-sink to transmit information via different current levels. For the master station a repeater and it's connected slaves, are one slave load only.

The protocol is transparent to all connected slaves. This means for example a transmitted address is read by all connected slaves regardless which segment they are connected to. This also means that a address system must be able to address more than 255 slaves. There is no need to connect slave addresses in sequential order to one segment. Repeater and slave systems can be connected to the

Master Unit in parallel as long as the maximum number of slaves and Repeaters does not exceed 255 and the maximum distance of 1000 meters is not exceeded.

TI developed an Analog Part of a Master Unit for evaluation purposes. Since the digital part of a Master is basically defined by the protocol used on the bus lines, the unit is defined with a interface for any digital processing unit. Any customer will define its own Master Units and repeaters but all will show similar features in the analog part.

The TI Analog Master Unit expects a processor system which is controlling the data communication in a half-duplex mode. It is this processor systems task to include check-sums to the protocol, check data collision, store data in RAM, EPROM, or other media, and control different run modes of the connected slaves. This processor is not included in the TI evaluation unit. For an evaluation a PC might be used to install a prototype system.

The Master must be equipped with an isolated power supply which can supply the power for the slaves. The system must have a galvanic isolation from earth to guarantee a ground-free bus system. 255 slaves must be supplied with a maximum of 1.5 mA per slave plus additional 20% security for short-circuits in a slave or data collision.

Data transmission from slaves must be identified. Since all connected driver units and remote power slaves are bus-powered, this power consumption level must be identified as idle state. Only fast current changes after the bus system is powered are data information and must be transmitted to the digital part. When a Master Unit can adapt to the idle current consumption of a bus calibration cycle is not necessary when the bus system or slave number and type is changed.

Overload checking and short-circuit conditions are checked to avoid the destruction of slave systems and measurement data. The analog part can be used for TSS721 and TSS711 protocols.

2.5. TSS721 Transceiver

One of the major requirements for the realisation of a cost efficient Bus concept is to reduce the number of electric parts and costs for the driver interface, because the driver interfaces is a high volume product. The major objective at the TSS721 development was therefore the integration of all necessary functions in one IC with a minimised number of external part.

TSS721 Features:

- receiver/transmitter logic according to the M-Bus specification with dynamic level recognition
- adjustable constant current sink via external resistor (nominal 20 mA according to DIN standard 66258 and 66348)
- polarity independent
- power-fail functions
- backup supply functions
- remote powering

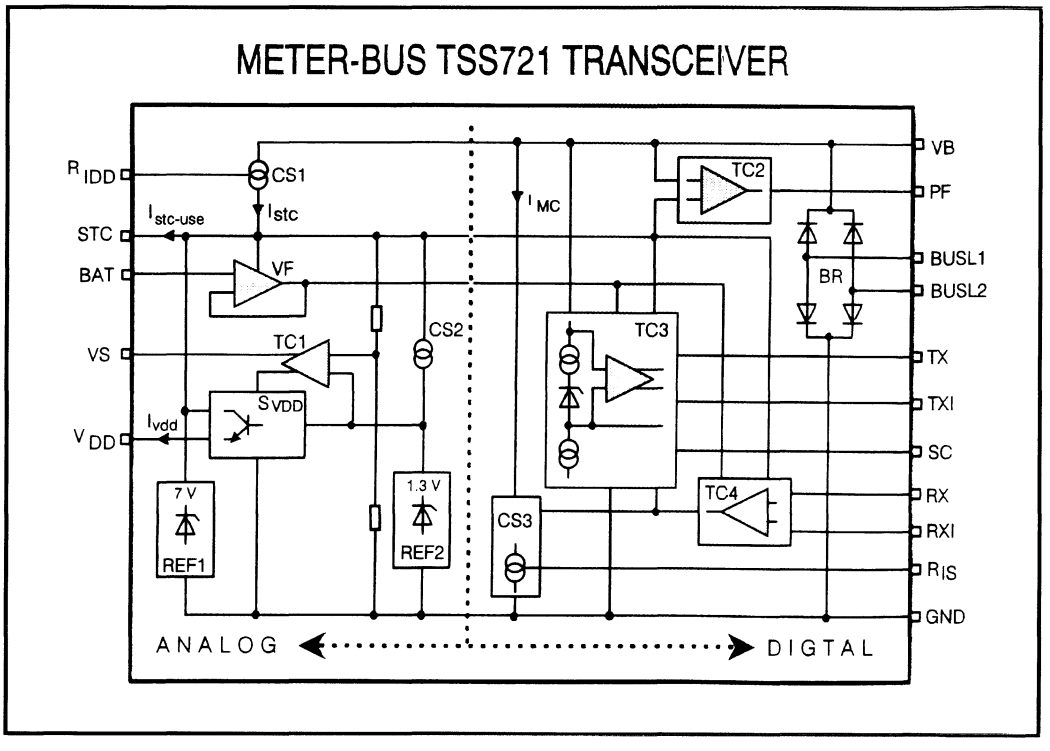


Figure 3.13 - TSS721 Transceiver

2.5.1. Analog Part

The bus lines are connected to the pins BUSL1 and BUSL2. The rectifier bridge rectifies the bus voltage and makes the device polarisation independent. This signal is then available on the pins VB and GND. If the chosen bus voltage is very low and the internal voltage drop can not be accepted, the bus voltage can be supplied to the driver via the pins VB and GND. The voltage drop in the Schottky rectifier diodes is then eliminated, but the bus-lines are not polarisation independent any longer.

The Bus voltage supplies several constant current sources. These constant current sources are the power supply for the entire TSS721 as well as for the connected module for the remote power supply. The concept to take all power supply out of the constant current source, is required by the M-Bus. Demand is a constant quiescent current from the bus. A current variation in each connected module would be added up and cause erroneous transmission.

The constant current source CS1 is the main power supply and can be programmed by an external resistor typically in the range of 400 µA to 960 µA. The resistor is connected to the RIDD pin and the current I_{CS1} is calculated by the following formula:

$$I_{CS1} = \frac{U_{RIDD}}{R_{IDD}} * 25$$

I_{CS1} = constant current of CS1
U_{RIDD} = reference voltage on pin RIDD (typ. 1.26 V)
R_{IDD} = 33 kΩ .. 80 kΩ

The current I_{CS1} splits up into the current for the device supply and the charge current for a support capacitor. The support capacitor provides current for a connected module at current peaks and in case the bus power fails. The capacitor is connected to the pin SC.

When the bus voltage is switched on and the TSS721 is powered a certain time is required to charge the support capacitor. Since the load current is limited it may, in some case, take up to one minute until the TSS721 starts the initialisation routine. REF1 tracks a capacitor voltage of typical 7.0 V and activates a Zener diode to take additional current. As already described a constant load on the bus is mandatory.

TC2 tracks the bus voltage. In the case of a power fail the power-fail pin PF is activated. This pin may be used to detect a power failure and initiate a safe shutdown of the micro-controller system. During the shutdown, power can be supplied by the support capacitor. In case the capacitor voltage sinks under typical 4.0 V the comparator TC1 switches off SVDD since it is not possible to regulate the voltage on VDD to a constant level of 3.2 Volts any longer. Then the low-active pin VS can be used to control a FET switch which may activate a support battery.

2.5.2. Digital Part:

The signal TX and TXI, the inverted output, generate a digital output depending on the voltage levels on the bus. A mark state generates a high level which is defined by the BAT input, the supply voltage of the slave system. The RX pin, or the inverted input, activates the current sink in case the salve system need to send a logical high. The level acknowledgement is again controlled via the input BAT. RIS is a control input and must always be connected to ground, via a resistor.

2.6. TSS711 Transceiver

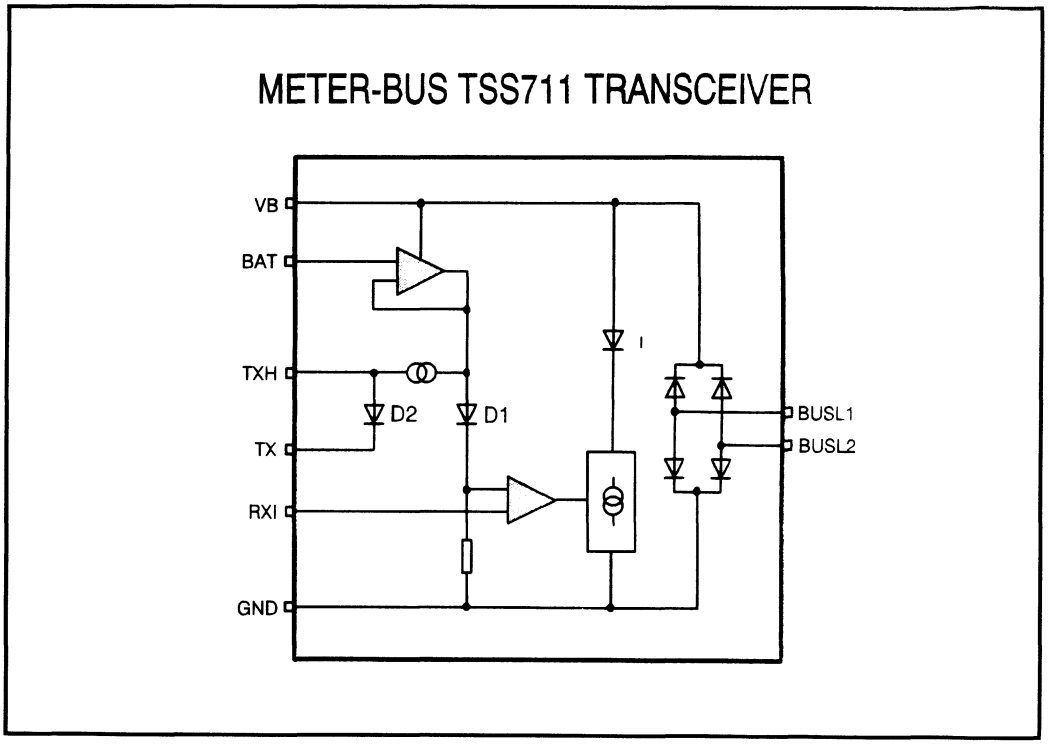


Figure 3.14 - TSS711 Transceiver

The TSS711 is a cheaper bus driver which can be used when no remote powering is needed. The TSS711 use the same type of physical transmission as the TSS721 does. The space level is 0 V, which means remote powering is not possible.

The voltage level delivered on BUSL1 and BUSL2 is adapted to the voltage level supplied on the BAT pin. If Mark is transmitted TX the transmission output is set to the voltage level BAT. A space initiates a low level on the output TX.

RXI is the inverted data transmission input. The internal current sink is activated on a logical high. Since the diode D2 is integrated between the input TX and RXI it is possible to connect both pins and therefore also support a micro-controller, which use one I/O line for data transmission only. TXH can be used if this function is handled on two different pins of the micro-controller system and the voltage drop on the diode can not be excepted.

2.7. Slave System Supply Modes

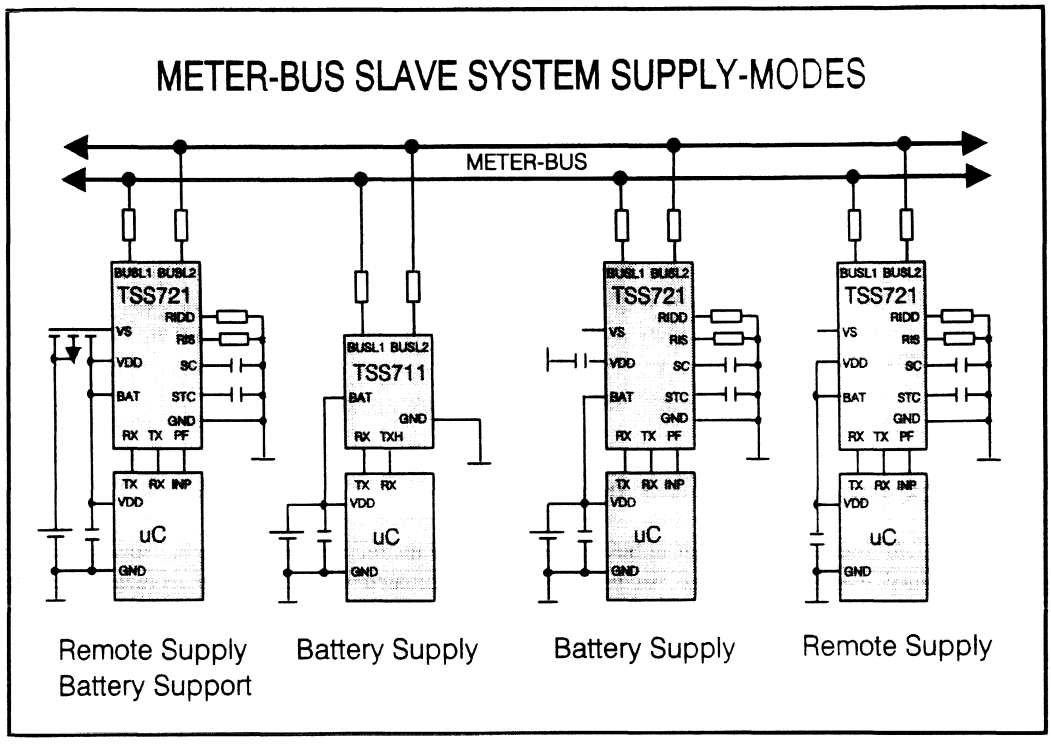


Figure 3.15 - Slave System Supply Modes

The TSS721 utilise three different energy supply modes of the connected slave system. The three modes are :

- **Local Supply** : energy for slave supplied local, e. g. by battery
- **Remote Supply**: energy for slave supplied by the bus
- **Mix Mode:** energy for slave supplied by bus, in case of power-failure a backup battery is activated

When power for the slave is supplied locally, normally by a battery, the TSS721 is working as a pure driver device only. The information on the bus are supplied, in the right voltage format to the slave system. The communication initiated by the slave micro-controller system is transferred in current modulations. For security reason it is advisable to add resistors (430 Ω) between the bus-lines and each driver device. Using resistors, if there short-circuit, the additional power consumption can be tracked

by the Master Unit and a alarm initiated. Even though the defective unit can not be addressed any longer all other devices connected to the bus can still be accessed.

The TSS711 does perform the same task as the TSS721 in this mode. The voltage level for the Master Slave transmission are different, but both systems can be used on the same bus-lines when all slave systems are battery powered.

When power for the slave is supplied remotely the TSS721 can only be used. The driver unit performs the data transmission. The module is fully powered by the bus. In case of a voltage breakdown on the bus the power-fail signal is activated. This enables the processor to save important data and initiate a safe shutdown. The power for this is delivered by the support capacitor.

In a mix-mode the slave system is supplied by the bus-lines as long as power is available. A power failure is also indicated by the power-fail pin PF. Additional to this a backup battery is activated by a FET-switch, controlled by the VS pin. The backup battery is active during the bus-off time only. The power supply for the salve system is guaranteed. Since the power fail pin is still usable for the application to track the a power failure, a low power consumption mode can be started. Thereby, the capacity of the backup battery may be minimised.

In all modes the TSS721 as well as the TSS711 are always powered by the bus-lines and do not use any slave system battery capacity.

2.8. TSS400/4 Standard Bus System

The TSS400/4 Standard has a built-in bus system. A single instruction enables the bus independently from executed macro instructions. An interrupt can by initiated when the bus becomes active. A selectable input trances the bus. A TSS711 or a TSS721 can be used to transmit data via long distances. Up to 256 systems can be connected to the bus. This number can not be expanded by repeaters.

The communication is unidirectional. The slaves sending information to a Master Unit only, not the other way round. After the bus is activated by a high signal each salve interrupts the current program execution and sends a predefined set of registers to the Master Unit. The protocol includes the salve address. Each address can only be used once in a bus system.

Depending on the salve address each slave is sending its information in a time window. This is a very easy and efficient way of building up a multi-slave system. No 'request to sent' protocols needs to be transferred on the lines. After a rising edge on the bus all slaves are synchronised to a following pulse and then start a timer which elapses in the time-window responding to the slave address. The data transmission is done via the I/O pin. This pin is also used to communicate with the EEPROM's, therefore it is necessary to multiplex this output.

The content of five storage registers as well as the slave address are transmitted. The storage register defined for the communications should be loaded with consumption data, measurement results and so on, during normal program execution. A transmission speed of approx. 600 Baud can be reached. A 4-bit protocol is used for transmission. This is convenient since the TSS400 holds a 4 bit CPU.

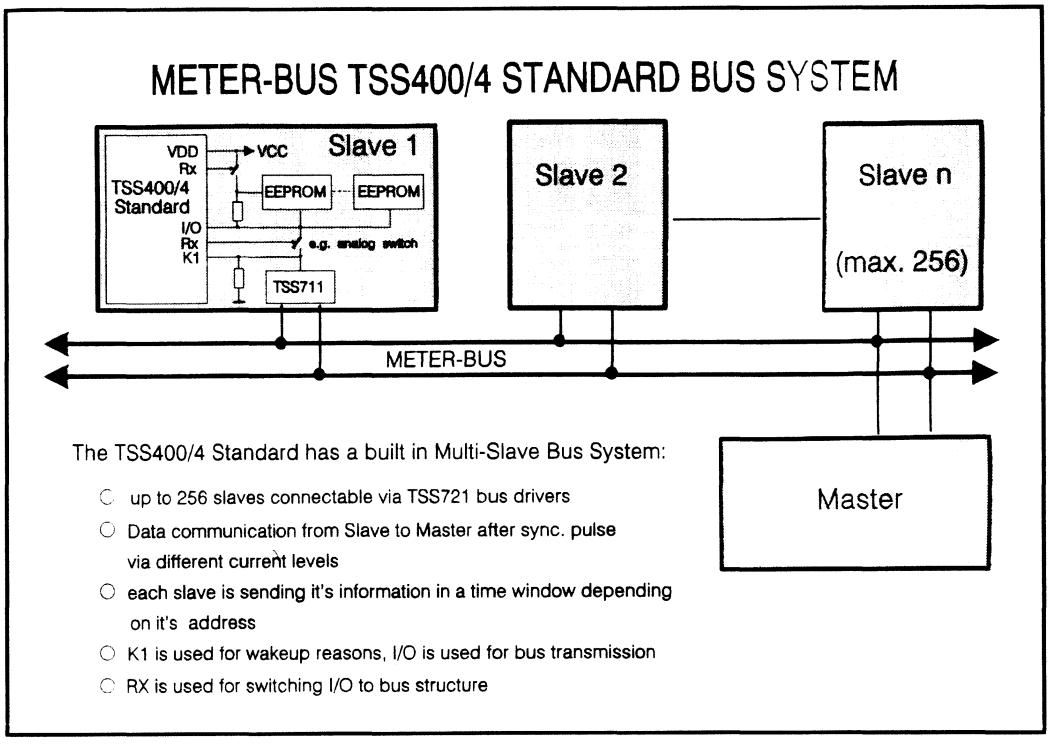


Figure 3.16 - TSS400/4 Standard Bus System

The bus function may be disabled during time critical parts in the user software, were no interruption can be tolerated. A macro command is performing this. Once a bus communication is initiated by the Master Unit, this slave would fail to answer in its time frame. Just an other readout would be necessary to collect the data from this device.

The TSS400 Standard Version can also be used to build up bus-systems with different protocols but this must be done by macro instructions in the user program. Since the TSS400 Standards have to communicate with serial EEPROM's the speed of such a data transmission is limited. A mask version naturally shows much more flexibility in protocol handling and higher speed.

Section 4
Data Transmission

Section Contributions by:

Andrew Faulkner
Simon Ramsdale
Tim Ardley

Contents Section 4.

1. Introduction

1.1. Data Transmission

This section places focus on a range of data transmission products supported by the linear department of Texas Instruments.

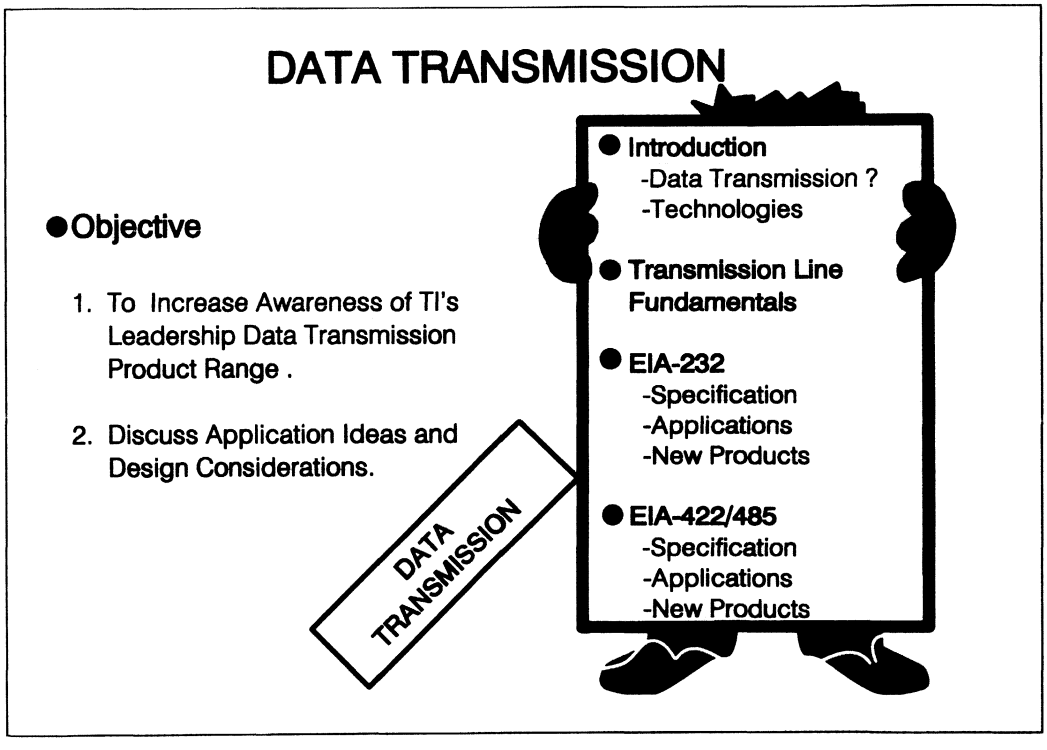


Figure 4.1 - Data Transmission

1.1.1. The Need

Specialised data transmission products arose from a need to send data over long distances in conditions often susceptible to noise interference. Although TTL products can be used they are far from ideal, and over the last ten years products optimised for the task of data transmission have been developed. These devices characteristically yield greater current output drive capability and/or wider operating voltage ranges, thereby offering improved noise immunity and line drive capability. Furthermore speed, power consumption, higher levels of integration and robustness are becoming standard requirements.

Texas Instruments has been a leading supplier of interface products for many years, and as you might expect is continually innovating new fields. Although the following sections are limited to the more common interface standards, TI is actively involved in many new emerging standards and markets. Such markets include; high performance backplane standards (IEEE.896 Futurebus+) and automotive multiplex wiring. The reader is advised to consult the accompanying literature sheet or contact a TI representative for information on these product areas.

With their considerable expertise in design, product definition and its range of technologies Texas Instruments is the ideal choice as semiconductor vendor for data transmission products.

1.1.2. About This Section

The following pages take a practical rather than theoretical approach in an attempt to give the practising engineer an insight into industries most commonly used serial standards - namely the Electronics Industries Association's (EIA) serial standards, EIA-232, RS-422 and RS-485. The data transmission section is divided into five main parts;

1. Introduction; Provides an overview of transmission scheme classifications followed by a discussion on technology choice.

2. Transmission line Fundamental; This section aims to make the reader aware of some of the potential problem areas in implementing digital data links and offers ways in overcoming these problems by discussing basic transmission line fundamentals.

The two main sections, **3. EIA-232** and **4. RS-422/485**, briefly explains the merits of each standard followed by overviews of Texas Instruments' key products and their application. The latter section also contains general guide lines for implementing differential data transmission schemes. To further aid the reader section 5 contains a data transmission trouble shooting guide.

1.1.3. Further Information

More comprehensive data on the products discussed throughout this section can be found in the current ***interface circuits data book.***

1.2. Which Transmission Scheme?

The following figure shows just one example of a data transmission network. It shows many different types of interconnect within a computer system. Although all are concerned with the exchange of data the data transmission scheme used, types of cable and system capabilities vary enormously.

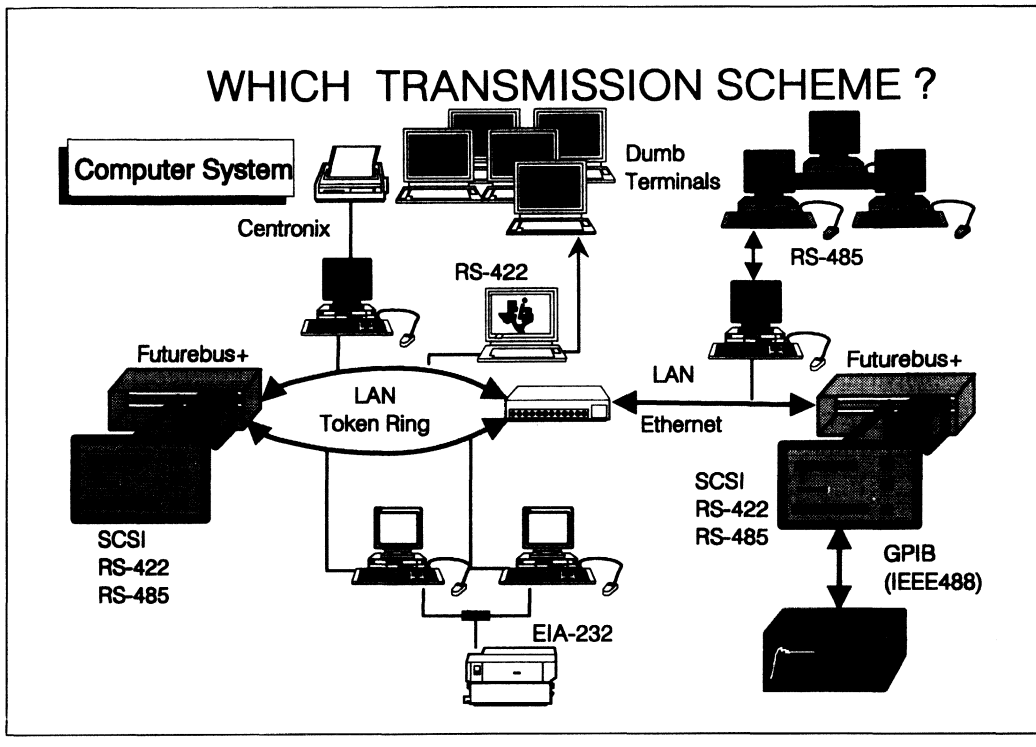


Figure 4.2 - Which Transmission Scheme?

1.2.1. Parallel or Serial? / Single Ended or Differential?

Transmission schemes may be broken into two main categories, parallel or serial. These categories may be further classified by the type of interface circuitry used; Single ended or differential.

Differential techniques are generally used when noise interference could be problematic or when long distances are to be covered at high data rates. ***Single ended*** techniques are used when cost is an issue or where short distances are to be covered, this is typified by board level logic, back plane systems or short data link applications.

Parallel systems are generally used where large amounts of information are to be transmitted over relatively short distances but at high speed (parallel systems generally require one line or cable per digital bit.). The backplane or board level bus is the most general and widely used of the parallel bus types. Other examples are the microprocessor specific Multibus™ and VMEbus™. The ever increasing need for even higher backplane data rates and optimised flexibility without being tied to a specific microprocessor architecture is solved by the rapidly emerging standard Futurebus+. SCSI (Small Computer System Interface) is also a parallel bus structure with increasing use for data transfer between PC/Workstations and memory storage systems including Winchester hard disk drives. Finally, IEEE488 allows parallel data transmission between measuring equipment and the PC, thus

Multibus is a trade mark of Intel, VMEbus is a trade mark of Motorola.

allowing the user to set up automated test routines.

Serial busses find their applications in longer length data transmission systems where the cost of running parallel cables would be cost prohibited. The most widely used, and known, serial data transmission standard is the EIA-232. Although originally developed for a modem to terminal equipment interface, EIA-232 has become widely used as an interface for nearly all PC peripherals. For longer line lengths and better noise immunity the serial buses RS-422 and RS-485 are preferred. The differential RS-485 is a popular standard, becoming extensively used in multi-station, high data rate applications - particularly due to its close links to SCSI.

At the longest line length level are Local Area Networks (LAN), like Token Ring and Ethernet. used to network computer equipment's. TI has recently introduced a transceiver function to address the requirement of the Ethernet repeater function, the SN75ALS085 (See the interface circuits data book for further information).

Other types of LANs can be found within the factory (factory automation) for interconnecting process controllers and sensors. One such developing standard is Fieldbus, which embraces electrical specifications as well as protocols.

Home Automation, a domestic LAN, is a growing area for future data communication systems. A standard like CEBus (Consumer Electronics Bus) or the European Esprit projects home system bus are examples of bus structures including more that just the electrical specification. These specifications include a robust protocol for controlling consumer appliances over an intelligent network within the home environment.

Another key growth market is automotive multiplex wiring. The need for very robust and fault tolerant driving/receiving elements is never so apparent as in automotive applications, especially when used in safety critical systems. Emerging automotive standards like CAN, Controller Area Network, VAN and the US. S.A.E. J1850 standard are set to play a key part in this area.

1.2.2. The need For Standardisation

The primary objective of any data transmission system is the distribution of information without error. Data transmission circuits are chosen primarily on the data rate, distance to be covered and system cost - whilst compliance with industry standards is necessary to maintain system compatibility.

There are a wide range of standards available for implementing digital data links. Some are very sophisticated like the Consumer Electronics Bus, for home automation, and Futurebus+, high performance backplane. These embrace, as discussed, specifications for protocol (timing and control) as well as the electrical and mechanical aspects of the interface. Others, such as the EIA-232 interface contain only basic timing information while the RS-422 and RS-485 specifications contain only electrical information.- although the timing and control of the interface still needs careful consideration.

1.3. Interface Standards

The electrical industries association (EIA) was among the first groups to recognise that industry needed standard guide lines from which to design digital data links.

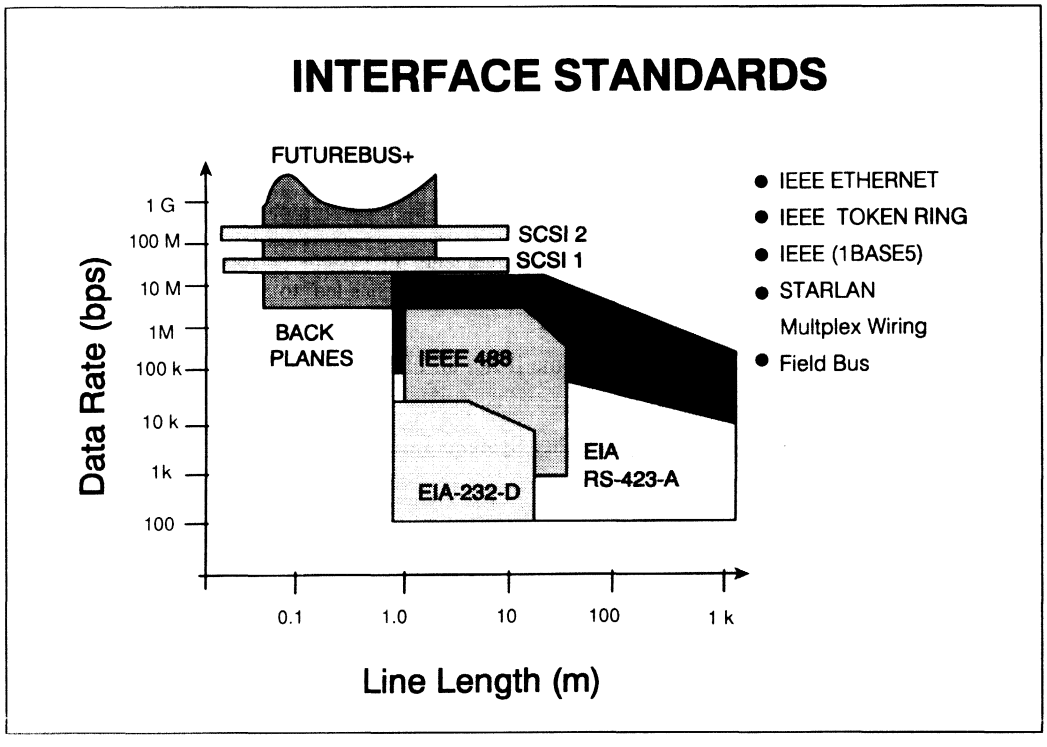


Figure 4.3 - Interface Standards

Figure 4.3 shows the common standards and compares their data rate and line length capability against other known standards.

Parameter		EIA-232	RS-423-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		±25	±6	6 to –0.25	12 to –7
Driver Output	Unloaded	±5	±3.6	±2	±1.5
Levels (V)	Loaded	±15	±6	±5	±5
Driver Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/µs (Max.)	External Control	NA	NA
Driver Output Short Circuit Current Limit (mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to –7 or 12 V

Driver Output Resistance -	Power on	NA	NA	NA	12 k
High Z state (Ω)	Power off	300	60 k	60 k	12 k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

1.4. Application Demands

The consumer's ever increasing demand for improvements in system performance, coupled with weight/size/cost reductions, lower running costs and reliability has led to a demand for increasingly complex semiconductor chips.

The underlining requirements demanded by some if not all of modern data transmission applications can be summarised as;

- **Increasing complexity / Higher Systems Integration**
- **Robustness**
- **More functions Lower Price**
- **Increased speed/power performance**

1.4.1. Increasing complexity / Higher Systems Integration

This is borne out by considering almost any system, particularly in the computer industry, where whole functions are mopped up into ASIC's (Application Specific Integrated Circuits) or highly system integrated processors. For example a minimal microcomputer architecture requires a central processor, memory (RAM and ROM) and input/output (I/O) control. Previously this would require several chips - it now can be implemented in just one, the single chip micro. The interface circuitry is no exception, consider the asynchronous communication element (ACE) that controls the serial interface between computer and peripherals. This has migrated from a multi-chip solution to a single dedicated controller, controlling up to 2 serial ports and one parallel port (TL16C552). It is quite clear that before long, line driving/receiving functions may also be integrated along with the controller chip.

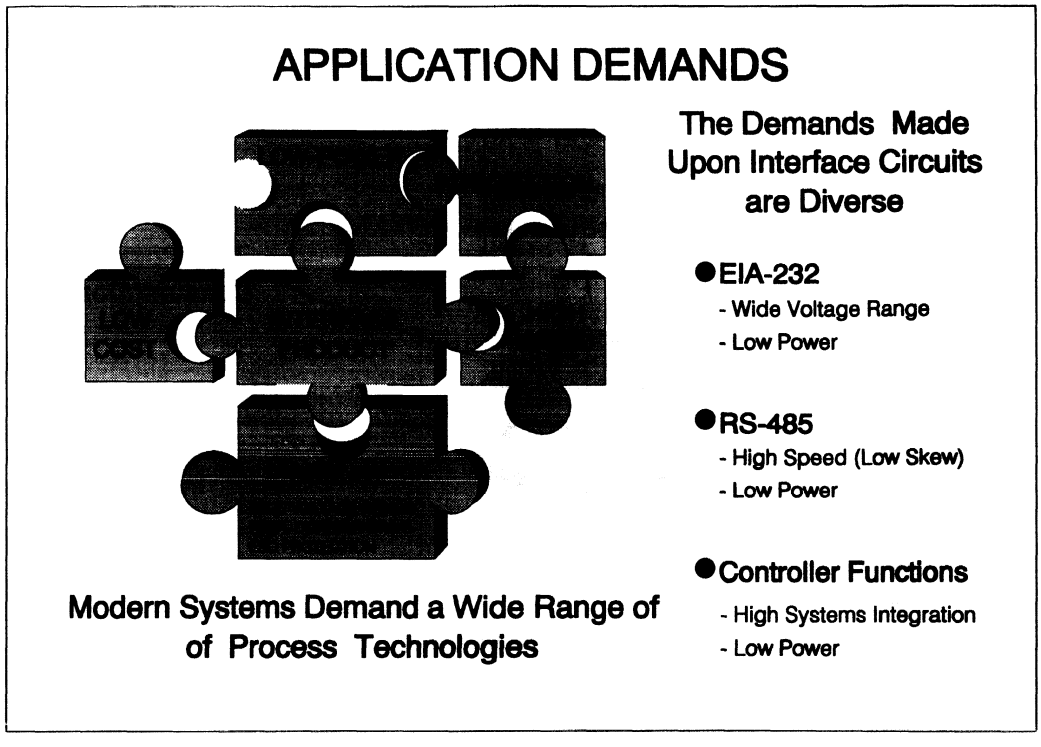


Figure 4.4 - Application Demands

1.4.2. Robustness

Including more functions on chip reduces system chip count, not only bringing savings in board real estate but in system reliability. However should a fault occur the increased complexity of these chips has made the task of fault identification more difficult, especially for the field service engineer. This has led to more robust design techniques and the inclusion of self test and diagnostic capabilities on chip. For example the **SN75186** EIA-232 driver/receiver contains a loopback feature allowing self test and the Futurebus+ chip set will include JTAG capability.

1.4.3. Increased speed/power performance

The old adage, 'You can't have high speed and low power' is no longer acceptable. High performance systems are now required either to operate permanently or temporally from battery cells, thus demanding low power consumption.

1.4.4. Cost

Generally speaking these performance advantages will be more expensive than the unit purchase price of the handful of components they replace. But when considering the increased reliability, saving in assembly and board population cost the overall system cost will be very much reduced.

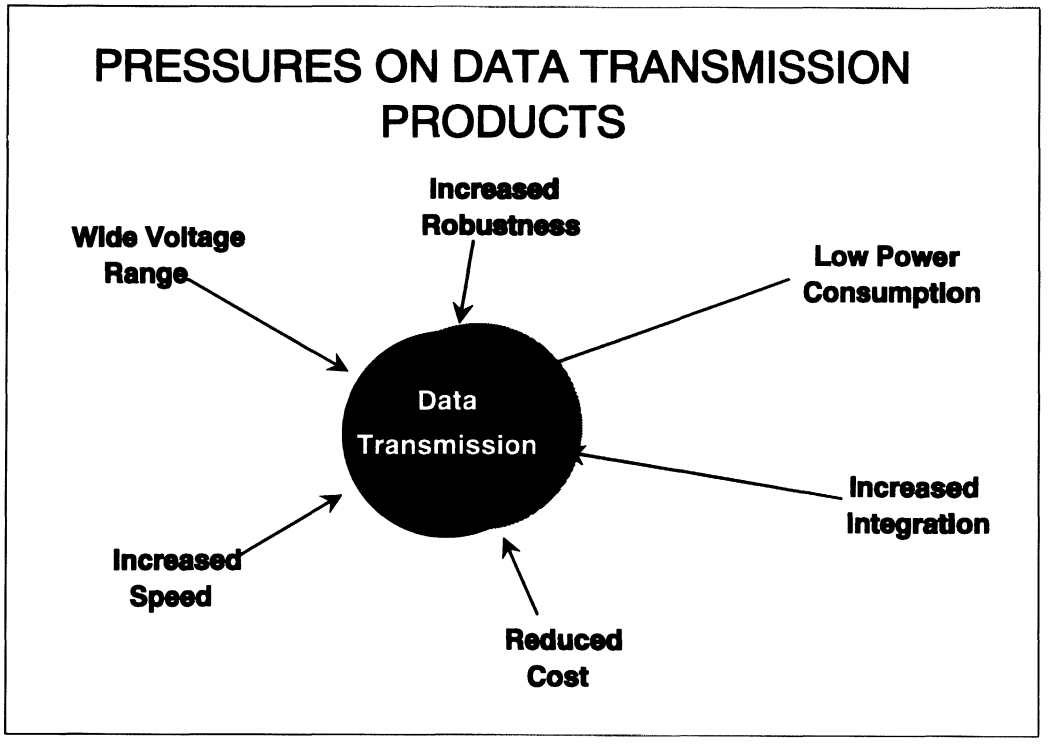


Figure 4.5 - Pressures on Data Transmission Products

The diverse range of applications and the markets demand for increased functionality, robustness and low power, require a broad range of process technologies. Furthermore the choice of the most appropriate technology is not a trivial matter as needs are often conflicting, i.e. high speed and low power. However, the dominating factors are usually speed and voltage operating range.

Although the list of technologies to choose from is seemingly endless, several key categories emerge with all others a variation needing slight process modifications. The categories are;

i) **Analogue Bipolar (operational amplifiers)**

ii) **Analogue CMOS (LinCMOS range of operational amplifiers)**

iii) **Digital CMOS (HCMOS '74 range)**

iv) **Digital Bipolar ('LS74 range)**

Broadly speaking bipolar technologies offer speed and robustness, whilst CMOS technologies provide low power consumption and high packing density. The analogue process variations offer increased robustness often at the sacrifice of packing density. There are of course exceptions to every rule.

1.5. Technology Solutions

Although a detailed discussion of technologies is beyond the scope of this section, it is worthwhile briefly considering the key technologies and the benefits they offer for data transmission applications. Until recently, semiconductor technologies used to manufacture line interface circuit devices have been based upon those technologies and processes used to build digital logic circuits. This resulted in circuits having mainly bipolar NPN structures. For example the change from ordinary bipolar to low power schottky (LS) and advanced low power schottky (ALS) technologies in digital logic devices, has been closely followed by line circuit devices.

In recent years there has been a change in the digital logic field towards device structures based upon CMOS processes. CMOS offers the obvious attractions of low quiescent power consumption and operating speed comparable to that of many bipolar technologies. The same change in technology for line circuits has not been so fast. One of the primary reasons for this is the need to make output transistor stages very large in CMOS technology to enable them to source the required high currents (as much as 250 mA). The input capacitance of these large CMOS stages also requires much higher drive currents from the bias circuits. At high frequencies of operation CMOS line circuits therefore lose some of their attraction because bias currents become so high. It is also difficult to build CMOS devices that could withstand the relatively high voltage levels used by some slower, older line interfaces, for example EIA-232. CMOS is particularly problematic when the externally applied voltages are taken outside its supply rails. This causes a phenomena called 'latch-up' to occur, and is due to a parasitic diode structure in parallel with the output transistor. Latch-up causes the device to draw increasing amounts of current until the device self destructs.

The most promising route forward in technology for line interface devices would appear to be through the use of a BiCMOS technology (a mixed digital CMOS and digital bipolar process). Such progress has again already been made in the digital logic field. BiCMOS technology combines the speed and high voltage capability of bipolar processes with the low supply currents and high input impedance's of a CMOS process. This is now to available for line interface circuits with the development of the AM26C31/32. See the RS-422 section for performance comparisons. Another merged technology is the analogue LinBiCMOS™ process which combines an analogue bipolar process with an analogue CMOS process. Enabling devices which are not only low power but are extremely robust and have high speed capability.

The LinBiCMOS process is set to be a major technology for TI's new data transmission products, allowing bipolar high voltage capability to be merged with high density low power CMOS.

Another key advantage of a merged technology design is that generally a cell based design approach is taken. For example cells developed for one device can be added to other designs, thereby reducing device development time and increasing the number of device options available.

A brief resume of Texas Instruments' key data transmission technologies is given in the following figure.

LinBiCMOS is a trademark of Texas Instruments.

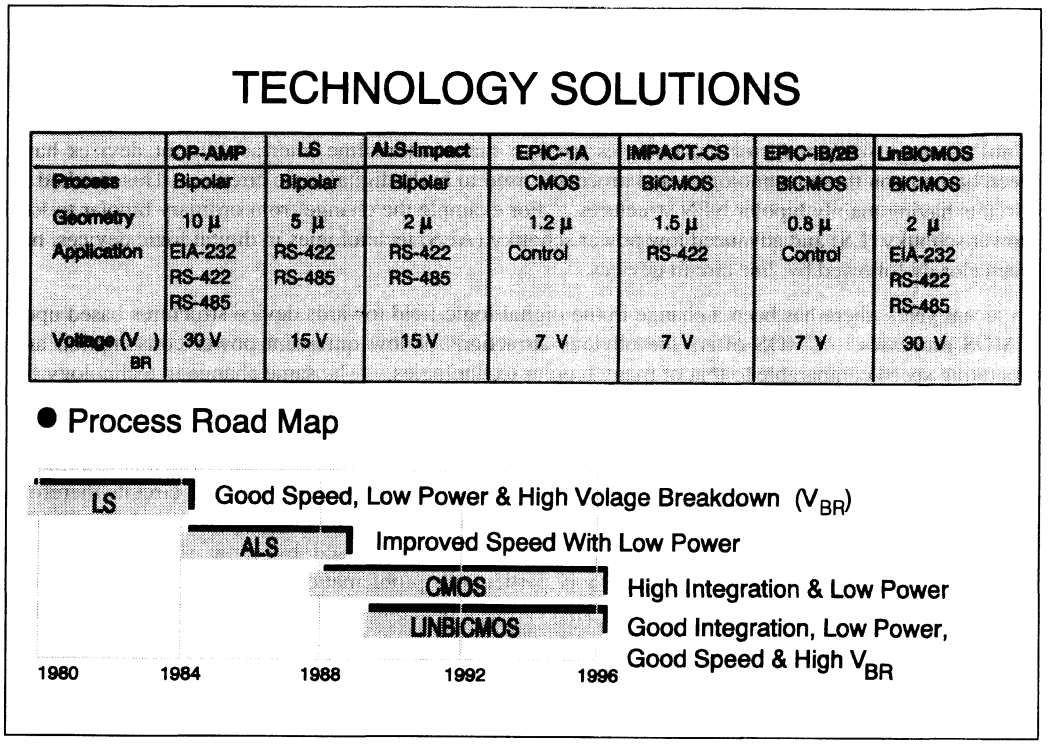


Figure 4.6 - Technology Solutions

Not listed in the box above is Texas Instruments' BiMOS process. This process is a derivative of a bipolar process with enhanced PMOS devices giving extremely low power. For example a power saving of 99% can be made over existing bipolar designs.

Although the requirement for optimised processes will continue, the trend towards merged technologies like LinBiCMOS will gain momentum, especially when little or no compromise in device specification is encountered.

1.6. LinBiCMOS - State-Of-The-Art Interface Technology

Although originally developed as a technology for designing mixed analogue/digital ASIC's, LinBiCMOS now looks set to make a major impact in the field of interface devices.

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3 µm pure CMOS technology with 16 V capability, making it ideal for the design of low power analogue products such as op-amps and analogue-to-digital converters (many examples of which are discussed elsewhere in this book). By shrinking the geometry's to 2 µm and adding a high performance 30 V bipolar structure, a new "analogue" merged bipolar/CMOS technology has been produced.

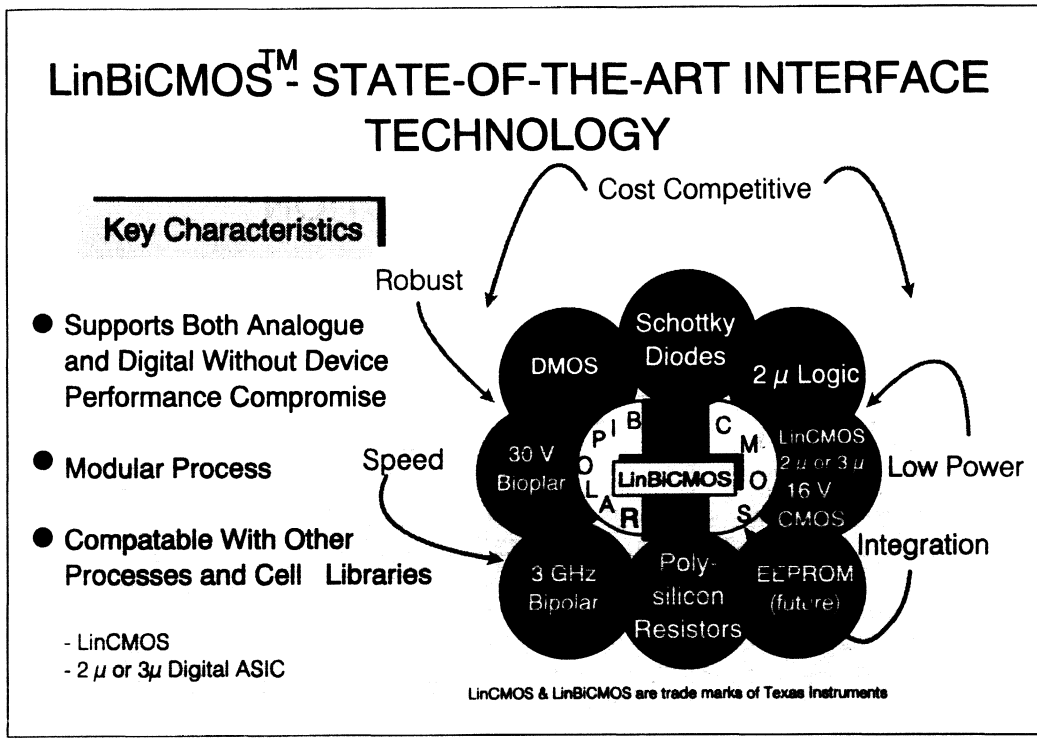


Figure 4.7 - LinBiCMOS, State-Of-The-Art Interface Technology

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost, as many "nice to have" features can make a process too expensive to address a wide range of opportunities. By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective.

Modules available for LinBiCMOS include high speed NPNs (with an f_T of 3 GHz compared with 500 MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and schottky diodes for clamping.

Another key benefit of LinBiCMOS is its compatibility with TI's ASIC 2 μm logic cell library. This means that any logic required within a new design can be quickly designed and simulated as each of the cells are already very well proven.

1.7. LinBiCMOS Cross Section

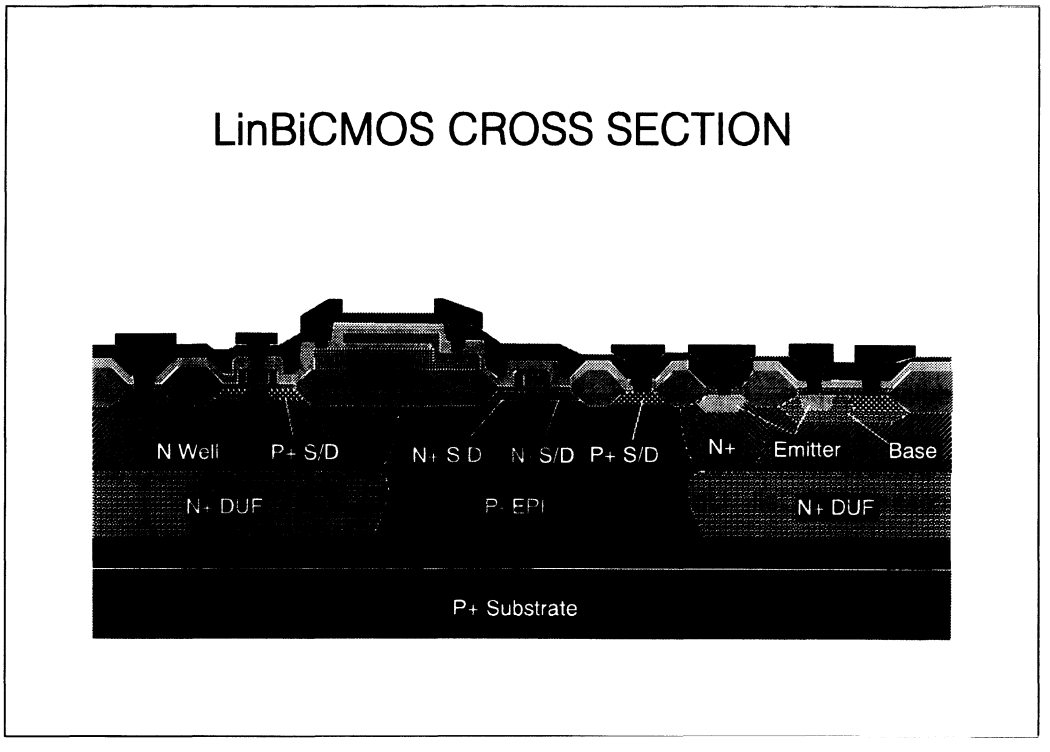


Figure 4.8 - LinBiCMOS Cross Section

By combining bipolar with CMOS it is possible to use each structure to its best advantage. CMOS is ideal for designing logic and for interfacing with external logic devices (controllers etc.), whereas bipolar is well suited to high voltage/current areas such as the line output stage.

With its high voltage capability and good switching speed, LinBiCMOS is ideal to address standards such as EIA-232 and RS-485. The RS-485 standard for instance demands driver output that can be shorted to +12 V and -7 V without damage, this is particularly difficult as only a single 5 V supply is available, meaning that parts of the chip must be designed to operate well outside its supply rails.

Development work on LinBiCMOS is still underway, and in 1992 TI expects to offer DMOS and EEPROM modules. EEPROM (electrically erasable programmable memory) offers some very exciting opportunities such as line driver/receivers with their own built in address.

To date LinBiCMOS has been used for both custom IC developments and catologue products. 1991 saw the introduction of products for both EIA-232 (MAX232) and RS-485 (SN75LBC176).

1.7.1. Technology Case Studies

The following case studies highlight some of the key technologies and their suitability for a given application and function.

1.7.1. Controller Functions

Controller functions usually present a simple technology choice. The major requirements, irrespective of application, are for low power consumption and high integration. Robustness is not generally a major concern as the device is usually tucked safely away in the heart of the equipment. High integration is important as systems designers strive to reduce chip-count, hence saving board space and increasing reliability. This requires a technology with high packing densities and small geometry's. A digital CMOS process, of which there are many variations, with 1µm geometry is the ideal choice.

1.7.2. EIA-232

EIA-232 is a single ended, serial standard commonly used to connect the computer to its peripherals, e.g. printer. Although it has a relatively slow data rate, 20 kbps, and can only be used only over short distances,<15 m, it is very low cost and easy to implement.

By far the most demanding requirements for the EIA-232 line drive/receive circuits is the ability to operate from dual supplies of up to ±15 V. As with all interface devices a high degree of robustness is demanded. Implementing on-chip ESD and transient protection circuits which can operate within such wide voltage ranges is difficult . The natural choice would be a wide voltage bipolar technology with its inherent robust structures (commonly used by operational amplifiers). In fact the vast majority of industry standard devices for EIA-232 have been designed using this process. However modern equipment increasingly requires battery operation (lap top PC's and hand held test equipment) thus low power consumption is also required. Generally a low power digital CMOS process would be incapable of withstanding the wide voltages required therefore a low-power bipolar or mixed bipolar and CMOS process (merged technology) would be the ideal.

1.7.3. Differential Applications

Termed a multi-point standard or mini LAN (Local Area Network) RS-485 allows up to 32 driver/receivers to be connected to a single line. The standard is fully differential, permitting greater line lengths (up to 1200 m) at high data rates (up to10 Mbps) to be driven.

Since the cable travels long distances, signals becomes very susceptible to cross talk and EMI, and although greatly reduced by the differential nature of the line robust devices with wide voltage operation are still needed. High speed and low power are also major requirements, making a low-power bipolar technology with high speed transistors the logical choice. Such a technology is the Advanced Low Power Schottky process (ALS). For applications requiring further power reductions, particularly telecommunications, a mixed bipolar and CMOS process would be needed. Generally a digital CMOS process would be incapable of handling the wide voltage common mode range of -7V to +12V for RS-485 applications.

1.7.4. IEEE Futurebus+

Futurebus+ is a high performance standard for computer backplanes. A backplane is the main communications highway between the CPU and option cards. It allows the CPU to exchange data, status, address information with its sub system modules (memory, co-processors etc.). The demands made by Futurebus+ on processing technologies is enormous. Firstly it needs highly complex controller circuits to take care of bus arbitration and protocol control, and secondly it requires high speed low power transceiver functions to drive the backplane.

Backplanes are particularly difficult to drive, particularly as each card plugged into the system contributes a capacitive load to the system, thus requiring greater current from the drivers output stages.. Consequently devices with high current drive capability are needed, 80 mA to 100 mA for Futurebus+. As the voltage swing of a Futurebus+ transceiver is only 2 volts then the wide voltage ranges offered by the analogue technologies are not required. A merged digital process could be used. This would also offer low power, which could be a significant factor when considering the number of devices required for a 32 bit+ bus.

The above case studies demonstrate that a serious supplier of data transmission devices needs to have a broad range of optimised technologies as well as merged technology capability.

1.7.2. Protocols

The majority of the text in this section is concerned with the electrical aspects of the interface. However every interface needs some form of control to provide a set rules to define the meaning and order in which data should be sent (this is dealt with briefly in the EIA RS-485 section). Termed protocols, these rules can be implemented by the microprocessor, or increasingly by a dedicated communications controller. In the past, electrical specifications have been kept separate from the protocol (which have usually been left to the systems engineer to devise) the consequence of which is incompatibility between systems even when employing the same electrical standard (RS-485, etc.). The trend today is to produce all-embracing standards that cover the electrical, mechanical and logical (protocol is contained in this group) specifications. Examples of this can be found in many of the standards just highlighted.

2. Transmission Line Fundamentals

2.1. System Influences

Before studying the more practical considerations of implementing a digital data link, an understanding of the signals behaviour is needed. More specifically a method of identifying potential problem areas and ways in which to overcome them is necessary. By an appreciation of these basic fundamentals the reader will be better placed to implement reliable and efficient digital data transmission systems.

For identification and simplicity purposes digital communication within a system can be divided into three distinct areas;

i. **Transmission of digital data between integrated circuits on the printed circuit board.**

ii. **The transfer of data between circuit boards via the system backplane.**

iii. **The transfer of data between separate equipment's or peripherals over still longer distances, for example by using serial communication standards like EIA-232 or RS-485 links.**

In the first two instances, printed circuit board and backplane communications, data transfer usually takes place with TTL or CMOS logic level signals. Even so, the speed of signal down the backplane system will be slower than that of the printed circuit system, simply because of the differences in the electrical characteristics between the printed circuit track and backplane wiring. These differences in electrical characteristics become even more conspicuous when using high speed, long distance communication links such as the multipoint RS-485 standard.

At low data rates a cable can be regarded as a pure short circuit, and it can be assumed that the propagation delay of the signal along the cable is negligible, and will not impact the overall system performance. This type of system assumes all loads are lumped together to form a single load. However as data rate and distance increase then the speed and shape of the data signal starts to be governed not only by the device but more by the electrical characteristics of the cable, i.e. its capacitance, inductance and resistance. This may lead to degradation in the signal quality. Not only will the electrical properties of the cable cause a signal degradation but also external sources of interference, for example electromagnetic interference (EMI) and cross talk coupled from adjacent lines.

It is obvious therefore that the occurrence of these limitations should be recognised and comprehended into the design of a digital data communications link, after all a cable is not always "just a piece of wire".

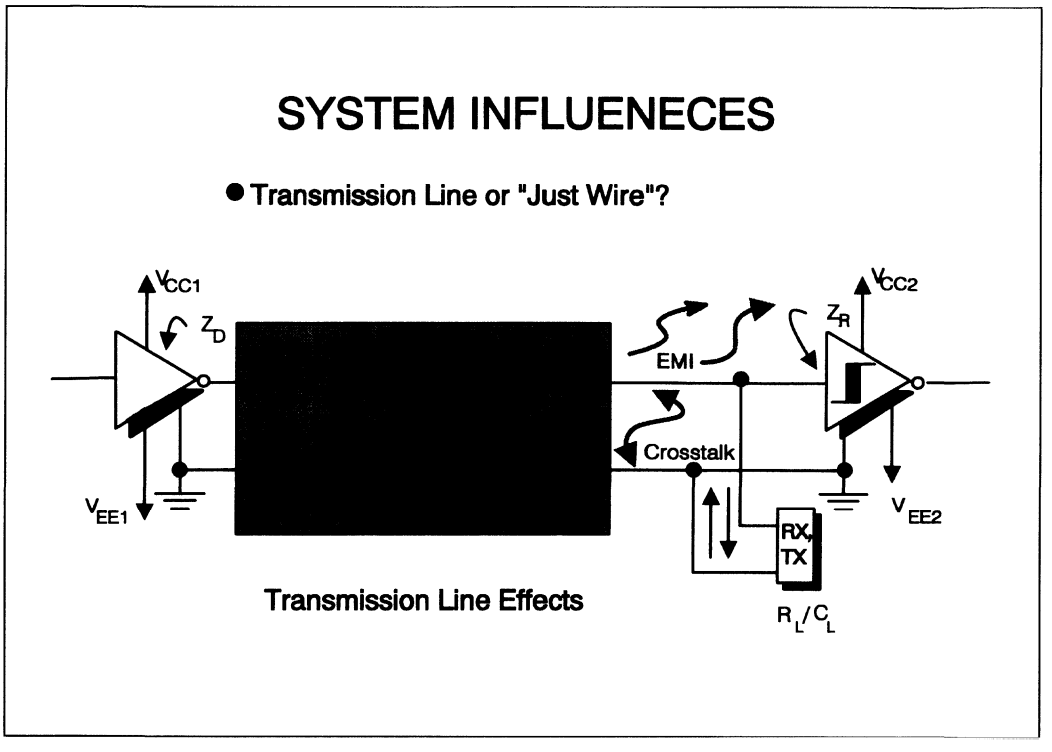


Figure 4.9 - System Influences

The behaviour of the signal and the integrity of the data depends upon the data rate and line length of the cable. There are two behavioural models;

i. **lumped parameter model (Short wire) .**

ii. **Distributed parameter model (Transmission line)**

A distributed parameter model models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections. As a result the transmission line is said to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wave front at any point as it travels along the line.

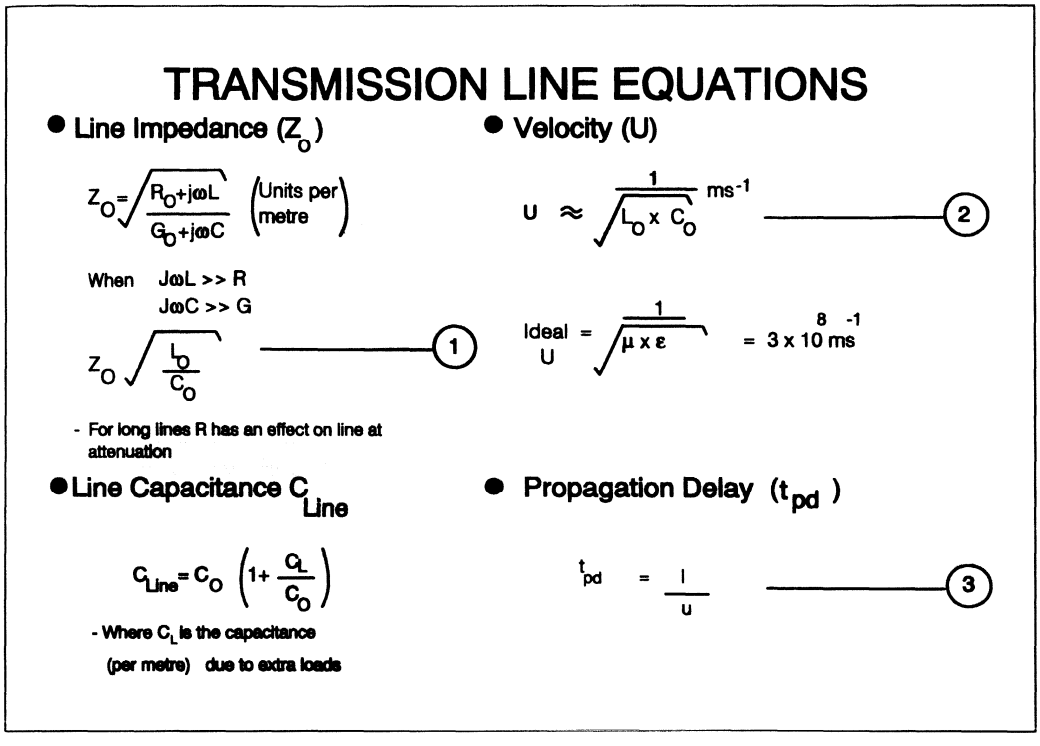


Figure 4.10 - Transmission Line Equations

2.2. Transmission Line Equations

The transmission line will always consist of two conductors. The current will flow in opposite directions in each of the conductors. In the single ended case one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light, 3.10^8 ms^{-1}. The limit to the speed will very much depend on the type of cable used.

2.3. Transmission Line Test

2.3.1. Classifying as a Lumped or Distributed Parameter Model

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings.

Consider a signal propagating down a simple data link comprising two wires. When the signal starts to change at the transmitter output the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system.

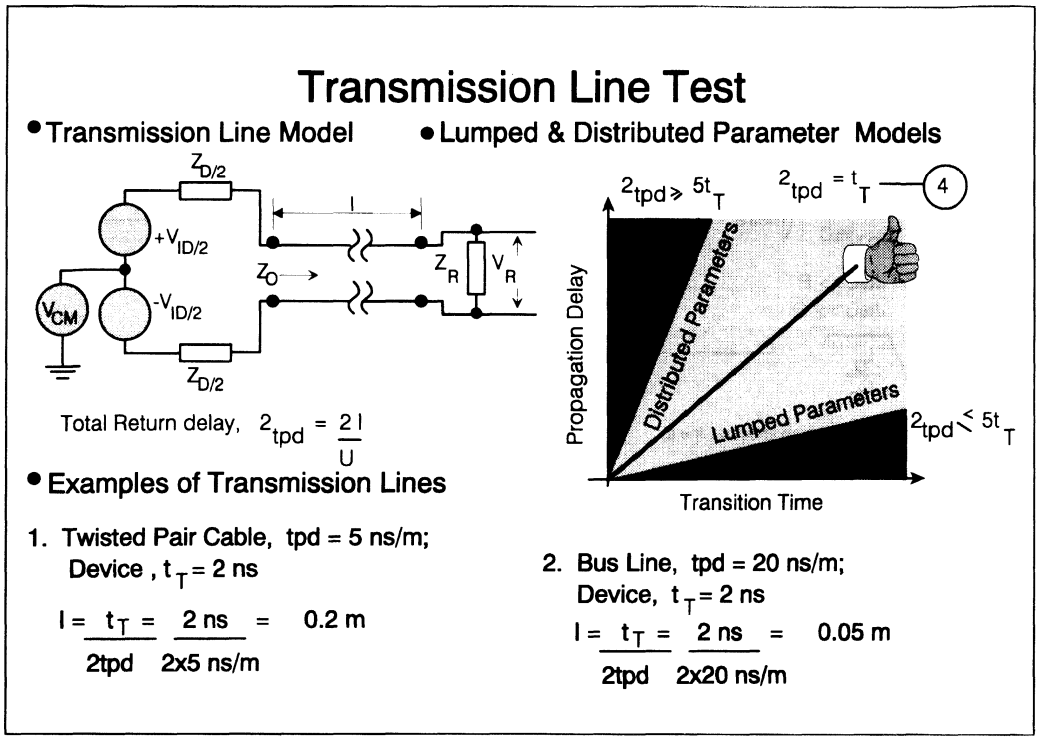


Figure 4.11 - Transmission Line Test

A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated;

If the rise time , t_T, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd}, to occur during the transition edge time, this is shown in figure 4.9.

2.4. Transmission Line Considerations & Effects

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added , providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. This extra load decreases the line impedance and reduces the speed of the signal along the line.

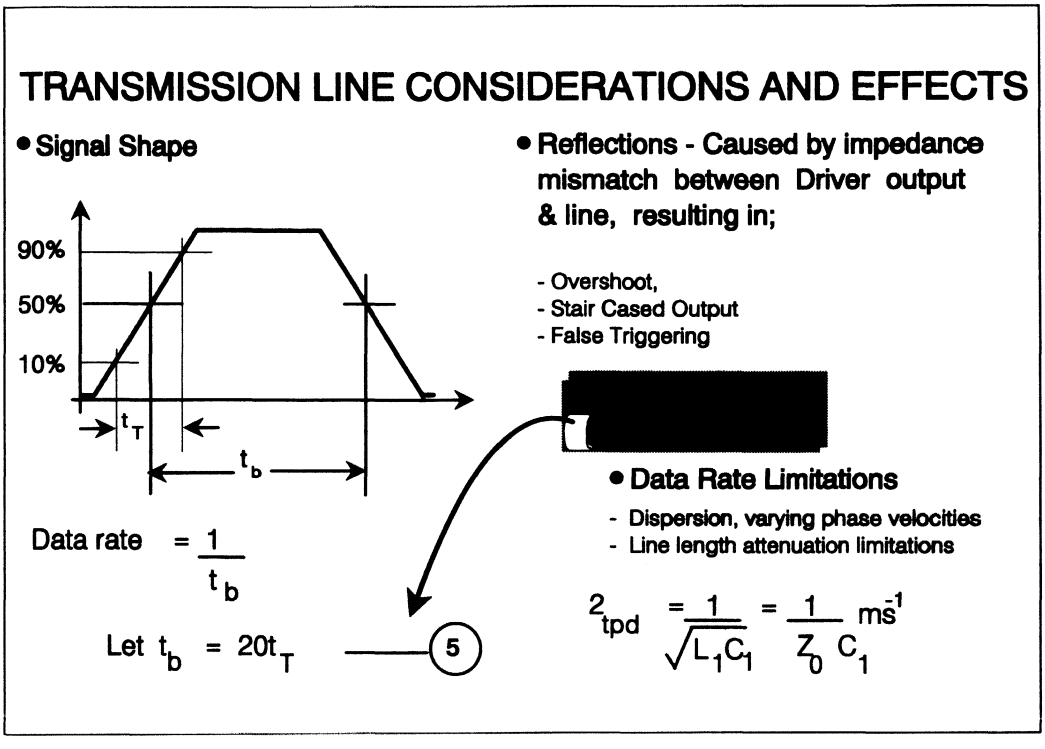


Figure 4.12 - Transmission Line Considerations

In the case of the lumped parameter model the line represents a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of the transmitter (assuming it can supply a finite amount of current to the line).

2.5. Transmission Line Reflections

Imagine a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This will cause the voltage at the output of the driver circuit to reduce as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

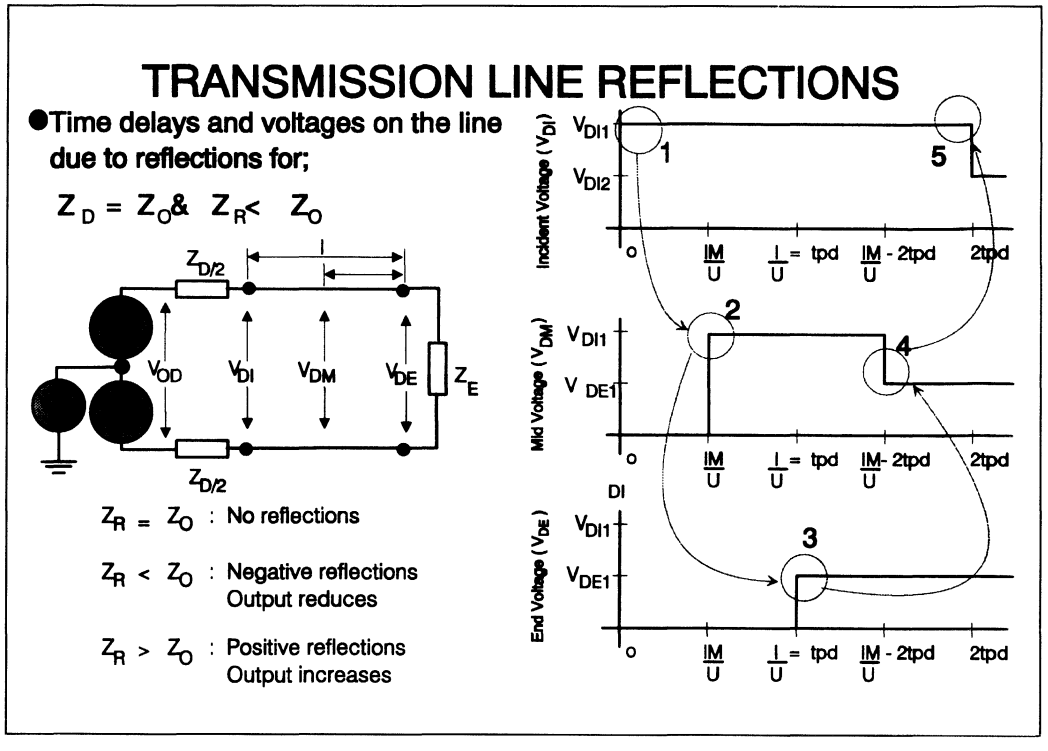


Figure 4.13 - Transmission Line Reflections

At at any point along the line the Ideal source impedance will appear as Z_O and the ideal load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source of twice the magnitude of the line voltage.

When the signal reaches the receiving end of the line it sees a terminating impedance equal to the impedance (Z_O) of the line that it is already travelling on. It interprets this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is dis-similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line..

Reflections at each end of the line will eventually settle and leave a constant dc. voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False receiver triggering can occur and repeated signal reflections will cause signal wave sdistortion.

2.6. Typical Reflections Due to Mismatching

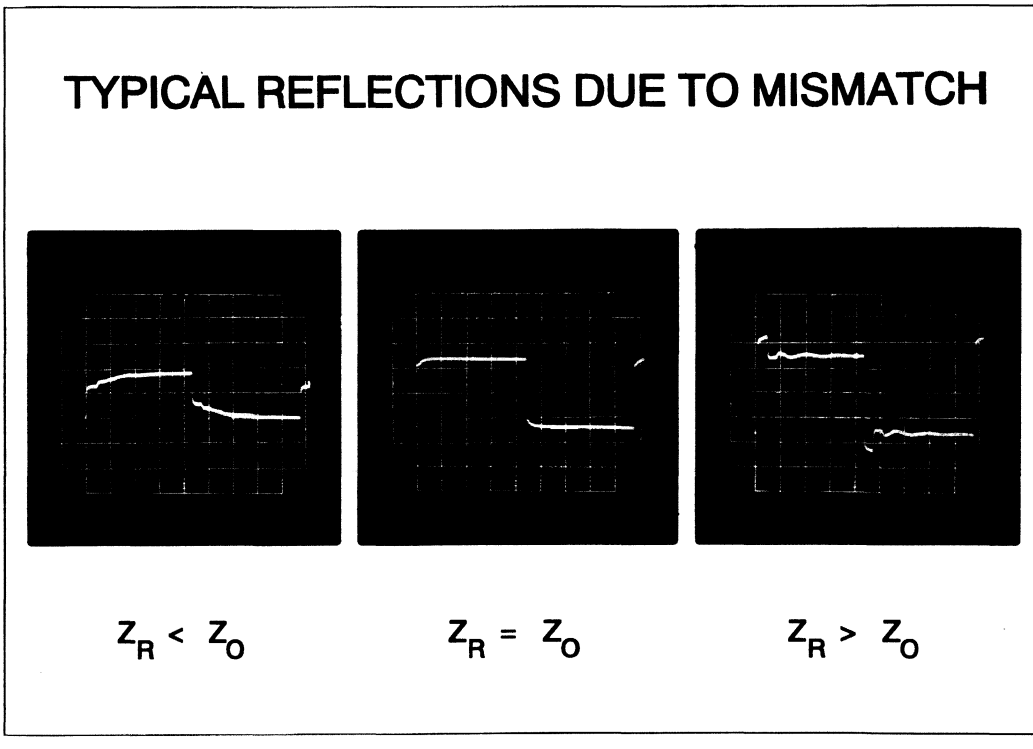


Figure 4.14 - Typical Reflections Due to Mismatching

The accompanying graphs prove the theory developed by comparing the signal quality between correctly terminated and incorrectly terminated lines. In all cases the top trace represents the output from the driver as presented to the line, while the bottom trace is the line input to the receiver.

For $Z_R < Z_O$ it can be clearly seen that the effect of the reflection voltage (top trace) is to reduce the incident step voltage. Similarly the reflection voltage has an effect for $Z_R > Z_O$, only this time the reflection voltage causes the termination voltage to be greater than the incident voltage. The ideal condition, $Z_R = Z_O$, produces a termination voltage relatively free from reflection voltages, and results in maximum power being delivered from the driver to receiver.

2.7. Transmission Schemes

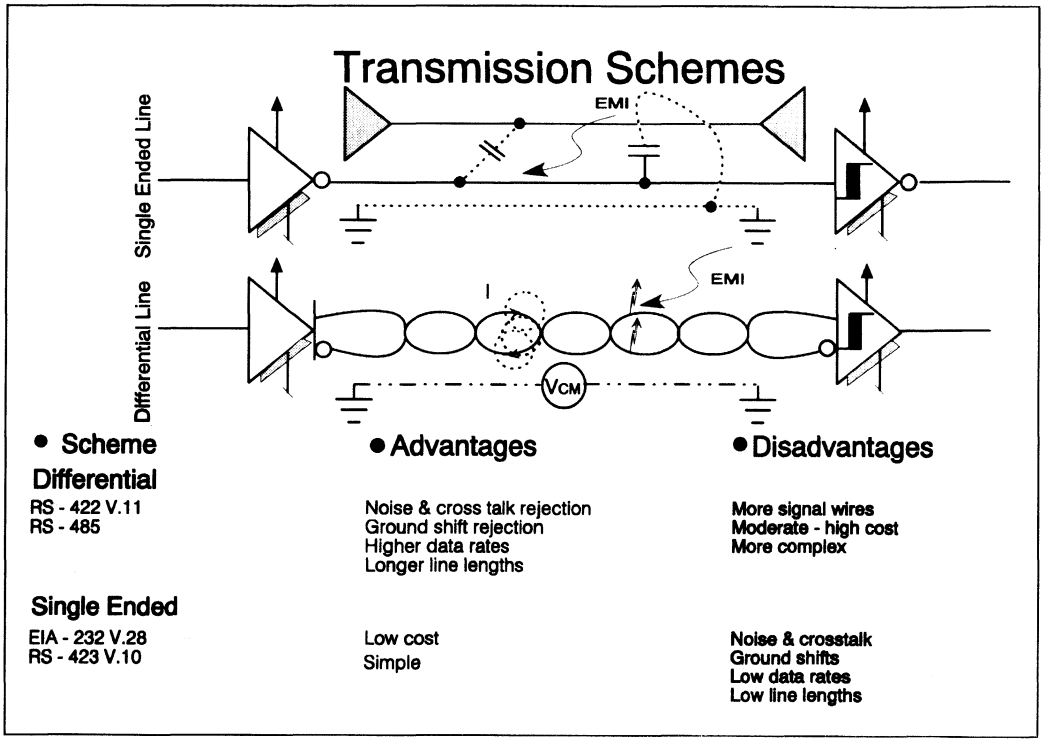


Figure 4.15 - Transmission Schemes

There are two main classification of transmission scheme, single ended or differential - these are described in the following text and depicted in figure 4.15.

2.7.1. Single Ended Line Considerations

Single ended data transmission systems consist of a signal line on which data is sent down, and a ground line through which the current returns. A direct result of this is that the ground line forms part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single ended system is the cheapest solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the

receiver device, thus increasing susceptibility to noise. Another common problem area with single ended systems is the effect of crosstalk between adjacent signal lines and the coupling into the line of noise from other sources. The line is both inductive and capacitive so will be susceptible to both electrostatic and magnetic coupling.

The crosstalk pick-up in the line is related to the effective coupling capacitance and the terminating impedance of the line. The higher the impedance of the termination circuit, the greater the induced voltage due to crosstalk. The induced voltage due to crosstalk also increases as the frequency or edge speed of the crosstalk signal increases.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

The induced noise can be reduced by;

- **Limiting the slew-rate of signals so that they do not cause crosstalk to be induced onto other lines**
- **Limiting the line length.**
- **Shielding the signal conductor.**

While the system noise could be reduced by:-

- **Isolating the signal ground from power conductors (e.g. keep signal grounds separated as far as possible from power grounds).**
- **Ground wires should be as low as impedance as possible.**
- **Use star ground system configurations.**

Some of these techniques are used in systems such as EIA--232 and the forthcoming Futurebus+ backplane system, which limit the slew-rate of signals by capacitive means (EIA-232) and by intentional generation of trapezoidal signals (Futurebus+).

2.7.2. Differential Line Considerations

A differential communication system involves the use of two signal carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the ***difference*** in voltage between the two wires. The absolute value of the dc common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

The use of a differential communications interface allows transmission of higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost but provides superior performance when data is transmitted at high rates over long distances.

2.8. Grounding Schemes

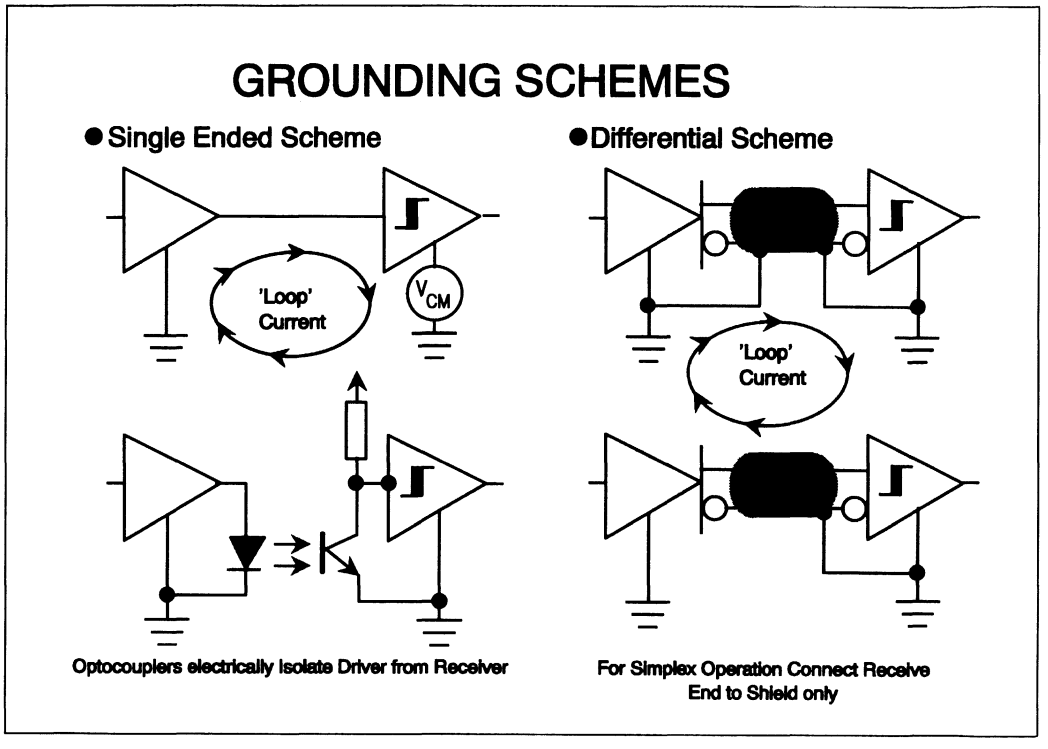


Figure 4.16 - Grounding Schemes

2.8.1. Grounding Should be Considered Early

Grounding should be considered early in the design phase of a party line system; there now follows a brief discussion of grounding considerations.

A 'ground' is an assumed arbitrary point of zero potential, and a ground connection is a tie to a point as close as possible to a ground potential. The objective of any grounding technique is to provide a path to earth of as low as resistance or impedance as possible. The reason for this is quite clear, the flow of current causes a voltage drop that is directly proportional to the resistance of the path to ground. Any resistance that results in unwanted difference of potential is the source of coupling to other circuits. The above may seem obvious but it emphasises the importance of principles like single point grounding in high performance linear circuits and the need to separate 'noisy' digital grounds from 'quiet' analogue grounds in a circuit. Of course the analogue and digital grounds will have to be combined at some point in the circuit, the terminals or at the zero volt bus bar for example.

2.8.2. Single Ended Grounding Schemes

For single ended data transmission it should be possible to transmit the data along a signal conductor to the receiver and then return the current to the zero volt potential. In ideal circumstances, the 0 V connection at the driver and receiver devices should be at the same potential. However, in long line applications, what happens in practice is that there is an apparent change in local ground or 0 V potential at one end of the system. This is represented in the figure by V_{CM} in series with the receiver ground. V_{CM} will cause the incoming signal to appear to have a reduced common mode voltage (assuming V_{CM} is positive). V_{CM} can reach values of several volts which could cause the link to fail. For example, if the receiver input switching threshold was set at 1 V and V_{CM} was 5 V, then the incoming signal would need to have an effective value of 6 V just reach the receiver's input switching threshold.

An obvious way to prevent the situation just described is to ensure that both receiver and driver have a common ground reference. This can easily be achieved by connecting a signal return/common ground reference. However, doing this can introduce another problem known as a 'ground loop' or 'earth loop'. This is formed because current is now free to flow as shown in the loop made up from the signal return wire and the earth path. Since V_{CM} is in this loop, current flows. If the loop encompasses many pieces of equipment, then the net results is that each equipment ground (or IC. ground) will have a different potential (something to be avoided).

In addition to the ground loop current that flows due to differing ground potentials, inductive coupling of signals external to the circuit into the ground loop is also another area of concern. The ground loop is prone to this effect since it forms a loop of large area and low impedance and is therefore highly inductive. In low frequency voice grade circuits, the interference is commonly found in the form of ac. hum picked up from nearby power supplies.

Therefore, single ended communication is not recommended for use in noisy environments due to interfacing coupling or for use over long distances if there is a possibility of ground shift.

A more complete solution to the problem of ground shift and interference involves the use of opto-couplers in order to electrically isolate the output of the driver from the receiver input. This is shown in general form in the figure. Since there is no electrical connection between driver and receiver, then no earth loop is formed. Modern opto-couplers also have extremely good rejection capability to high frequency common mode signals; as high as 10 kV/ms and can operate at up to 10 Mbps (HCPL2601 from TI).

2.8.3. Differential Grounding Schemes

Figure 4.16 illustrates a very simple guide-line for dealing with shield grounding in differential systems. If the shield is grounded at both driver and receiver ends, then a possible ground loop path exists which can lead to the problems already described.

The answer is to ground the shield only at the receiver end. This ensures that a ground loop current cannot flow. The shield therefore acts as a low impedance path to ground for externally interfering signals.

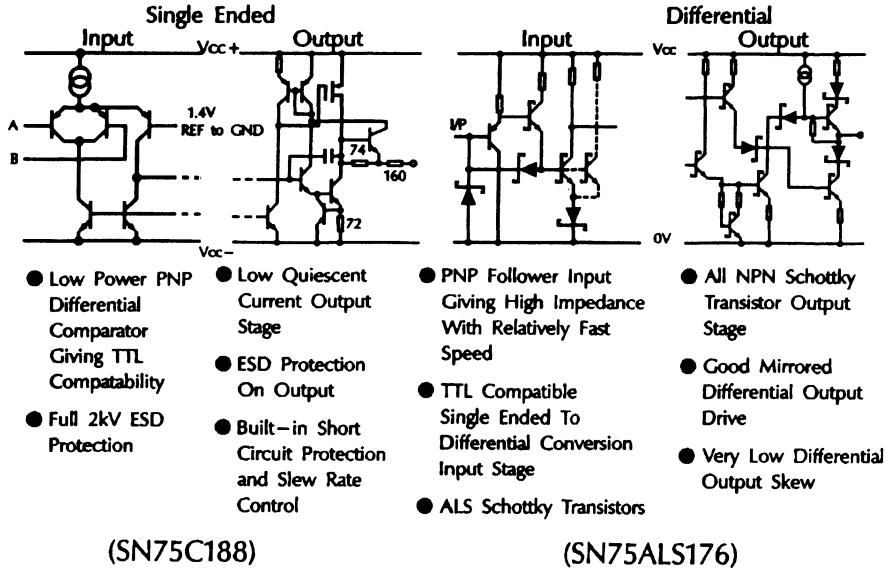


Figure 4.17 - Driver Configurations

2.9. Driver Configurations

The two basic formats for data transmission systems; single ended and differential, have differing current and voltage requirements. As a consequence there are differences in the internal structures of the integrated circuits used to drive lines in each of the two formats. The largest difference lies in the design of the output stage.

Consideration of the input stage in most line driver circuits will show them to be TTL compatible. The SN75C188 quad EIA-232 driver and SN75ALS176 RS-485 transceiver shown in figure4.19 demonstrate this. The inputs of both devices feature a reversed bias diode and resistor to the positive supply and an effective two forward diode drops to ground. This is a similar configuration to that found in a standard TTL gate and results in the 0.8V and 2.0V TTL threshold levels. However, the SN75C188 has been designed for dual rail applications and so shifts the 0-5 V input voltage to the +/- 12V output voltage range. Since it is designed to drive differential lines, the SN75ALS176 includes a single to differential converter stage consisting of a latch with an extra invertor structure.

Single ended line drivers are normally used to transmit data at lower speeds and require less output current drive capability. They are therefore good candidates for implementing in a lower power process technology. A new generation of EIA-232 devices built using a BiMOS process has emerged to make low power consumption a reality. The new Generation of low power BiMOS devices includes quad drivers and receivers (SN75C188/198/189), both triple and quad combined

driver/receivers (SN75C1406/1154) and a mixed three channel driver and five channel receiver (SN75C185).

The new BiMOS technology devices offer more advantages than just reduction in power consumption; slew rate limitation of the EIA-232 signal to 30 V/μs is carried out on-chip. This eliminates the need for external capacitors.

High speed differential output drivers, the SN75ALS176 for example, use an all schottky NPN totem-pole output stage. This increases the output switching speed performance over technologies using PNP transistors in critical signal paths. The advanced low power schottky technology (ALS) also substantially reduces supply current consumption over standard LS NPN structured devices (SN75176).

As data rates demanded from systems increase, switching speeds in differential driver outputs also increase. However, since the outputs are complementary in nature it is essential that the two outputs change state at the same time. Total simultaneous switching when driving a long cable is almost impossible to achieve, but the excellent signal skew specifications for 'ALS devices almost eliminates this problem making them suitable for even the most demanding of applications.

2.10. Receiver Configurations

The design of a line receiver circuit is also dependent upon the type of data transmission system it is ended to work in. The key operational parameters to be specified include:

- **Differential or single ended inputs.**
- **Input signal switching threshold.**
- **Input signal common mode range.**
- **Speed/power requirements.**

The design of a single ended receiver is usually simpler than that of its differential counterpart. The single input stage to a single ended receiver is similar in function to a voltage compactor circuit. The input signal is compared to an internal reference and the output is switched accordingly.

New generation EIA-232 receivers, constructed using BiMOS technology, have been designed to meet new systems' power saving requirements. They also include line noise rejection filter circuits in their design, providing further system integration. The filters incorporated into the receiver are capable of rejecting voltage noise and glitches on the line which are less than 1 μs duration. This feature saves on board space and reduces external component cost. The output stage of the SN75C189 receiver circuit has been designed using a low power common emitter circuit.

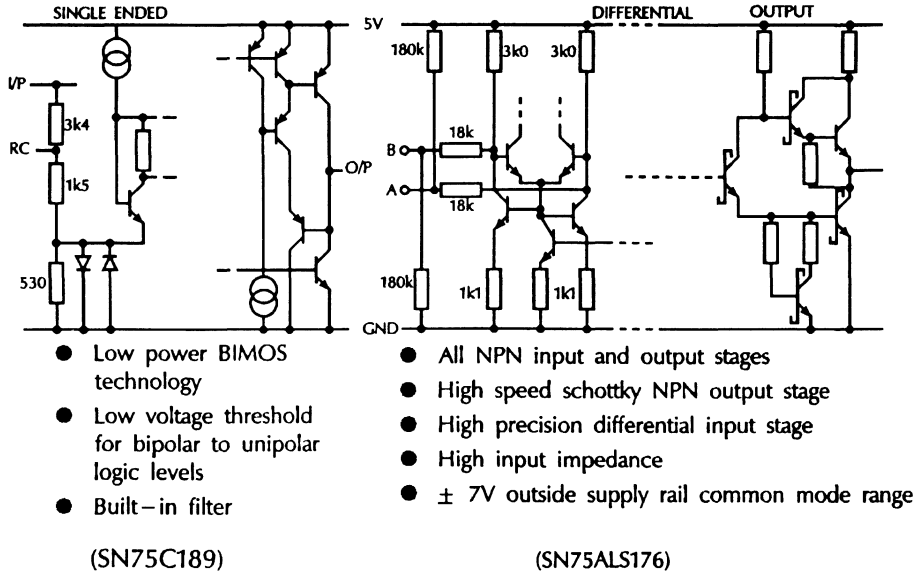


Figure 4.18 - Receiver Configurations

Differential receiver circuits have to operate in the presence of large common mode dc. voltages at the input terminals, while still maintaining a good differential accuracy. This is achieved by making the heart of the receiver a high speed differential amplifier. The common mode range of this amplifier is small, so as to maintain its gain accuracy and speed. However, in order to cope with the large common mode input voltages, from -7 V to +12 V, the input circuitry incorporates a potential divider network that reduces the effective common mode input voltage while still maintaining a high input impedance. The network clamps the common mode part of the signal to a constant level suitable to the differential amplifier stage. The same resistive network also provides the large minimum input impedance required to meet RS-485 requirements.

The output stage of these receivers uses an ALS NPN transistor network that provides the high speeds demanded by the RS-485 system, while maintaining a good power consumption

3. Interface Circuits For EIA-232

3.1. General Information

This section provides an overview of the EIA-232 standard, its application and products overview for the Texas Instruments range of EIA-232 products.

The Texas Instruments range of EIA-232 data transmission products not only consists of low-power EIA-232 interface circuits, but also high performance asynchronous communication controllers. The EIA-232 interface circuits, mostly designed using a low-power bipolar process (BiMOS), offer higher levels of integration, optimisation and robustness than previously available.

The broad range of asynchronous controllers include options for both single-and dual-asynchronous control and include parallel port control. Higher performance applications are served by the inclusion of dedicated DMA (direct-memory-access) handshaking control and input/output FIFOs.

3.1.1. Reliability Data

System designers have long been aware that the mean-time-between-failure (MTBF) for most systems is limited by the reliability of the line interface circuitry. This is mainly due to over thermal dissipation in the interface circuits (using devices with high quiescent power consumption) and to external influences such as line short circuits and ESD damage. The use of bipolar structures on critical input/output pins is therefore a necessity, particularly if the CMOS 'latch-up' phenomenon is to be avoided. Clever bipolar design techniques have resulted in a family of devices that are not only robust but have exceptionally low-power consumption, typically 99% less than the older industry standard designs

Recent life test data collected on the range of EIA-232 devices yielded a failure rate of 1.65 FITS (failures per 10^9 device hours). This was at an ambient temperature of $55^{\circ}C$ (to an upper confidence level of 60% and assumes an activation energy of 0.96 eV).

3.2. EIA-232-D Industry Standard for Data Transmission

The Electronic Industries Association (EIA) introduced the EIA-232 standard in 1962 in an attempt to standardise the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). Although emphasis was then placed on interfacing between a modem unit and data terminal equipment, other applications were quick to adopt the EIA-232 standard. The growing use of the PC (personal computer) quickly ensured that EIA-232 became the industry standard for all

low-cost serial interfaces between the DTE and peripheral. The mouse, plotter, printer, scanner, digitizer, and tracker-ball, in addition to the external modem unit, are all examples

of peripherals that connect to an EIA-232 port. Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

The EIA RS-232-C standard, revised in 1969, has now been superseded by EIA-232-D (1986), which brings it in-line with CCITT V24, V.28 and ISO IS2110. The latest revision includes a mechanical specification for the interface connector and loopback and test modes as the major changes. Although an older standard, with problems like high-noise susceptibility, low data rates and very limited transmission length, the EIA-232 fulfils a vital need as a low cost communication system. Consequently new products are being developed at a faster rate than ever.

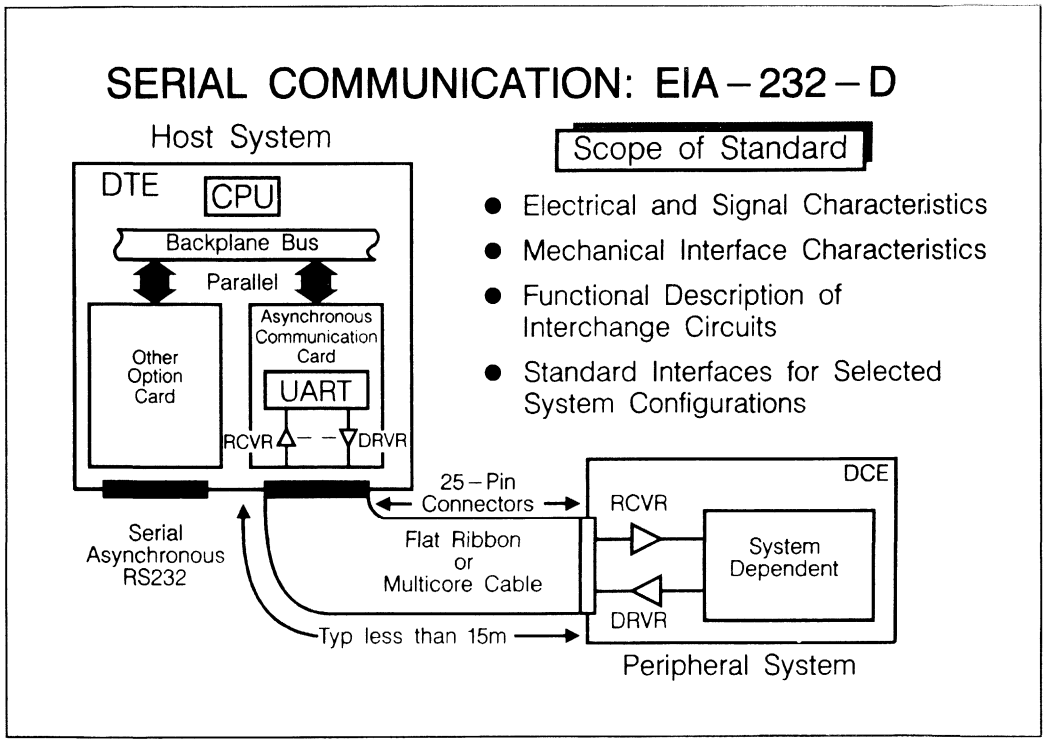


Figure 4.19 - EIA-232-D Industry Standard for Data Transmission

3.3. EIA-232D Electrical Specification

3.3.1. Scope of Standard

Electrical and Signal Characteristics

Electrical and signal characteristics of the signals and associated circuitry in terms of signal voltage levels, impedance's, and rates of change.

Mechanical Interface Characteristics

Mechanical interface characteristics defined as a 25-way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25-pin D-type connector, most laptop PCs , today use a 9-pin "DB9S" connector.

Handshake Information

A functional description of the interchange circuit enables a fully interlocked handshake exchange of data between equipment's at opposite ends of the communication channel. However, V24 defines many more signal functions than EIA-232, but those that are common are compatible. twenty two of the twenty five connector pins have designated functions, although few, if any, practical implementations use all of them. The most commonly used signals are shown in the following table;

Designation		DB25S Pin	Common Usage
Signal Ground	SG	Pin-7	Interface ground reference.
Signal Out	SOUT	Pin-2	From the DTE to the DCE.
Signal In	SIN	Pin-3	From the DCE to the DTE
Request To Send	RTS.	Pin-4	DTE informing the DCE it wants to transmit. Also used to control direction of communication in half-duplex system.
Clear To Send	CTS	Pin-5	DCE informs the DTE that the DTE may transmit. This is usually in response to a RTS and its own ready condition.
DCE Ready	DSR	Pin-6	The DCE informing the DTE that it is connected to a communications channel and all dialling, talking, testing etc. is over. (Also called Data Set Ready.)
DTE Ready	DTR	Pin-20	The DTE informing the DCE that it is ready to transmit or receive data.
Received Line Signal Detector	DCD	(Pin-8)	The DCE informing the DTE that it is receiving valid signals over the channel. Sometimes called Carrier Detect.

Ring Indicator	RI	(Pin-22)	The DCE informing the DTE that a ringing signal is being received on the communication channel. (Used in auto-answer systems.)

A common reason why "standard" EIA-232 devices fail to communicate with each other is that one device implements only some of handshake signals, but the other is expecting all of them.

Standard Interface Connections for Selected Equipment Configurations

The standard also contains information on selected system configurations, outlining the use of interchange signals for different applications.

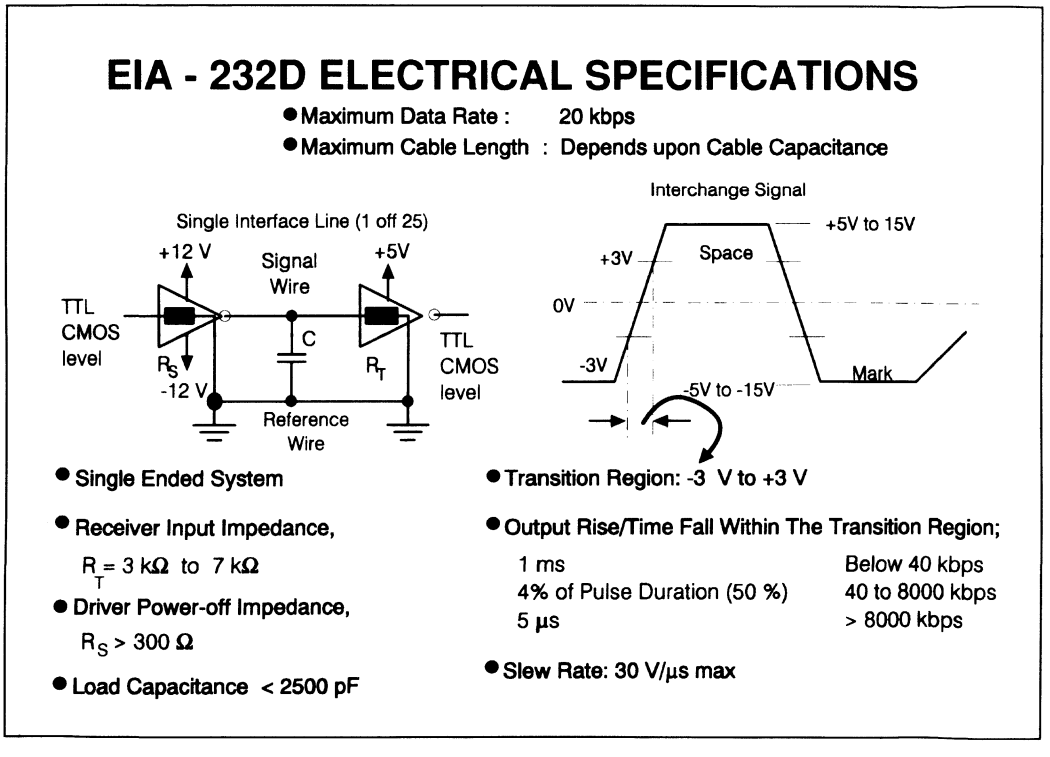


Figure 4.20 - EA-232-D Electrical Specifications

Data transmission using EIA-232 is relatively slow. The EIA-232 standard specifies a nominal upper limit for the data signalling rate of 20,000 bits per second (20 kbps). Transmission line effects, such as reflections at such data rates and short line lengths can be ignored; hence, load resistance and capacitance can be regarded as lumped parameters.

Although some applications use data rates well beyond the recommended maximum of 20 kbps, but faster transmission standards such as RS-423, RS-422 and RS-485 are recommended.

The cable length as specified in RS-232C is to a maximum 15 metres. A limit on the cable length is not specified in the 'D' revision, but rather a maximum load capacitance of 2500 pF. As the typical cable capacitance is in the order of 150 pF/m, then the maximum cable length is generally around 15 m. The combination of the driver's output current capability, the load capacitance (cable length), and the standard's switching requirements should be considered in every design. This is particularly true when conforming to the more stringent CCITT V.28 specification.

A driver converting a TTL/CMOS signal to EIA-232 levels is usually supplied from ±12 V. A receiver converting EIA-232 levels to TTL/CMOS levels requires only a single 5 V supply. The receiver input impedance, specified to be in the range from 3 k to 7 kΩ, combined with the signal levels dissipate considerable power – even if no transmission takes place.

A receiver treats a signal above 3 V as a logic zero, a "space" or an "ON" condition. A signal below -3 V is treated by the receiver as logic one, a "mark" or an "OFF" condition. The band between -3 V and 3 V is the transition region. The generator or driver must provide a minimum of +5 V and a maximum of -5 V at the interface point (any point between driver and receiver).

3.4. Transition Time Limitations vs Data Rate

EIA-232 is a single–ended transmission system, and as such makes the transmission line susceptible to induced noise and common-mode signals. Additionally, single ended systems can radiate Electro Magnetic Interference (EMI) and switching noise (crosstalk) into adjacent systems. The latter effect, crosstalk, can be minimised by limiting the period of time the signal can stay within the transition region. This time is dependent upon the data rate and reduces susceptibility to noise during transitions as well providing a defined signal for asynchronous applications. A maximum $\delta V/d\tau$ of 30 V/µs minimises cable crosstalk, high frequency switching emission, and interference with other signals

Figure 4.21 shows the time required for data and timing signals to pass through the -3 V to 3 V transition region versus data rate for the standards: EIA RS-232-C, EIA-232-D and CCITT V.28. The 30 V/us maximum slew rate and the upper data rate of 20 kbps limit are also added, restricting the signal transition to a well–defined area. The transition time for control signals should not exceed 1 ms.

Note that the requirements of the CCITT specification V.28 are stricter than either revisions of "232". V.28 states that "the time required for a signal to pass through the transition region during a change should not exceed 1 ms or 3% of the nominal element period on the interchange circuit, whichever is less". RS-232-C allows the transition time to be 4% of the duration of a signal element. EIA-232-D represents a relaxation at data rates above 8 kbps where the maximum transition time becomes flat at 5 µs. This means that all devices meeting V.28 and RS-232-C will also meet EIA-232-D. The practical implications of these timing limitations relate the driver's maximum output current and to the maximum cable length for a given data rate.

A basic equation can be derived to calculate the necessary driver output current for a given data rate;

$$I = C\delta\frac{V}{t}$$

δt = 3% or 4% of nominal element period depending upon standard

δV = Transition region (-3 V to 3 V = 6 V)

Where:

C = Cable capacitance

I = Current limit (min)

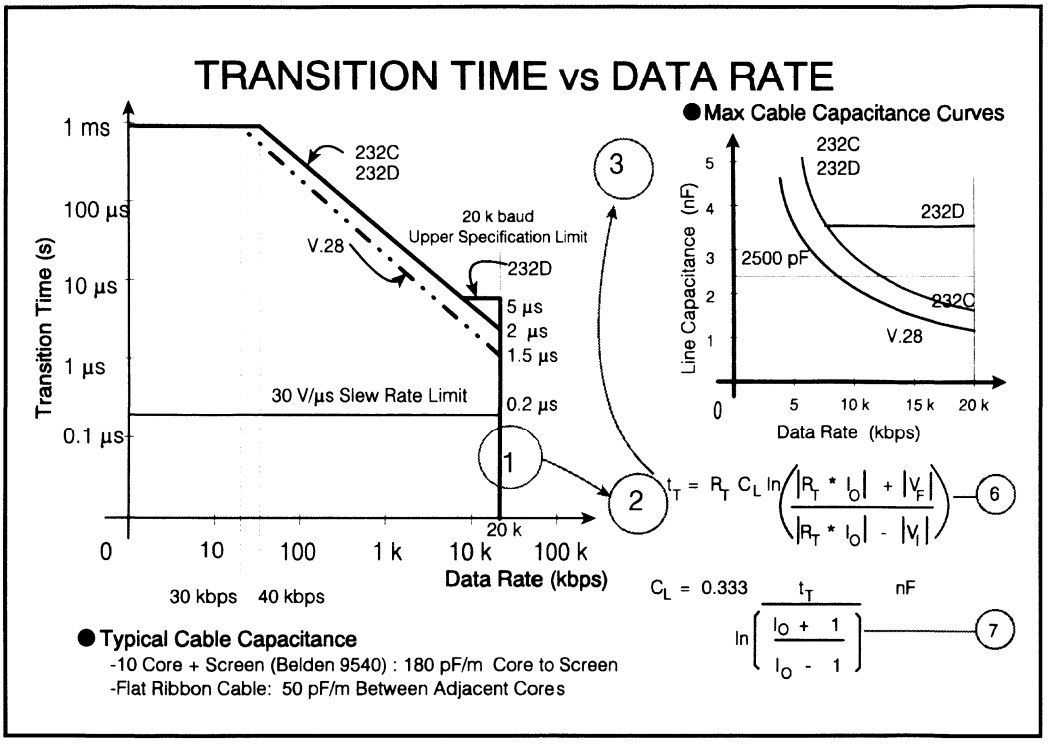


Figure 4.21 - Transition Time Limitations vs Data Rate

3.5. Designers Key Technical Care Abouts

The principle requirement of any device designed for operation in an EIA-232 application is in its conformance to the standard's specification. Seemingly this would leave little room for product differentiation. However, by taking into consideration the key points listed in the accompanying figure it is apparent that semiconductor manufacturers can differentiate their products, thus allowing original equipment manufacturers to differentiate theirs.

The ever increasing use of laptop and portable, battery–backed equipment employing the EIA-232 interface, demands lower-power devices than previously available. Also the increasing integration of modems, PCs and peripherals coupled with the necessary reduction in board space requires the elimination of external passive components. Ultimately expensive power supply components used to generate the necessary ± voltage supplies can be discarded in favour of drivers and receivers (available

on the same I.C) containing charge pump circuitry. Although not required in computers containing disk drives, since ± supplies are already available, this feature is required for many hand–held test and medical equipment.

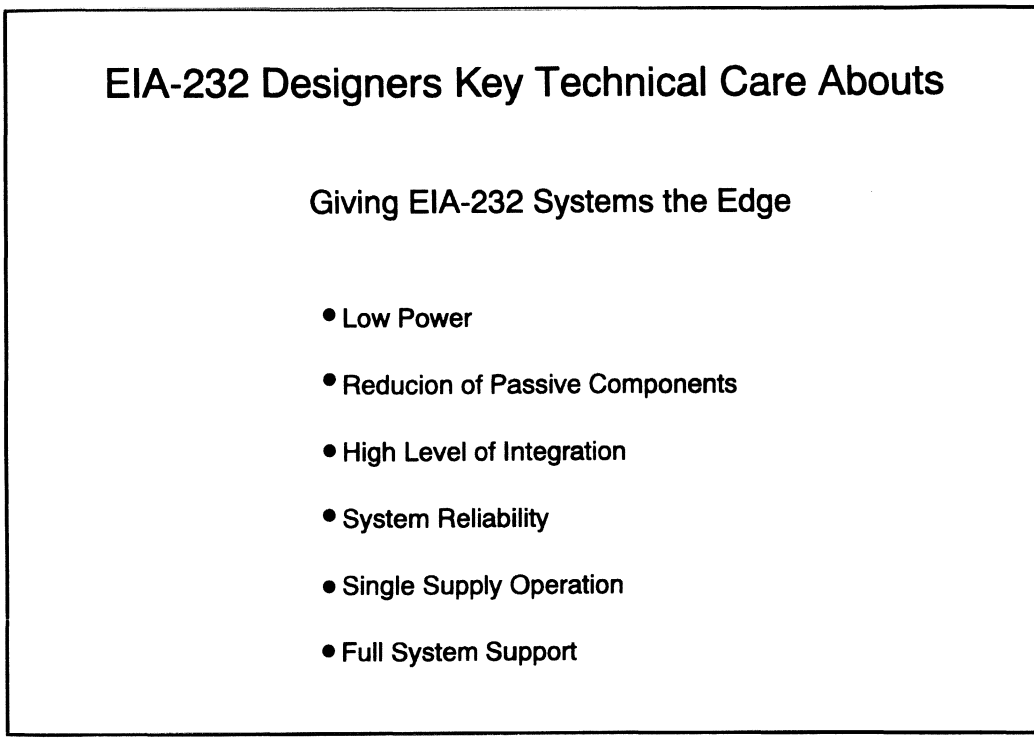


Figure 4.22 - Designers Key Technical Care Abouts

In systems like host terminal controllers or server systems where multiple EIA-232 lines are used, system downtime is expensive and difficult to diagnose. Therefore added reliability and robustness must be built into these system, furthermore, employing self–test capabilities will greatly simplify fault–finding diagnoses.

Most EIA-232 systems use asynchronous data transfer that requires a communications controller for the parallel-to-serial data conversion (and visa versa) to control the flow of data, to add/delete the start/stop bits and for error checking. Although the microprocessor can be used for this purpose, dedicated controllers are generally preferred to off load the mundane interface activity from the processor.

3.6. Introducing the Low-Power BiMOS Family

TI has been a leading supplier of EIA-232 products for many years. Bipolar devices such as the quad–driver SN75188 and quad–receiver SN75189 have become synonymous with EIA-232 designs.

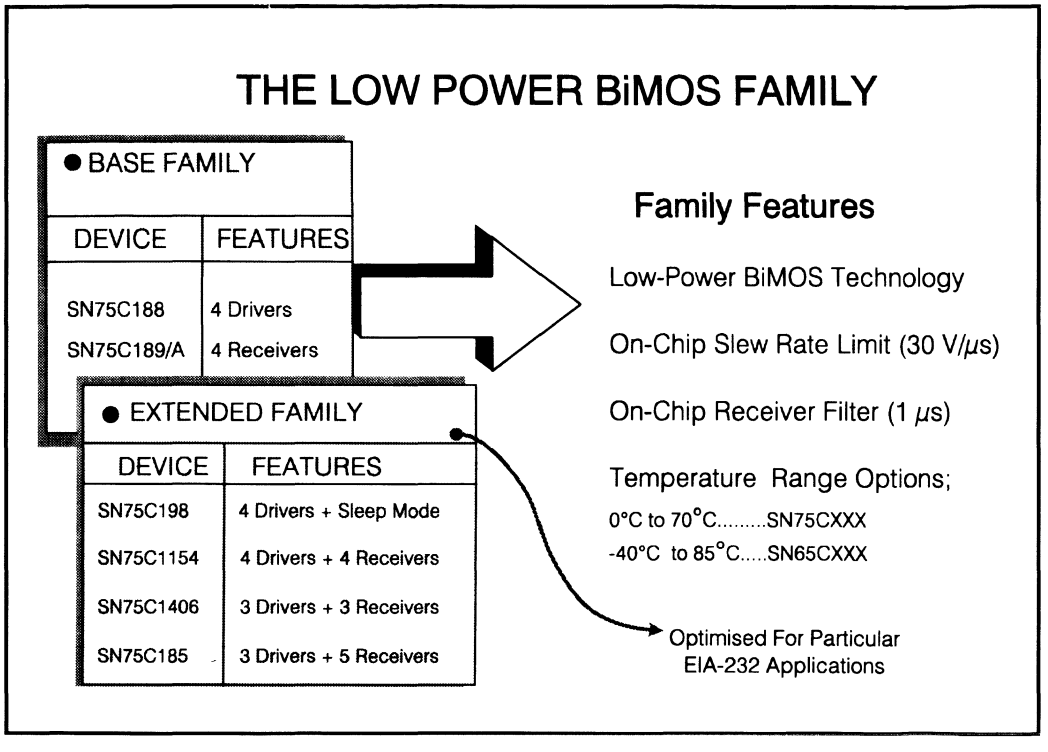


Figure 4.23 - Introducing the Low-Power BiMOS Family

Although these products (see Interface Circuits data book for complete range) continue to enjoy popularity and are still being selected for today's designs, the emergence of battery–backed and portable equipment's has led to a need for devices yielding much lower power consumption than the old bipolar technology can give.

As a consequence TI looked towards one of its many new technologies – BiMOS.

BiMOS is a low-cost, low-power process capitalising upon the benefits from both bipolar and the low-power consumption of PMOS structures. Using this process in EIA-232, designs can yield as much as a 99% saving in power consumption.

The new generation of BiMOS devices are shown in figure 3.2, along with the key family features. In essence, all devices have been designed with the power and space restrictions imposed on modern

equipment in mind, namely each device in the family, in addition to having low power, contains the necessary capacitive components for receiver filter implementation and driver slew-rate limit. The extended family of devices are optimised for particular usage of EIA-232 handshake lines; for example, the SN75C185 is optimised for IBM™ compatible serial ports.

All devices are offered in either surface mount packaging (SO) or in the plastic dual-in-line package (DIP). Temperature ranges available are; Commercial – , 0°C to 70°C, or industrial –, -40°C to 85°C. These devices are selected by SN75Cxxx or SN65Cxxx respectively.

3.6.1. Low Power BiMOS

Many devices used today, like the MC1488/SN75188 and MC1489/SN75189, are fairly old designs consuming a lot of power. New developments like the SN75C188 and SN75C189 have yielded low-power devices offering insignificant quiescent power consumption when compared with the line current. (Line current flows from the driver output through the receiver input impedance, typically 5 kΩ, to ground). This current flows even when no data is transmitted.

One way to reduce this line current in data off periods is to employ a driver with a 3-state output feature like the SN75C198. By disabling the output, the power consumption can be reduced to only 1% of the old SN75188/SN75189 system.

Most industry standard devices require capacitor bypassing to ground, on all the lines, to ensure the maximum slew-rate limit of 30 V/µs specified by the standard. The capacitor value, C_S, can roughly be estimated from the maximum driver output current and the cable capacitance. The cable length and capacitance is usually not a fixed parameter, however with a maximum output current of 12 mA from the SN75188 a 400 pF capacitor for C_S will ensure operation within the standard even without a loading cable.

When communicating between the elements of a data processing system in a hostile environment, spurious data, caused by ground shifts and noise, may be introduced. Therefore, it can become difficult to distinguish between a valid data signal and those introduced by the environment. To overcome this problem in systems using older devices, a RC receiver filter is formed by a part of the receiver's resistive input impedance and an external capacitor, C_F, giving a single pole roll-off. This adds up to a total of eight capacitors required per quad driver and receiver pair for proper operation.

The SN75C188, SN75C198, SN75C189 and SN75C189A designs feature built-in slew-rate limitation that meets the standard under all load conditions. Furthermore, a unique built-in receive filter rejects all signals below 1 µs of duration, regardless of voltage amplitude and accepts all signals longer than 4 µs as valid data.

The new designs eliminate eight external passives per driver/receiver pair.

3.7. Real Low Power EIA-232

EIA-232 devices with an on-chip charge-pump generate dual supplies for the EIA-232 driver function from a 5 V logic supply voltage. Because of this, they are gaining increasing popularity.

However, for power-conscious applications such as laptop/notebook PCs, their peripherals, and for battery-driven industrial equipment, the SN75C198 and SN75C189 combination significantly reduces the power supply demands.

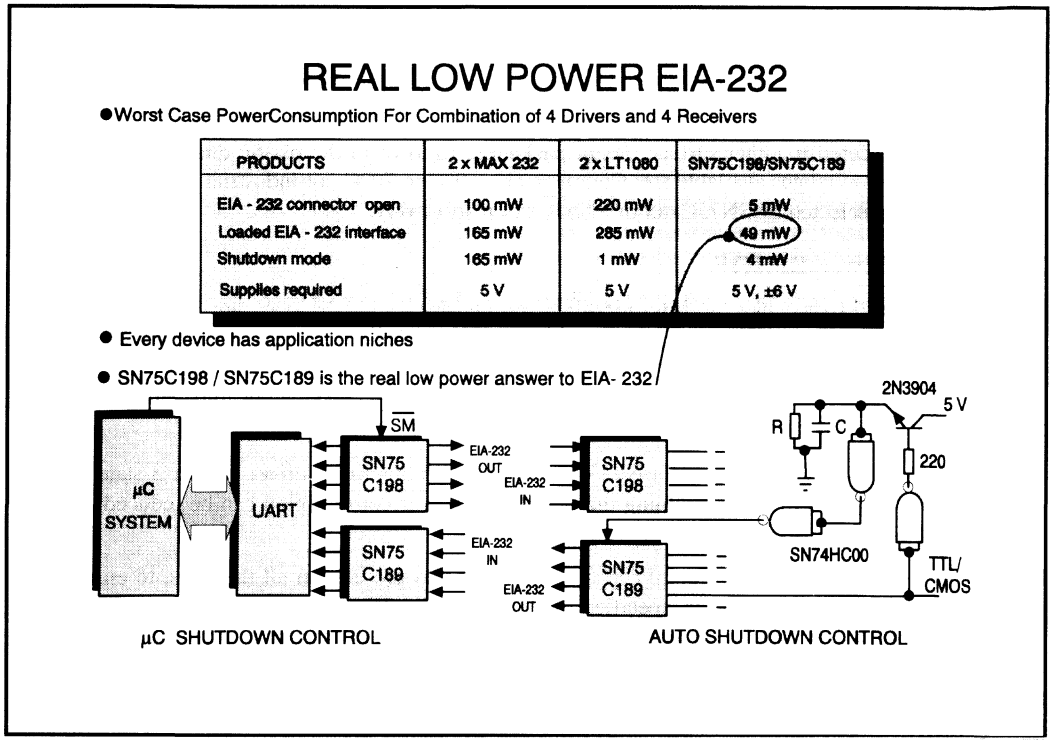


Figure 4.24 - Real Low Power EIA-232

Even when taking into account the low efficiency of dual-voltage supply generation, these devices are clearly the best solution.

3.7.1. Comparison of Alternatives

The worst-case power consumption for different driver/receiver combinations forming four EIA-232 driver lines and four EIA-232 receiver lines are given in the table on the following page. All devices are available from Texas Instruments. Minimum supplies required to meet EIA-232-D requirements are used.

Function/Parameter	4 Driver and 4 Receiver Functions with 3-State Output or Shutdown Mode			4 Driver and 4 Receiver Functions		
	SN75C198 SN75C189	2x LT1080	LT1030 SN75C189	2x MAX232	2x LT1081	SN75C188 SN75C189
Charge-Pump	No	Yes	No	Yes	Yes	No
Supplies Required	±6 V(min) 5 V	5 V	± 7V(min) 5 V	5 V	5 V	± 6V 5 V

Max. Icc No Load	160 µA (±6 V) 700 µA (+5 V)	44 mA	1 mA (±7 V) 700 µA (5 V)	20 mA	44 mA	160 µA (± 6V) 700 µA (5 V)
Max. Icc Shutdown	40 µA (± 6V) 700 µA (5 V)	200 µA	150 µA (± 7V) 700 µA (5 V)			
Total Active Power Consumption. No Load +	5.4 mW	220 mW	17.5 mW	100 mW	220 mW	5.4 mW
Total Active Power Consumption. 3 kΩ Driver Loads	49 mW	285 mW	78 mW	165 mW	285 mW	49 mW
Shutdown Power Consumption.	4 mW	1 mW	5.6 mW			

+No Load condition refers to the situation where no EIA-232 cable and receiver is attached.

For continuous data transmission or under no load conditions, the combination of SN75C198/SN75C189 or SN75C188/SN75C189 has the lowest power consumption. However, if a EIA-232 link is established that has periods where no data is being transmitted, the required average power consumption can be further reduced by taking advantage of the SN75C198's 3-state output (or sleep-mode function). This avoids wasting power dissipated into other, receivers' input impedance's. The SN75C198/SN75C189 combination is the most attractive solution for real low power systems with data off periods of less than 99% of the total time. If data is submitted less frequently than 1% of the total time, the LT1080 solution becomes more favourable, but a higher peak power demand is required from the power supply when transmitting.

Although requiring three supply voltages, ±12 V and 5 V, the SN75C198/SN75C189 solution can easily beat the power consumption of 5 V charge-pump systems, even when the efficiency of generating the additional ±12 V is taken into consideration. If an additional centre tap winding is added to the existing +5 V switch mode power supply's transformer, simple rectification with Schottky diodes and ripple smoothing is usually enough to provide the ±12V supplies, as no strict stabilisation requirements exist. If needed, low drop-out regulators can provide further stabilisation without too much power loss.

3.7.2. Shutdown Control Methods

Microcomputer controlled shutdown is simple to implement under no-data conditions by bringing the SN75C198 quad driver in to sleep-mode (pseudo 3-state output) condition. Using sleep-mode in this manner can also be used to prevent 'garbage' from being transmitted during device power-up.

Power savings can also be obtained in existing systems or where no extra µP port is available for control purposes by an auto shutdown control. This is implemented by simply adding a low-power SN74HC00 logic gate, a transistor, and an RC time constant to form a simple mono-stable multivibrator. The SN75C198 is enabled as long as its sleep mode pin is kept high by sensing a low TTL/CMOS level on an EIA-232 data or handshaking transmit line. Enable time is prolonged by the time it takes to discharge C through R to the CMOS gate's threshold level.

An alternative automatic scheme can be implemented by using a TLC555 timer configured for edge-triggered mono-stable operation. If the TLC555 trigger input is ac coupled to the TTL/CMOS input of

the EIA-232 driver being first activated during a transmission, the timer enables the SN75C198. The TLC555 keeps the EIA-232 driver active for a time equal to 1.1 * RC, where R and C are the timers' external resistor and capacitor in its mono-stable configuration.

3.8. Noise Filtering for EIA-232-D Interface

The standard states a maximum line cable capacitance of 2500 pF, which corresponds to an approximate line length of 15 m. As the interface line gets longer, it becomes more susceptible to noise pick-up from the surrounding environment. This pick-up is due in part to the inductive nature of the line. As the signal switches, a rapidly changing magnetic field induces noise currents into the line, thereby corrupting signal data. The level and cause of this noise will dictate the nature of solutions or precautions that should be taken.

For operation at high data rates, the use of a differential line might be the best solution. If however, a low cost and simple single-ended solution is required then standard EIA-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input stage, making them too slow to respond to fast switching noise pulses. Even small levels of input noise can falsely trigger the receiver. The maximum data rate specified in the standard is 20 kbps, corresponding to a minimum pulse period of 100 µs. Therefore in normal applications, most devices are far faster than the specification requires.

To slow down older bipolar receivers such as SN75189s, a capacitor, C_C, needed to be placed on each of its response control pins. This means an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low-pass filter on the receiver's input, shown in figure 4.25. In order to provide large pulse rejection, the capacitor needs to be quite large. Furthermore, the filter response is asymmetric, affording protection against positive noise voltage spikes only and will tend to attenuate rather than reject short noise pulses.

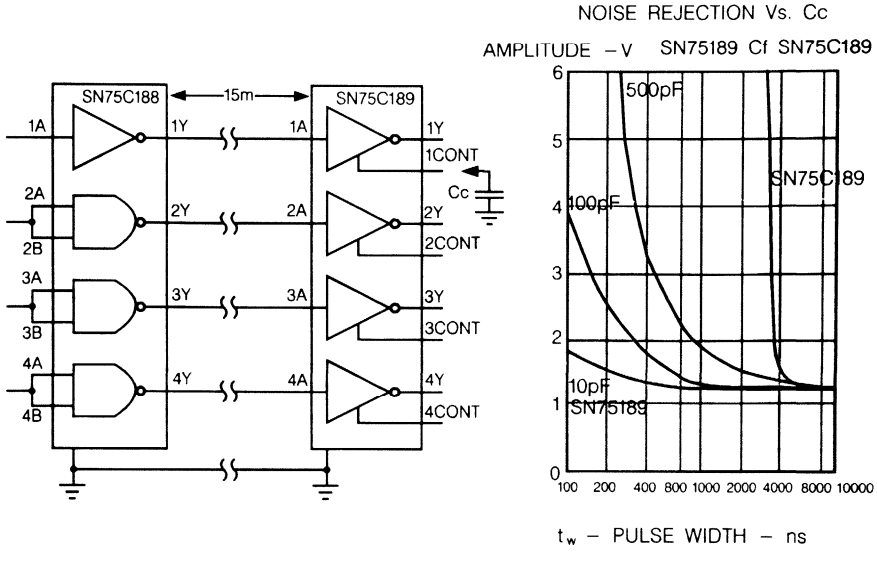


Figure 4.25 - Noise Filtering for EIA-232-D Interface

Receivers in the new TI. BiMOS driver/receiver family possess on-chip filtering, which reject fast transient noise pulses. Implementing the filters on-chip allows precise filters to be implemented without significantly altering the receivers response. These filters are totally symmetrical, offering protection against both positive and negative noise pulses and with the ability to reject rather than attenuate short noise pulses. To approach the level of filtering offered by the BiMOS receivers the standard receivers require much larger capacitors and even then fall well short of filtering requirements.

In summary, the advantages of these internal filters are in improved quality and reliability of filter operation, which can operate over the entire EIA-232 bps rate range.

3.9. Simplifying the System Interface

As the digital logic within systems become more integrated and operates from lower power supplies, it is logical that the interface circuits also need to be more integrated and consume less power. The BiMOS range of devices use low-power design techniques to integrate multiple driver/receiver elements into a single chip, thus meeting both these requirements.

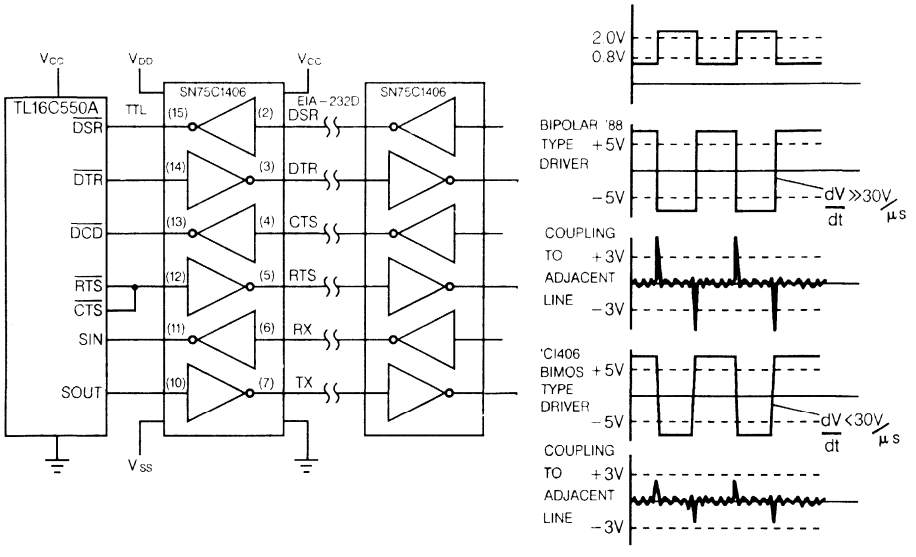


Figure 4.26 - Simplifying the System Interface

The following text describes the advantages of using single-chip multiple receiver/driver functions for common EIA-232 applications. The devices highlighted are the SN75C1406 (three drivers/three receivers) and SN75C1406 (four drivers/ four receivers).

Minimal EIA-232-D Interface

An absolute minimum system for EIA-232-D requires only six lines:

- $\overline{\text{RTS}}$ **Request to Send. DTE to DCE**
- $\overline{\text{DTR}}$ **Data Terminal Ready. DTE to DCE.**
- $\overline{\text{TX}}$ **Data Transmission line to DCE.**
- $\overline{\text{RX}}$ **Receive line**
- $\overline{\text{CTS}}$ **Clear to send. DCE to DTE**
- $\overline{\text{DSR}}$ **Data Set Ready. DCE to DTE.**

The **SN75C1406** and **SN75C1154** are low-power BiMOS EIA-232-D integrated circuits containing three driver/receiver pairs and four driver/receiver pairs, respectively. This makes them better able to provide the necessary interface signals within the same integrated circuit. The EIA-232 standard was devised for modem (DCE) to PC (DTE) interactions, but the applications of the interface signals have been expanded to include PC (DTE) to printer (DTE)interfaces.

When considering the latter case, the triple driver and receiver pairs of the 'C1406 make it an ideal choice. In these applications, only one extra signal will normally be applied – the Data Carrier Detect (DCD) signal, which can be amalgamated with the CTS signal. This gives only six interface lines plus the signal ground wire. The common term for this application is DTE-DTE zero modem and enables the DTEs to communicate without a DCE.

The timing of this operation is as follows:

i. **DTR** – One of the DTEs states that it is connected to the line, driving the DSR pin of the opposing DTE.

ii. **DSR** – The opposing DTE replies in the same way, announcing that it is connected.

iii. **DCD** – The DTE then checks the state of its DCD input. A low state implies that the opposing DTE's RTS output is low and not wishing to transfer information.

iv. **RTS** – The DTE is then able to drives its RTS input high, driving the opposing DTE's DCD input high and its own **CTS** input high.

v. **CTS** – Having driven its own CTS input high, the first DTE is now able to transmit the data it wished to send.

This is one such arrangement that allows one DTE to communicate with another DTE; there are however, many such arrangements. Each one of these arrangements puts a greater control of the flow of information on one of the key signal lines and is quite frequently dependent upon the type of DTE used.

The 'C1154 integrates a further driver/receiver pair into the chip, making it suitable for further EIA-232 applications. For example, the extra receiver input will allow the 'C1154 to monitor the Ring Indicator (RI) input from a modem or other similar type of DCE.

Like all their BiMOS counterparts the 'C1406 and 'C1154 offer high performance at very low power dissipation. All the receivers contain the same receiver filter as in the C189 receiver, so making them less sensitive noise induced onto the line. Another advantage with these devices is their drivers' on-chip slew rate limiting.

Slew Rate Limiting

When driving short lines fast changes in the voltage on one line can induce charge into an adjacent line. This can cause problems, especially when using short line lengths and can limit the speed at which data can be sent. The figure compares the performance of a bipolar '188 type device to the SN75C1406 device. It clearly shows the importance of slew-rate limiting when trying to maintain performance of the whole system.

The faster the driver output voltage is switched, the greater the amount of charge induced into the adjacent line. This charge will be converted into a voltage, and if the charge is large enough, the voltage on the line could cross through the receiver's input voltage threshold region, causing the receiver to falsely trigger. As the capacitance of the line increases with longer interface line lengths, these slew-rate-related effects become reduced.

The EIA-232-D standard specifies a maximum slew rate through the transition region of **30 V/µs**. Relating this to capacitance and current only 100 µA of output current into 30 pF load capacitance is needed to exceed the slew-rate limit. All devices are capable of supplying more than 5 mA. Therefore if the slew rate limit is not to be exceeded, the switching speed of the driver's output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of the loading capacitor required will depend upon the line length, but it is generally in the order of 330 pF. The effect of this capacitor is to cause the output transistors to saturate, causing it to short circuit current limit, thus preventing fast switching edges.

There are some major problems with this established process; one being the variance in current at which the output short-circuit current limit operates, especially when taking temperature changes into consideration. Again the value of capacitance placed on the line will depend upon the driver's output short-circuit capability as well as line length. For example a device capable of sourcing 10 mA will need a total capacitance of 330 pF placed on its output to meet the 30 V/µs slew rate limit, while placing this value across a device capable of sourcing 4 mA will have its slew rate limited to less than 12 V/µs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver will normally be close to one supply rail, so when it tries to switch to the other, the active transistor will have almost all of the supply voltages across it. The extra external capacitor will clamp the driver's voltage close to the supply voltage causing the output transistor to source large amounts of current. The combination of a large source current and large voltage cause it to dissipate large amounts of power. Operating at these prolonged bursts of high current will ultimately increase the chip temperature which in turn can affect the long-term life of the device. Bipolar technologies are normally much better able to withstand such effects

A better solution is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew-rate-limited operational amplifiers, the slew rate of line drivers can also be limited. Using the Miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The on-chip capacitors are normally in the order of 5 pF, while the currents driving the on-chip capacitor are the order of micro amperes, thus reducing power consumption within the device.

The biasing current to the output transistors is unaffected by this technique and will be more than sufficient to drive the 3 kΩ load as offered by the receiver.

3.10. SN75C185; The Optimised Solution

The SN75C185 driver/receiver is further testimony to Texas Instruments' commitment to the EIA-232 standard. Designed specifically for today's low-power applications, this device provides the designer with higher levels of system integration, reliability and optimisation than previously available. Figure 3.7 sets out the key features of the SN75C185.

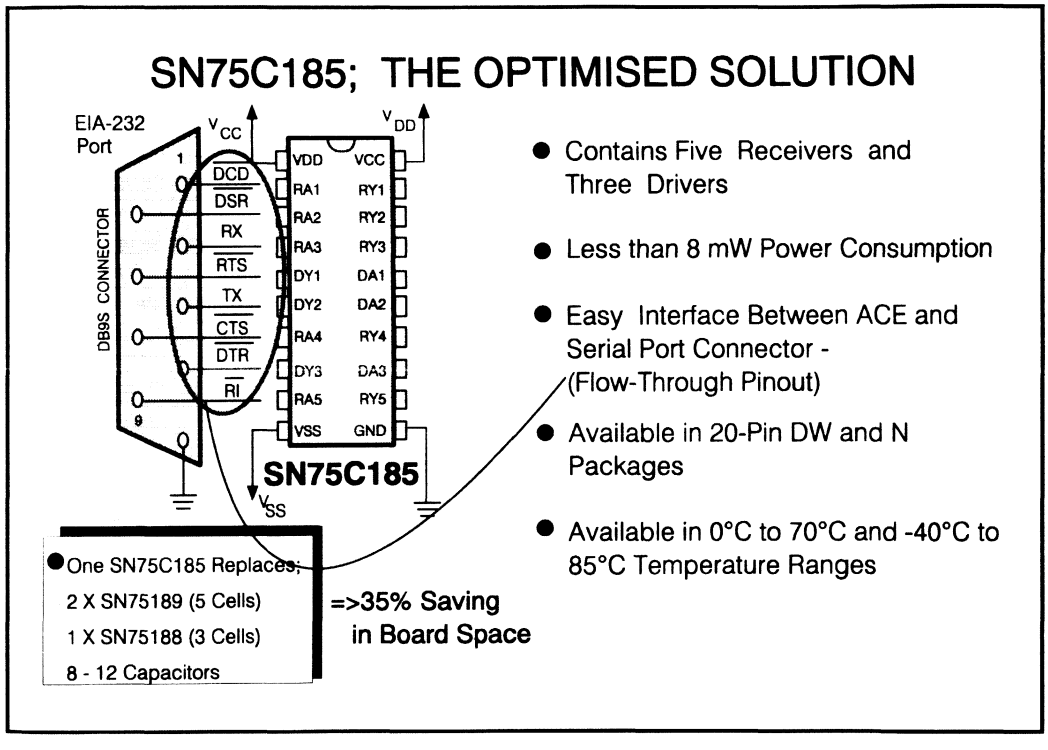


Figure 4.27 - SN75C185; The Optimised Solution

3.10.1. The DB9S Connector

The ever increasing use of portable/battery backed equipment such as the laptop PC, hand-held test and medical equipment has confronted the designer with many new challenges, namely, restricted power- supply, capacity, weight, battery operation, and restrictions in enclosure space. This situation is further aggravated by the consumer's ever increasing demand for higher performance solutions.

By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be provided – the SN75C185 provides just this. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/μs) and receiver filter implementation, all in a single 20-pin package

The rationale for integrating three drivers along with five receivers is easily understood by looking at common implementations of the EIA-232 standard. Although twenty-two signal lines are designated within EIA-232, far fewer are used in practice. The large number of handshaking lines and the absence of standard guidelines has led to a multitude of EIA-232 implementations – a fact not lost on EIA-232 users, as invariably the EIA-232 compatible PC will not communicate with its EIA-232-compatible printer!.

In an attempt to eliminate this problem, industry has formed a defacto standard around the combinations of handshaking lines shown in the figure 4.27. This is further illustrated by a casual look at the back of any laptop PC or hand-held test equipment that will reveal an ever- increasing use of the 9-pin (DB9S) connector, rather than the space consuming 25-pin (DB25S) connector.

The designer's dilemma is eased further by the use of a flow-through pin out architecture. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs, printed circuit board (PCB) layout can be greatly simplified.

3.10.2. Low Power as Well

In common with all of Texas Instruments BiMOS products, these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving, when compared to the alternatives is calculated in the following pages and is illustrated graphically in figure 4.28.

Available in either a single 20-pin, wide-bodied SO pack or DIP pack, the SN75C185 offers designers greater than 25% saving in board space, compared to alternatives.

3.11. SN75C185; Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially when using devices in confined spaces. These areas will normally have very poor air circulation, causing the ambient temperature of the whole system to increase.

These types of problems are particularly difficult to diagnose as failure can often be intermittent as devices pass into and out of thermal shutdown.

For these reasons, low quiescent-power devices are becoming a necessity for modern applications. As digital technologies advance, their power consumption decreases, making the interface circuits the limiting factor as far as system power consumption is concerned.

The **SN75C185** was designed with power consumption in mind. In addition it offers matched pin-out to industry-standard sockets and ACEs, as well as offering on-chip slew-rate limiting and on-chip noise filtering. Another benefit is that it contains three drivers and five receivers which is the minimum DTE requirement to interface to the EIA-232-D standard.

3.11.1. Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad-driver package and two quad-receiver packages; in the driver chip, one device is redundant while in the receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations below demonstrate this difference.

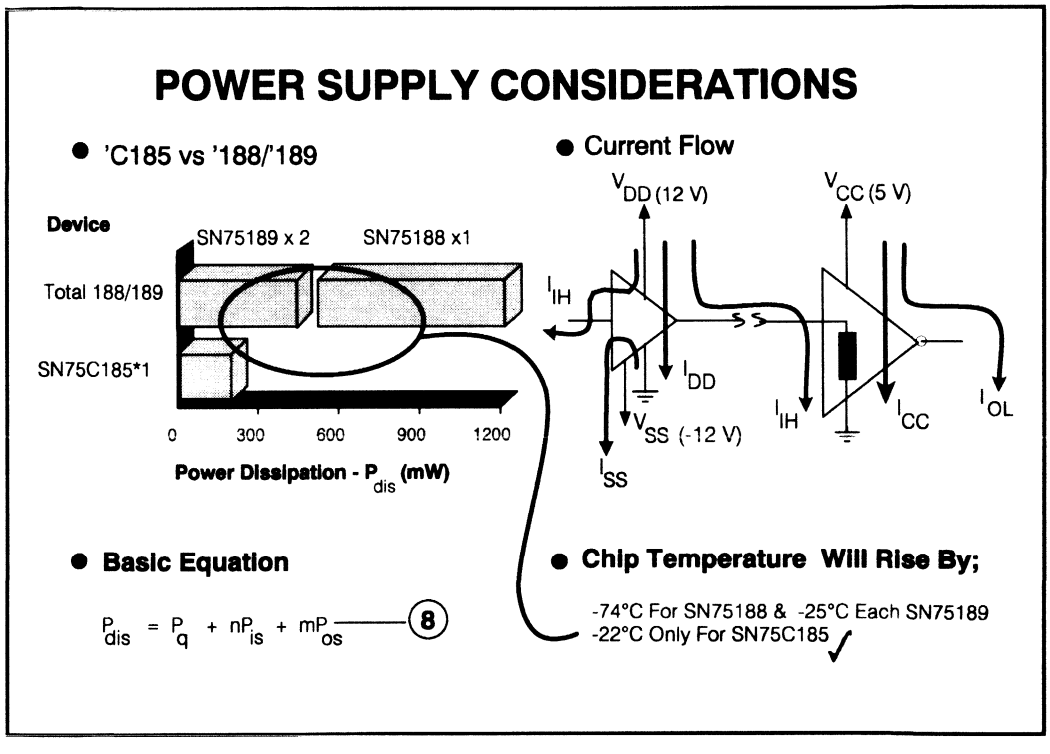


Figure 4.28 - SN75C185; Power Considerations

When comparing the 'C185 solution to that provided by the '88 and '89 devices, the power saving is enormous.

Both implementations require three supply voltages; a 5 V and ±12 V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576mW. In addition to this would be the power dissipated in the input stage, P_{isd}:-

$$P_{isd} = V_{CC} * I_{IL}$$

$$= 12 * 1.6 \text{ mW}$$

$$= 19.2 \text{ mW}.$$

This is multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{osd}, is:

$$P_{osd} = (V_{CC} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 9) * \frac{9}{3} \text{ mW}$$

$$= 9 \text{ mW}.$$

This figure will be multiplied by three to take into account the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$P_{dis} = 576 + 4 * 19.2 + 3 * 9 \text{ mW}$$

$$= 680 \text{ mW}.$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver.

$$P_{osr} = V_{OL} * I_{OL}$$

$$= 0.45 * 10 \text{ mW}$$

$$= 4.5 \text{ mW}$$

This power dissipated is multiplied by five to take into account the five receivers being used. The input stage can also dissipate some power, but this power is not supplied by this part of the interface system. The power dissipated within the IC will however cause the junction temperature to rise.

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{92}{3} \quad \text{mW}$$

$$= 27 \text{ mW}$$

This power dissipation is then multiplyed by five. The remaining receivers will require tying to a state where they will not be susceptible to noise. Tying them to the 5 V supply increases the power dissipation by a further 8.3 mW per receiver.

Assuming three receivers in one SN75189 are being used and two receivers in the other, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 4 * 27 + 3 * 4.5 \quad \text{mW}$$

$$= 233 \text{ mW}.$$

The power dissipated in the second receiver is:-

$$P_{dis} = 130 + 4 * 27 + 2 * 4.5 \quad \text{mW}$$

$$= 210\text{mW}.$$

This raises the temperature of the first and second receiver by 25°C and 23°C, respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling **1.12 W.**

Using the SN75C185

The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent- power consumption of the SN75C185 is equal to:-

$$P_q = V_{DD} * I_{DD} + V_{SS} * I_{SS} + V_{CC} * I_{CC}$$

$$= 12 * 200 + -12 * -200 + 5 * 750 \quad \mu\text{W}$$

$$= 8.55 \text{ mW}$$

The power dissipated in the input stage of the driver is:-

$$P_{isd} = V_{DD} * I_{IL}$$

$$= 12 * 1 \quad \mu\text{W}$$

$$= 12 \mu\text{W}.$$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output stage of the driver, P_{osd}, is:

$$P_{osd} = (V_{DD} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 10) * \frac{10}{3} \quad \text{mW}$$

$$= 6.67 \text{ mW}.$$

This is multiplied by three to take into account the three drivers driving the interface line, giving a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:

$$\begin{aligned} Posr &= V_{OL} * I_{OL} \\ &= 0.4 * 3.2 \quad mW \\ &= 1.28 \text{ mW} \end{aligned}$$

This value is multiplied by five giving a total of 6.4 mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

The power dissipated in the input stage, P_{isr}, equals:

$$\begin{aligned} P_{isr} &= \frac{V_{OH(d)}^2}{R_L} \\ &= \frac{10^2}{3} \quad mW \\ &= 33.3 \text{ mW} \end{aligned}$$

This power dissipation will also require multiplying by five. Giving a total input power dissipation of 167 mW.

Summing all the power contributors the total power dissipation is given by;

$$\begin{aligned} P_{dis} &= P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr} \\ &= 8.55 + 3 * 12*10\text{-}3 + 3 * 6.67 + 5 * 33.3 + 5 * 1.28 \quad mW \\ &= 201 \text{ mW}. \end{aligned}$$

The total power dissipated by the SN75C185 is **201 mW**

This is represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.

3.12. SN75186; Improve System Reliability

The following pages have been adapted from a linear application brief (Ref: LL181), that describes the unique features of the SN75186.

As today's electronic systems increase in complexity the need to improve system reliability and to add testability features (design-for-test) are fast becoming major concerns. Consideration of these factors early-on in the design phase not only give significant improvement in system mean-time-between-failure (MTBF) but could prove to be a major product differentiator.

The following pages describe how the unique features of the SN75186 may be applied to implement both a reliable EIA-232 link and one that can be tested without incurring system power-down.

The line interface circuit's proximity to the outside world, via the edge connector, make EIA-232 driver/receivers particularly vulnerable to failure. Furthermore as the number of I/O channels increase the likelihood of failure is not only more probable but increasingly difficult to diagnose. Consequently system designers are demanding increasingly robust EIA-232 circuits and ones that simplify fault diagnoses. The SN75186 has been designed specifically to address these needs.

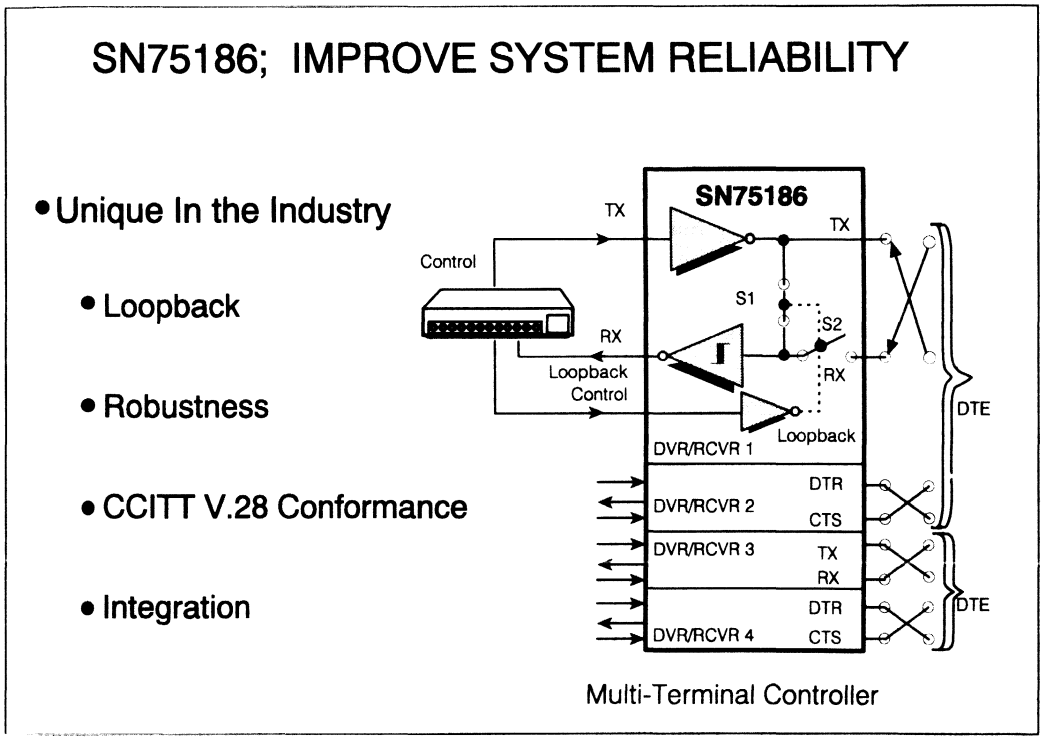


Figure 4.29 - SN75186; For High Reliability Designs

3.12.1. Integration

The combination of four drivers and four receivers, all conforming to the EIA-232-D and CCITT V.28 specifications, plus a unique loopback control circuit set the SN75186 apart from all other EIA-232 products. Furthermore, the integration of driver slew-rate control (30 V/µs) and receiver filter implementation (1µs pre-set filter) frees up board space and ensures reliable operation. Yet further levels of integration are achieved by the elimination of external diodes usually needed to prevent reverse current flow during EIA-232 power-off fault conditions. The SN75186 overcomes this need by presenting a high impedance (5kΩ) driver output whilst un-powered.

3.12.2. Reliability

The device's reliability is demonstrated by an ESD (electrostatic discharge) protection rating of 4000 V, and the ability to withstand ±30 V at any EIA-232 input or output – whether powered or un-

powered. Low power consumption, thermal overload and short circuit current protection are also added to significantly improve the long term reliability. In the unlikely event that failure should occur the SN75186 can be placed into loopback mode which allows the driver output to be fed back to the receiver input. Employing loopback in this manner allows software controlled testing of the SN75186 and aids the detection of line faults. Perhaps even more significantly these tests may be performed whilst the host controller remains powered.

3.12.3. Interface Vulnerability

Principle causes of line interface circuit failure are attributed to over thermal dissipation (use of devices with high quiescent power consumption) and to externally influenced events. Events such as line short circuits, excessive voltage spikes, ESD or physical damage due to incorrect cable insertion all conspire to cause either gradual performance reductions or catastrophic failure.

ESD is recognised as a primary source of semiconductor damage and failure- particularly during shipment, assembly and repair.

Contrary to popular belief both bipolar and CMOS structures are susceptible to ESD failure. For example CMOS structures can be destroyed by static voltages of less than 60 V, while bipolar devices can be damaged by voltages as low as 400 V.

The failure mechanism in both cases is different; CMOS structures being voltage sensitive are damaged by electrostatic fields that break down the dielectric isolation between the gate and source - quite often causing short circuits. Bipolar structures on the other hand are current sensitive, and are damaged by the currents that flow as a result of the fields present.

Device failure manifests itself as either a catastrophic failure, resulting in a complete functional failure, or a benign degradation that causes a gradual reduction in parametric performance.

Implementing ESD protection for CMOS logic devices is relatively simple since the applied input range lies within the supply voltages. Usually this protection circuit comprises of zener diodes connected between the supplies and series current limiting resistors. Protection of EIA-232 circuits proves far more difficult. Mainly because the receiver input is required to operate up to ±30 V which is well outside its 5 V supply. Even industry standard devices struggle to meet **this requirement adequately, and many fail at ESD voltages as low as 500 V.**

3.13. The Durable EIA-232 Solution

The SN75186 on the other hand boasts an ESD protection rating in excess of 4000 V when tested in compliance to MIL-STD-833C method-3015 and allows a full ±30 V (referenced to ground) to be applied to any EIA-232 input/output.

The receiver input, having a high input impedance, is more susceptible to charge-induced spikes than other inputs or outputs. Protection in this case is afforded by two sets of 45 V zener diodes polarised by two further diodes. It is this arrangement that allows the high range of input signals and provides the robust protection from ESD damage. The input of the driver is also protected by a zener diodes. Similar forms of protection are afforded to the supply voltages , V_{EE}, V_{CC1} and V_{CC2}, these pins can quite frequently be overlooked when considering ESD precautions. Figure 2 shows the results of impedance measurements conducted after exposing the devices to ESD stress. For a device to pass this parametric test the impedance must lie between 3 kΩ to 7 kΩ, as set by the EIA-232 standard.

Curve A and B depict industry standard device performance after exposure to ESD pulses of 2000 V and 4000 V respectively. Curve C indicates a clear pass for the SN75186 after exposure to 4000 V and industry standard devices after 1000 V

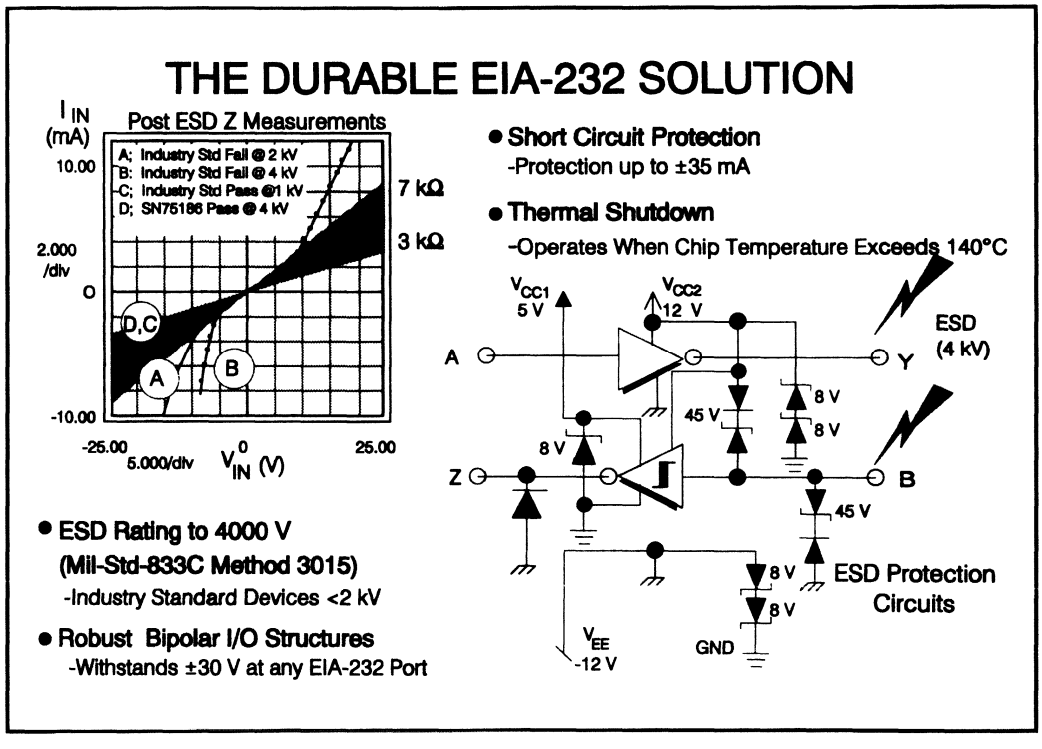


Figure 4.30 - The Durable EIA-232 Solution

Points A, B and C on the above curve show loopback detected fault conditions. These are indicated by a receiver output that fails to toggle in phase with the driver input, i.e. locks. A receiver output locked low indicates a short circuit to above -5 V (Points A and B) while a receiver output locked high indicates a short circuit to below VDD,-10 V (c).

In addition to excellent ESD handling capabilities the SN75186 also contains other protection features; for example the device contains short circuit current protection rated to a maximum of ±35 mA and thermal overload protection that operates when the chip temperature exceeds approximately 165°C.

The combination of these features coupled with low current operation surely make the SN75186 the most reliable device available today.

3.14. Loopback Operation

Fault location in data transmission systems has traditionally been problematic, mainly due to the difficulties in isolating the fault between the interface circuit and communications line. The accepted method of locating faults by disconnecting the cable and inserting a loopback connector is both time consuming and results unacceptable system down-time. This problem becomes even more acute as the number of I/O lines increase, in for example a multi-terminal cluster controller.

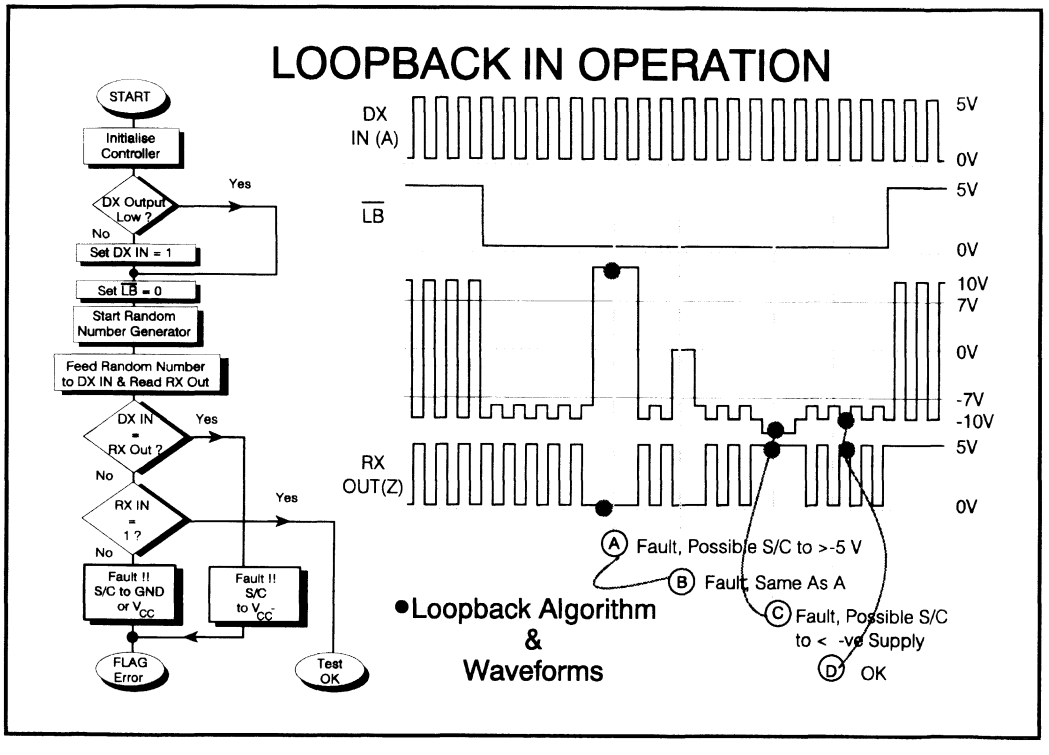


Figure 4.31 - Loopback Operation

The SN75186 not only addresses the issue of reliability but of testability too.

In *normal mode* operation the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs $\overline{LB}$ high. The voltage levels on the line are shown in figure 4.31, and normally swing between ±10 V. Taking $\overline{LB}$ low activates *loopback mode* in the corresponding driver/receiver pair. The output from the driver is then fed back to the input of the receiver through dedicated loopback circuitry. Data now available at the receiver output can then

compared with the data transmitted to determine correct functioning. Failure is indicated if the receiver output fails to toggle in phase with the driver input, i.e. locks high or low.

In loopback mode data external to loopback operation is ignored and the driver is prevented from causing the far-end receiver from changing state. This is achieved by clamping the driver output voltage well below the -5 V marking state required by EIA-232. Below this marking level, a reduced 1.5 V output amplitude is transmitted by the driver and is detected by an on-chip loopback comparator and fed to the input of the receiver to complete the loop.

Line faults external to the SN75186 can also detected by this operation. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = -12 V, line short circuits to voltages greater than -5 V and less than -12 V will be detected.

It is recommended that loopback is only entered when the driver output is low (< -7 V), that is the marking condition of EIA-232. Entering loopback when the driver output is high could result in a low-level, non-damaging oscillation at the driver output.

3.14.1. The TL16C552 ACE

Control of the SN75186 can be best implemented by use of the TL16C552 asynchronous control element (ACE).

The TL16C552 can serve two serial input/output ports simultaneously in either microcomputer or microprocessor based systems. In addition to its dual asynchronous serial capabilities the TL16C552 provides a full bi-directional parallel data port that fully supports the Centronix-type printer interface. In common with other ACEs within the TI family the device contains addressable and programmable registers that allow data, control and status information to be read and stored. Higher performance applications are served by the inclusion of 16-byte receive and transmit FIFOs that reduce the number of interrupts served on the CPU. In addition the TL16C552 contains two pins for each ACE that serve as dedicated handshaking lines for DMA control.

Figure 4.31 shows a simplified algorithm for controlling the SN75186 loopback function. Although a detailed discussion in the use of the TL16C552s registers is beyond the scope of this text (more complete information can be found in the TL16C552 data sheet) a brief discussion of the necessary control requirements follows;

3.15. SN75186 to TL16C552 Interface

3.15.1. Normal Mode

Control of the EIA-232 interface is implemented using the TL16C552's modem control and data signals. Although 3-outputs and 5-inputs are made available by each ACE not all control lines are necessary for many applications. For example the much simplified DTE to DTE (zero modem) interface shown in figure 4.32 requires only $\overline{DCD}$ and $\overline{DTR}$ control lines ($\overline{DCD}$ and $\overline{DSR}$ are tied together). The $\overline{RTS}$ line is used to initiate loopback and loops back SOUT to SIN and $\overline{DTR}$ to $\overline{DCD}$. Prior to data transmission each DTE is required to monitor its $\overline{DCD}$ input. A high level on this pin indicates that no transmission is currently taking place. In EIA-232 terms the line will be in

the mark state with a voltage around -10 V. Communications between the two DTEs can then commence by one DTE driving its $\overline{\text{DTR}}$ pin low thus driving the other DTEs' $\overline{\text{DSR}}$ and $\overline{\text{DCD}}$ pins low. The other DTE responds by driving its $\overline{\text{DTR}}$ pin low. Once these states have been attained the transfer of data between the two can commence. Communications will cease when either DTE takes its $\overline{\text{DTR}}$ output high.

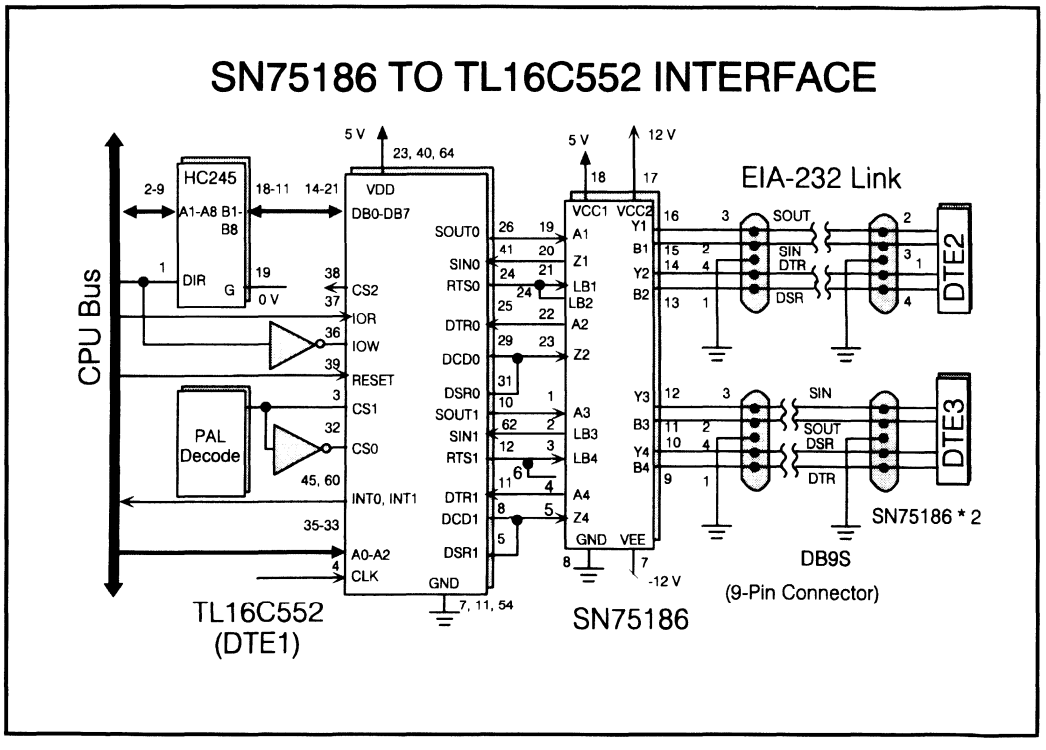


Figure 4.32 - SN75186 to TL16C552 Interface

Figure 4.32 shows a simplified dual DTE to DTE interface (Zero Modem) interface. Use of the SN75186 not only gives improved reliability but allows software controlled testing for both device and line faults. Minimal glue logic is needed, namely; the SN74HC245 octal latch (buffer function) and a PAL containing a chip select decoder and invertors. The parallel port capabilities of the TL16C552 have not been utilised in this application.

3.15.2. Loopback Mode (detail)

Before loopback mode can be entered the initiating DTE (*DTE1*) must first make sure all its driven outputs are set high. Thus ensuring that no communications activity is currently taking place and permits efficient operation of the loopback circuitry. Control is facilitated by use of the Modem-status register to check the state of the $\overline{\text{DCD}}$ input, and by setting the appropriate bits in the transmit holding register (to drive SOUT high). A low level at $\overline{\text{DCD}}$ indicates that *DTE2* is trying to initiate communications. Further communications may be prevented by programming the modem-control register to keep *DTE1s* $\overline{\text{DTR}}$ output high.

Once the above conditions have been satisfied loopback mode can be safely entered by bringing the $\overline{\text{RTS}}$ output low. The modem-control register is used to set $\overline{\text{RTS}}$ low. As with all registers, the modem-control register is selected by setting the appropriate bit on the address line (A0 to A2).

The functionality of both the EIA-232 line and the SN75186 can now be tested by the application of a pseudo-random code to the input of the SN75186 drivers, via SOUT and $\overline{\text{DTR}}$ (in this case).

The registers involved in this activity are the transmit holding registers (SOUT) and the receive holding registers (SIN) for one loopback pair and the modem-control register $\overline{\text{DCD}}$ and modem-status register (DCD) for the other. The line-control register will also be needed to set the format of characters sent via SOUT.

Since both the $\overline{\text{RTS}}$ and the $\overline{\text{DTR}}$ outputs of the ACE are controlled by the Modem-Control register special care is needed to ensure that the $\overline{\text{RTS}}$ (loopback initiator) bit is not overwritten when sending the pseudo random code through the $\overline{\text{DTR}}$ / $\overline{\text{DCD}}$ pair. This is easily achieved by writing a logic one to bit 1 (MCR1) every time the modem-control register is overwritten.

Design of the SN75186 is such that over 90% of the device can be tested in this manner, the remaining 10% has been designed so that the possibility of damage is very remote.

3.15.3. Further Control Considerations

Other control lines used in this application are;

$\overline{IOR}$ and $\overline{IOW}$: Used to set the direction of data via DB0-DB7 during register read/write operations.

$\overline{CS0}$ and $\overline{CS1}$: Chip selects used to select between the TL16C552s serial ports (port1 or port2). $\overline{\text{CS2}}$ is the parallel port select and is disabled.

$\overline{RESET}$: A low level on this pin sets the TL16C552 into idle mode and suspends all serial data activities. This pin is set low prior to operation to clear all serial registers.

CLK: Clock input (DC to 8 MHz) fed to the bps rate divisors.

Other registers involved in both loopback and normal mode are the divisor latches used to set the bps rate through SOUT.

3.16. High Data Rates and Long Line Lengths

The SN75186's loopback function and its robust input and output structures enable it to be used in areas hitherto not possible for high reliability data transmission. In addition to this is the device's large output drive capability that opens up new possibilities for higher data rate and longer line length applications.

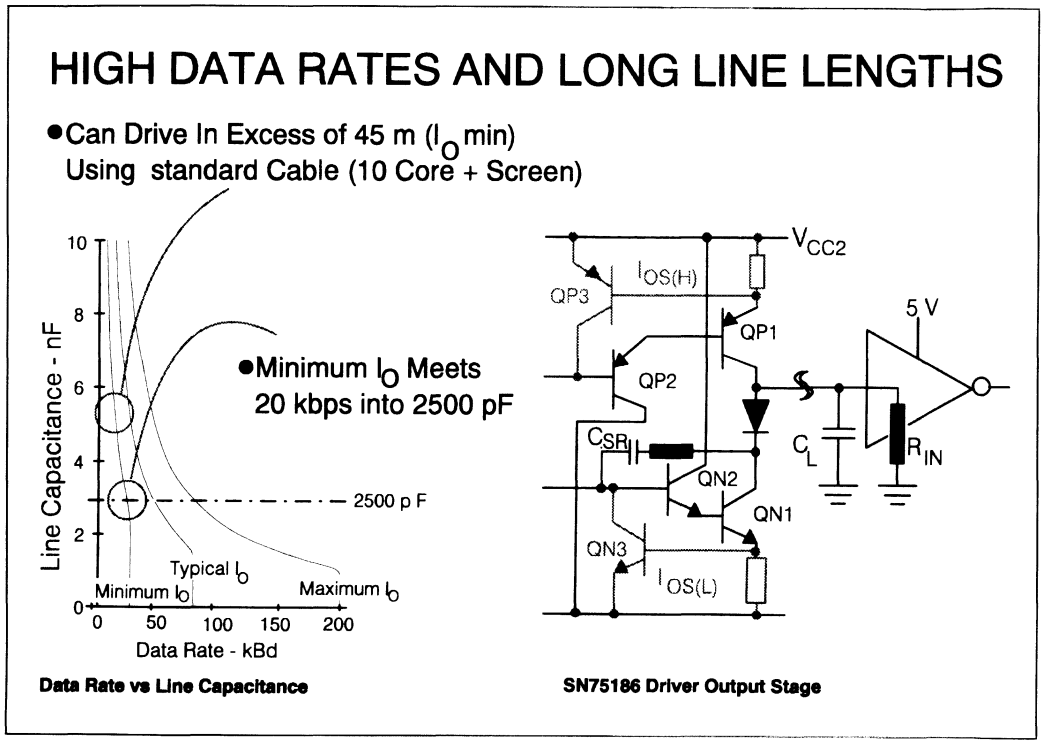


Figure 4.33 - High Data Rates and Long Line Lengths

The EIA-232 standard was designed specifically for the modem interface, hence its relatively low data rate (20 kbps) and modest line length of 15 m. However, the increased acceptance of the EIA-232 standard has given raise to application areas previously outside the capabilities of standard devices. Increasingly higher data rates and longer line length drive capability are being required.

Again the SN75186 is more than a match, not only in reliability and integration but in speed and line length drive capability also.

3.16.1. Internal Slew Rate Control

The EIA-232 standard specifies a maximum slew rate of 30 V/μs. In order to meet this specification, and to reduce cross-talk between adjacent lines, a driver output shunting capacitor is usually needed. The effect of this capacitor, usually around 330 pF in value, is to cause the drivers output transistors to saturate causing them to short circuit current limit, thus preventing fast transition edges. As well as being an additional expense this practice is unreliable as operation depends upon chip temperature, line loading capacitance (line length) and device output current.

Many modern devices integrate this control on-chip, however as before special care is needed to ensure the slew rate limit circuitry does not limit the line length drive capability. The SN75186 contains special slew rate control circuitry that limits the rate of the rising and falling edges without starving the output driving transistors of drive current- the SN75186 has a minimum output current of 10 mA.

3.16.2. High Data Rate

The maximum speed of data transmission is defined by the ratio of the time through the transition region (-3 V to +3 V) to the unit interval time period. EIA-232 specifies this ratio as 4%. As the cable length gets longer, the time taken to pass through the transition region increases due to the line's extra capacitance. Therefore the line capacitance and the driver's output current capability place a limitation on the maximum speed of data transmission. Figure 4.33 shows how the driver output current varies with output voltage.

The rate at which the output voltage ramps down depends on the internal slew rate limit and the output current. If the device is driving short line lengths the slew rate control will dominate and will be unaffected by the current limit. Therefore the output current will be very much smaller than 10 mA. In this case the time taken to pass through the transition region will be approximately 200 ns, allowing very high data rates.

However when driving long line lengths then the current limit will dominate and will depend on the peak current flowing out of the device. Current limit would come into effect almost immediately and will remain active throughout the transition region. This now introduces a minimum time limit through the transition region of :-

$$t_T = R_i * C_l * \ln\left(\frac{|R_i * I_o| + |V_f|}{|R_i * I_o| - |V_i|}\right)$$

The voltage levels, V_f and V_i, used in this equation are the extremes of the transition region. Assuming a typical current limit of 20 mA and a receiver input resistance of 5 kΩ, the typical time taken to pass through the transition region would be :-

$$t_T = 300 * C_l \quad \text{seconds.}$$

The effect of this equation and how it affects the data rate and line length can be seen in figure 4.33.

For example, taking the maximum EIA-232 cable capacitance , 2500 pF, and following the typical output current curve the SN75186 is capable of data rates around 50 kbps. Obviously if the transition time to unit interval ratio was relaxed the speed could be increased yet further. Following the maximum output current curve, for the same line capacitance, data rates of approximately 116 kbps can be achieved. These curves also allow the line length to be determined. At a line data rate of 20 kbps, and following the minimum curve, a load capacitance of approximately 8 nF may be driven. Using a standard cable of 180 pF/m this equates to a line length of approximately 45 m.

3.16.3. Receiver Filtering

In addition to the noise reducing internal slew rate control circuitry, the SN75186 also has noise rejecting filters on the inputs of the receivers. These filters reject noise with periods less than 1 µs.

Previously filtering was achieved by external capacitors connected to an on-chip resistor to form a low pass filter. This not only gave poor asymmetrical filtering response (Filters positive going noise pulses only) but a relatively poor frequency response. This can be problematic when transmitting data at high rates since problems in data timing and synchronising can occur.

The filters included in the SN75186 are both symmetrical and provide excellent noise rejection.

3.17. Modern Technology Charge Pumps

One recurring problem for EIA-232 users is the necessity for dual-supply rails; that is 12 V and -12 V. This is in addition to a 5 V supply rail, meaning that a total of three regulators are required, the largest being the 5 V. Linear regulators can only step down voltages, so it is not possible to convert the 5 V supply to a 12 V supply, nor can they invert the supply's polarity. The first regulators capable of performing such tasks are inductive switching regulators, but these can be noisy and require a lot of peripheral passive components. Another drawback, particularly for system integration is the large inductor and the power switch required. No one has yet been able to integrate inductors onto monolithic integrated circuits (except by the use of gyrators).Therefore, until recently, no cost effective solution for EIA-232 power supply generation has been available.

An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is then transferred into a holding reservoir capacitor that is then used to supply the output voltages. Furthermore such a scheme can be integrated into silicon. Using the network of capacitors shown in figure 3.14 both voltage doublers and invertors can be made.

3.17.1. Charge Pump Operation

Charge-pump operation is best explained as a series of phases; There are four phases used that provide the clocking signals to control the distribution of charge. Phases 1 and 3 are used to provide voltage doubling and phases 2 and 4 provide voltage inversion.

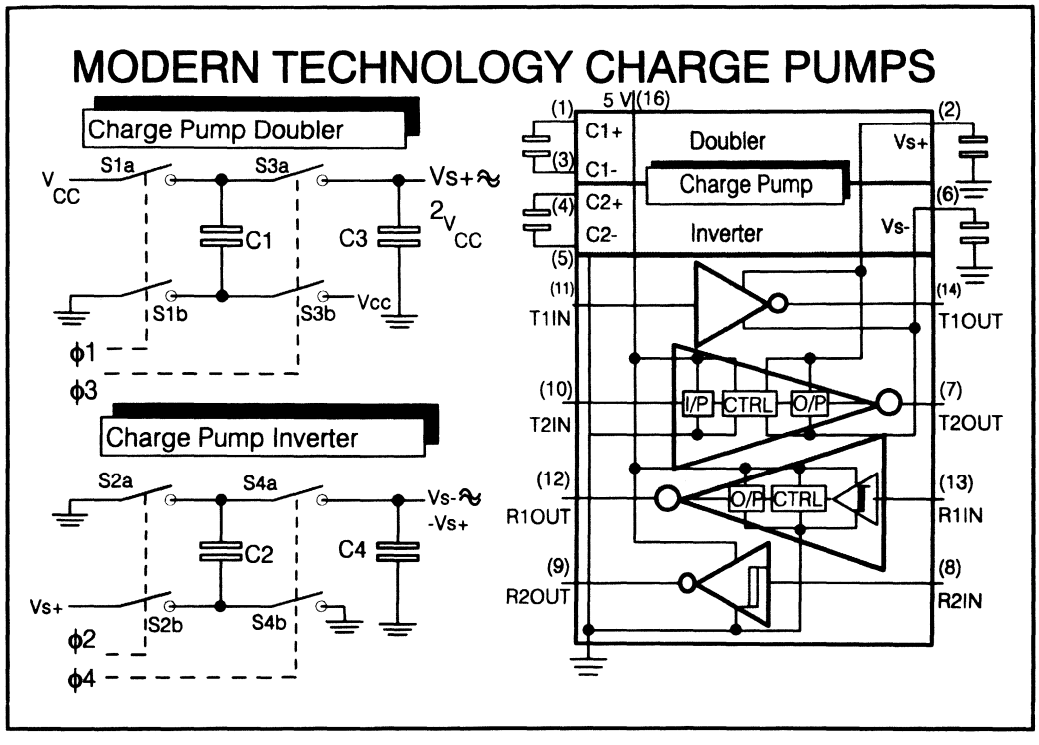


Figure 4.34 - Modern Technology Charge Pumps

Phases 1 and 3

During phase 1 the first pair of switches (S1a and S1b) close allowing capacitor C1 to charge up via V_{CC}. C3 supplies the load current. During phase 3, switches S1 open and switches S3 close thus transferring the charge stored in C1 on top of the supply voltage. This means that relative to ground, the voltage on the top plate of C1 is now twice Vcc. The charge on C1 now charges up C3 in addition to supplying the load current. This process, assuming ideal switches, doubles the supply voltage.

The doubled voltage is now applied to a further bank of switches and capacitors to provide voltage inversion. In this operation, phases 2 and 4 are similar in operation to phases 1 and 3.

Using this technique, it is possible to convert the 5 V digital supply to a positive 8.5 V supply and a negative 8.5 V supply.

This form of regulator, now known as a **CHARGE PUMP** has not only been integrated onto silicon, but has also been coupled with EIA-232 drivers and receivers to make a EIA-232 line interface system capable of working from a single supply.

TI has three variants of such a device available today, with many more planned: the **LT1080/1** and the **MAX232** both of which are fast becoming industry standard devices. Although working on similar

principles they use different technologies, and the choice of technology can have a large effect on the overall performance of the system, just as it has in logic systems.

The original version of the MAX232 was fabricated in a CMOS process. This can cause reliability problems due to an inherent thyristor structure giving latch-up susceptibility.

In order to meet the relatively large currents and/or voltages required by data transmission circuits, CMOS technologies need large geometry's and large area output devices. The large geometry's enable the devices to withstand higher voltages, while the large area enables the device to pass larger currents. The larger the area of the device, the larger the parasitic capacitance associated with the device. This means that with CMOS processes there will be a voltage, current, speed, and cost compromise. The higher the current, the harder it can be to provide the speed.

To overcome many of these problems, TI fabricated its MAX232 product using the LinBiCMOS™ process.

3.17.2. The LT1080 From Texas Instruments

LT1080 and LT1081 are dual-driver/receiver pairs featuring an internal charge-pump which facilitates single-supply operation. Two 1 µF capacitors are required for the charge pump operation and two additional 1 µF capacitors are used for smoothing of the generated dual voltages. These devices are designed to avoid latch-up and provide a realistic balance between CMOS levels of power-dissipation and real-world requirements for ruggedness. The driver outputs are fully protected against overload and can be shorted to ± 30 V.

The charge pump provides enough current for driving low power external circuitry such as other EIA-232 drivers or op amps. However, they should be loaded with care, since excessive loading can cause the generated supply voltages to drop, causing the EIA-232 driver output voltages to fall below EIA-232 requirements.

The LT1080 features a shutdown mode that, in addition to a power reduction, puts both the driver and receiver outputs in high-impedance states. This, in addittion to a suuply current of just 320 µA allows several devices to share a receiver and driver line. It should be noted that use of devices in this manner is not covered by the EIA-232 specification.

The key features of the LT108/81 are summarised;

- **Dual Driver Receiver Pair**
- **Operates from a single Supply**
  -Generates ±9 V using two 1 µF Capacitors
  -Can Supply Additional Low Power EIA-232 Devices
- **Three State Outputs**
- **Robust Bipolar Design**
  -No Latch up
  -Can With Stand ±30 V at any EIA-232 Terminal

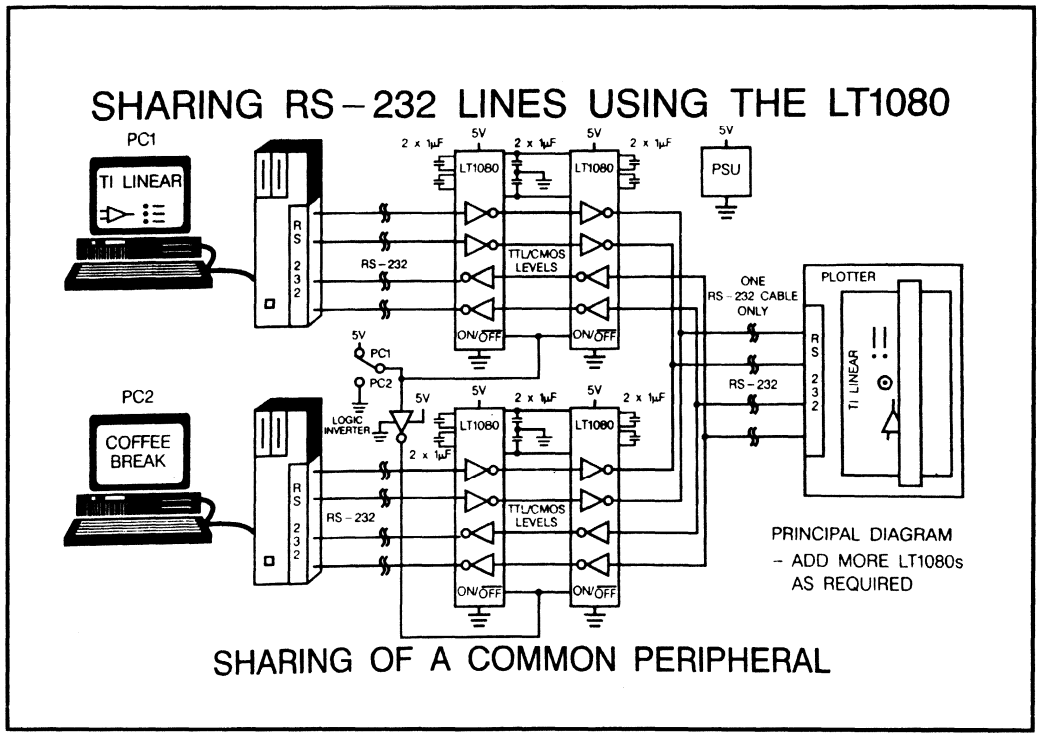


Figure 4.35 - Sharing EIA-232 Lines Using The LT1080

3.18. Sharing EIA-232 Lines Using The LT1080

3.18.1. Three State Operation

Placing the LT1080 in the **shutdown mode** by taking the ON/$\overline{\text{OFF}}$ pin **low** reduces the supply current into its V_{CC} pin to less than 100 µA. In addition, enabling shutdown puts both the EIA-232 driver and receiver outputs in a high-impedance state with leakage currents below 100 µA and 10 µA respectively. Control of the shutdown mode is simple since the ON/$\overline{\text{OFF}}$ pin is CMOS/TTL compatible, with a logic **high** fully enabling the device.

The virtual zero current consumption in shutdown mode can benefit power conscious systems in data off periods. However, this feature also allows drivers and receivers from different devices to share common EIA-232 lines, opening up new applications areas. Shifting between the two modes takes approximately 1 ms.

3.18.2. Parallel Connection

Parallel connection of driver outputs and receiver inputs of two LT1080s, and enabling /disabling them with an alternating control scheme, allow two DTEs to share a common peripheral.

The example illustrated shows two PCs, both having access to a common plotter through the same EIA-232 cable. If the plotter is not used frequently, even a simple manual switch at the PC side of the data communications cable is acceptable for shifting the plotter EIA-232 link from one PC to the other. This method is more reliable and convenient than fumbling with cables on the back of PCs to change the plotter host. When peripherals need more than two driver lines and two receiver lines, add more LT1080s.

Sharing EIA-232 lines in this fashion can be transferred to many other application areas, bearing in mind that such interconnections are not covered by the EIA-232-D. Care should also be taken, since excessive loading of a driver with more than one receiver's input impedance can cause the driver's output voltage swing to fall below EIA-232 requirements. In the application shown, two PCs sharing a common peripheral, additional output drive capability will be required on the plotter side.

3.19. Bidirectional Communication with LT1080

Connecting the driver outputs of one LT1080 to the receiver inputs of another, and vice versa, and using their power ON/ $\overline{\text{OFF}}$ function allows the LT1080 to operate as a true transceiver, enabling bi-directional communication.

Parallel connecting both driver outputs and inputs as well as receiver inputs and outputs of two LT1080s, and enabling/disabling them with an alternating control scheme allows true transceiver operation for bi-directional communication.

3.19.1. LT1080 Transceiver Application

The example illustrated in figure 4.37 shows two DTEs, each implemented by two LT1080s in the transceiver mode, sharing four bi-directional lines. Three of the lines are used for handshaking, while the other is for data, but all are bi-directional. Theoretically, more than two stations can be connected to the communication line to form a low data rate mini-LAN, but each driver needs to be capable of driving all receiver inputs simultaneously. As EIA-232-D devices are not designed for this purpose, care should be exercised to ensure that enough drive capability is available to pass through the receiver's input threshold region with an acceptable slew rate to reduce susceptibility to noise. In applications where the LT1080 drivers are driving two receiver inputs, worst case data sheet parameter designs means that conformance to minimum EIA-232-D line level requirements can not be guaranteed. However tests conducted on this application, the communication worked perfectly.

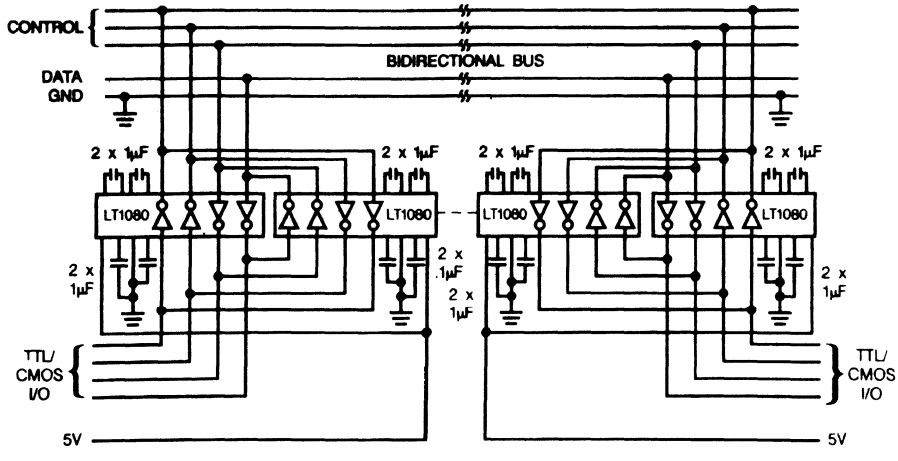


Figure 4.36 - Bidirectional Communication with LT1080

3.19.2. The MAX232

For more cost sensitive applications the MAX232 may be preferred. The MAX232 is functionally equivalent to both the LT1080 and the LT1081 and shares the same pin-out as the LT1081.

The MAX232, designed using Texas Instruments LinBiCMOS process, is a dual- driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels (standard specifies a voltage between ±5 V to ±15 V) from a single 5 V logic supply.

Each receiver converts EIA-232 voltage level inputs to a 5 V TTL/CMOS level. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V and can accept ±30 V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels.

LinASIC™ Cells

The driver, receiver, and voltage generator functions are all available as cells in the Texas Instruments LinASIC cell library. This will allow future integration with more complex devices such as Texas instruments range of ACEs.

The key features of the MAX232 are summarised;

- **Dual Driver Receiver Pair**
- **Operates from a Single 5 V Supply**
- **Lower Cost Alternative to the LT1081**
- **Designed Using LinBiCMOS**
- **Available as Cells in the LinASIC Cell Library**
- **Available in both Standard SO and Wide Bodied SO Packages**

3.19.3. An Objective Comparison Between the LT1080/81 and the MAX232

The differences between the LT1080/81 and the MAX232 have been somewhat eroded with the advent of Texas instruments' LinBiCMOS process. There are however, still some differences that will be of importance for certain applications. These key differences are shown in the accompanying tables and described below:

	MAX232	LT1080	LT1081	Units
Device				
No of Pins	16	18	16	
Pin-out	As LT1081		As MAX232	
I_{CC}	10 (max)	22 (max)	22 (max)	mA
Shutdown	No	320	No	µA
Technology	LinBiCMOS	Bipolar	Bipolar	
Driver				
V_{OUT}	V^- + 0.3 to V^+ - 0.3	V^- + 30 to V^+ - 30	V^- + 30 to V^+ - 30	V
I_{IN}	200	20	20	µA
$I_{S/C}$	±10	±12 (typ)	±12 (max)	mA
Slew-Rate	30 (max)	4 (min) to 30 (max)	4 (min) to 30 (max)	V/µs
Receiver				
V_{IN}	±30	±30	±30	V
$V_{OUT(H)}$	3 @ -1 mA	3.5 @ -160 µA	3.5 @ -160 µA	V
$V_{OUT(L)}$	0.4 @ 3.2 mA	0.4 @ 1.6 mA	0.4 @ 1.6 mA	V
$V_{(HYST)}$	0.2 to 1	0.1 to 1	0.1 to 1	V

For EIA-232 purists (the EIA-232 standard does not specify 3-state conditions) MAX232 represents the best option for low-power applications , with a driver and receiver quiescent current of just 10 mA (the line current needs to be added to give the total current drain).

However if the drivers/receivers are inactive for long periods, then a 3-state (shutdown) feature may be preferred. In the 3-state mode, the line is in effect disconnected, resulting in negligible line current .

The LT1080 contains such a feature, applying a logic low to the LT1080's ON/$\overline{\text{OFF}}$ pin placing the receivers and drivers of the device into a high-impedance state. A logic high will restore the device to normal operation.

The current consumed during shutdown can be calculated as follows:

$$2 \times \{I_{OZ\,(Driver)}\} + 2 \times \{I_{OZ(Receiver)}\} + I_{CC(Off)}$$

$$\{2 \times 100.10^{-6}\} + \{2 \times 10.10^{-6}\} + 100.10^{-6} = 320\ \mu A$$

The LT1080/81, as you would expect from a totally bipolar process, has a slightly wider output voltage range, making it more suitable for applications operating in electrically hostile environments. The voltage range is specified from V- +30 V to V+ -30 V, meaning that if the supply output voltages are ± 9 V, then external voltages of up to ± 21 V can be applied to the driver outputs without incurring device damage.

One final difference is in the receiver TTL/CMOS drive capability. The drive capability relative to a standard TTL gate requiring an I_{IH} of 40 µA and an I_{IL} of -1.6 mA is shown below:

Parameter	MAX232		LT1080	
		Fan out		Fan out
$I_{(OH)}$	-1 mA	25	-160 µA	4
$I_{(OL)}$	3.2 mA	2	1.6 mA	1

From the table above, for worst-case design, the MAX232 has the greater current drive capability with a fanout of 2.

3.20. EIA-232..... 3 kV Opto Isolation

Galvanic Isolation

The capability to meet toughened noise legislation is a key requirement for many new end- products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any EIA-232-D interface is galvanic isolation.

Such isolation in data communication systems is achieved without direct connection or wires between the EIA-232 interface devices and the DTE/DCE. Magnetic linkage from transformers provide the power for the system and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages that can affect the signal are also eliminated. Common-mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique. To take a more practical view, two examples are mentioned where problems are likely to occur without an isolated interface:

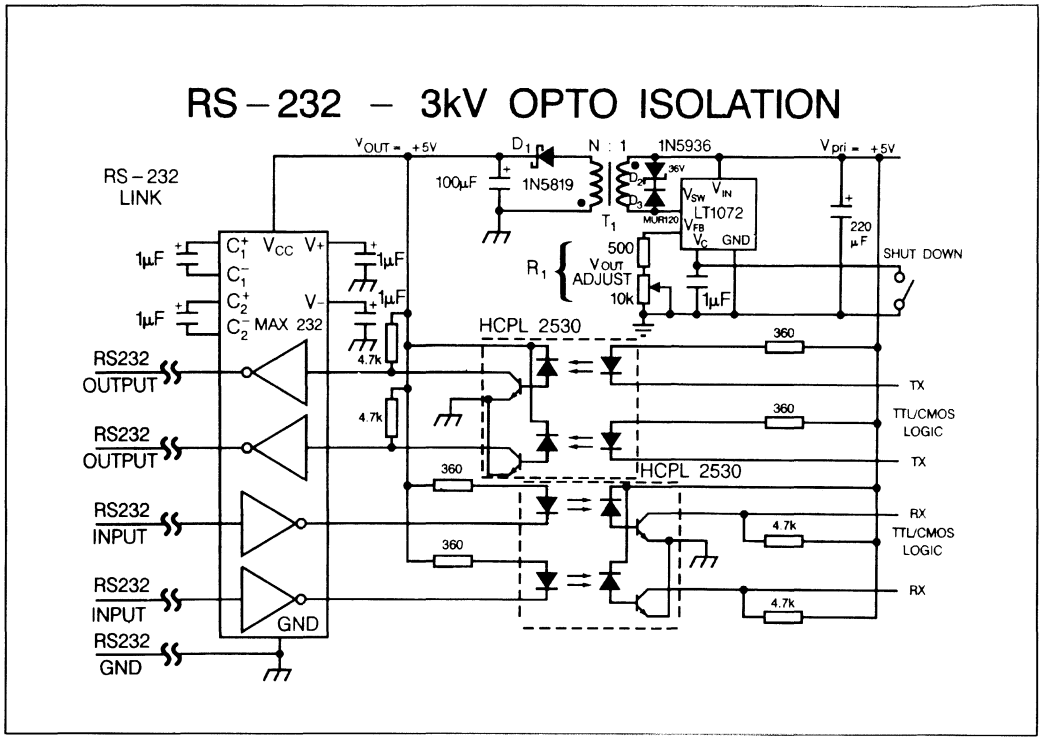


Figure 4.37 - EIA-232..... 3 kV Opto Isolation

Firstly, when using an EIA-232 line to connect two pieces of equipment placed in different rooms or buildings, the ground potentials can differ by several volts. An indication of a possible problem is if a spark is seen at the connector housing, when joining these "grounds" with an EIA-232 cable. The spark itself may be harmless, but fluctuating levels of noise current should be expected when the cable is connected. With a high enough level, these noise currents may cause unreliable or faulty data transmission.

Secondly, in manufacturing environments where an EIA-232 link connects a data logger to a host computer and large motors are used, problems are also likely to happen. When a motor is started up, it can induce a momentary substantial difference in ground potentials at the data logger and the computer due to surge current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and at worst, damage to the computer may occur.

3.20.1. Simple Opto Isolated EIA-232 Design

The EIA-232, 3 kV opto isolation application shown has two galvanic barriers; a transformer, T_1, providing magnetic transfer of power to the EIA-232 dual driver and receiver, MAX232, and two dual-opto couplers, HCPL2530, making an isolated data path available. The circuit used is applicable to other Texas Instruments EIA-232 drivers and receivers than the shown MAX232. However, in many industrial applications, a simple CTS/DTR handshaking scheme is adopted, which suits two drivers and

two receivers. If more handshaking lines are required, the MAX232's built-in charge pump can also drive a SN75C1406, triple driver, and receiver.

Opto coupling performed by two Texas Instruments dual HCPL2530 allows fast data transfer limited, only by the MAX232's capability, typically in excess of 64 kbps. For lower data rates, HCPL2730 is adequate.

An isolation voltage of 3 kV is provided by these couplers. The isolated 5 V supply for the MAX232 is generated from the 5 V logic supply by Texas Instruments LT1072 switching regulator. The LT1072 has no electrical connection to the load; instead, the circuit derives its feedback from the transformer's fly back voltage.

This technique is often referred to as an isolated fly back regulator. The switching regulator needs to deliver only modest current levels (100 mA) allowing a physically small isolation transformer. Although a 5 V logic supply is assumed, flexibility of the design allows easy adaptation to other regulated or unregulated input levels, from 4.5 V to 15 V, by changing the 360 Ω resistors to provide approximately 10 mA current through the LEDs. In the isolated feedback mode, the LT1072 does not use the feedback pin to sense output voltage; instead it senses and regulates the transformer primary voltage during the LT1072's switch off time. This voltage is related to the output voltage, V_O by:

$$V_O = N * V_{pri} - V_f$$

Where, N = turns ratio of transformer, V_f = forward voltage of rectifying output diode and V_{pri} = primary voltage during switch off. The secondary voltage will be stable if V_{pri} is regulated. LT1072 switches from the normal mode (feedback provided from a potential resistor divider across the regulated secondary output) to regulated primary mode when the current *out* of the feedback pin, V_{FB}, exceeds ≅10 μA. An internal clamp holds the voltage, V_{FB}, on this pin at approximately 400 mV. The resistor from the V_{FB} pin to ground is used to put the LT1072 in isolated feedback mode. V_{pri} is regulated to 16 V +7 kΩ(V_{FB}/R_1), where the 16V is the LT1072's internal fly back mode reference voltage, V_{FB}/R_1 is equal to the current through R_1, and the 7 kΩ is an internal resistor. V_O is therefore given by:

$$V_O = N\left(16\ V + 7\ k\Omega\left(\frac{V_{FB}}{R_1}\right)\right) - V_f; \quad (1)$$

Re-arranging the equation gives the turn ratio:

$$N = \frac{V_O + V_f}{16\ V + 7\ k\Omega\left(\frac{V_{FB}}{R_1}\right)}; \quad (2)$$

The feedback pin voltage, V_{FB} is about 0.4V for R_1 = 8.2 kΩ, but the actual voltage depends on resistor value since the feedback pin has about 200 Ω output impedance in this mode. From this information, V_{FB} can be given by:

$$V_{FB} = 0.41\ V \frac{R_1}{200 + R_1}; \quad (3)$$

Choosing R_1 as a fixed 500 Ω resistor in series with a 10 kΩ potentiometer allows for some adjustment of the output voltage. As the voltage according to (1) is not linear with R_1, an adjusted value of R_1 = 1.4 kΩ resulting in V_{FB} = 0.359 V, was found to give a good variation around 5 V. This resistor value is then used as basis to determine the transformer's turns ratio, N, from (2):

$$N = \frac{5\ V + 0.4\ V}{16\ V + 7\ k\Omega\left(\frac{0.359V}{1.4\ k\Omega}\right)} = 0.303;$$

Varying R_1 between 500 Ω and 10.5 kΩ results, according to (1) and (3), in a secondary output voltage, V_{out}, range of 5.7 V to 4.5 V.

Details of the transformer design is outside the scope of this data transmission section but is important for achieving the overall switching regulator performance and isolation voltage requirements. Please refer to the data sheet and available literature on switching regulator transformer design.

A snubber network consisting of a fast turn-on, high break down diode, D_3, and a 36 V zener diode, D_2, limits the magnitude of the leakage inductance spike. Using a zener diode rather than a resistor in parallel with a capacitor improves efficiency because it minimises the duration of the inductance spike. A Schottky diode, D_1, in the secondary reduces the voltage loss to the output and increases efficiency. To save power in data off periods the LT1072 shutdown function can be activated by shorting V_{CC} to ground. This switch function can be implemented by a MOSFET transistor controlled by digital circuitry or software. The power consumption for the complete application is reduced to less than 1.25 mW in the shutdown mode.

3.21. SN75LBC187; Optimised For Laptops

The following describes a device currently under development, the reader is advised to contact a TI representative for the latest details of product availability.

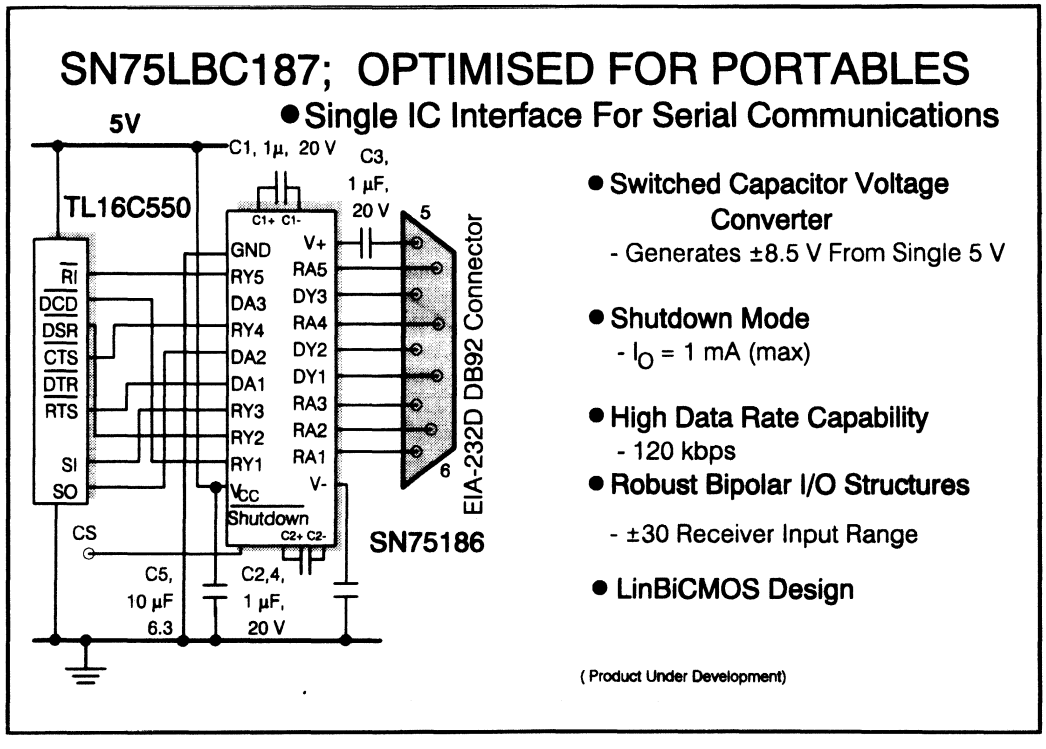


Figure 4.38 - SN75LBC187; Optimised For Laptops

The SN75LBC187 is a low Power LinBiCMOS device containing three independent drivers and receivers, and a switched-capacitor voltage converter. The SN75LBC187 provides a single 5 V supply interface between the asynchronous communications element (ACE) and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to standards ANSI/EIA-232-D-1986 and EIA/TIA-562 and CCITT recommendation V.28.

The switched-capacitor voltage converter of the SN75LBC187 uses four small external capacitors to generate the positive and negative voltages required by EIA-232 (and CCITT V.28) line drivers from a single 5 V logic supply input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without sustaining damage.

The device also features a reduced power or shutdown mode that virtually eliminates the quiescent power supply when the IC. is not active.

The SN75LBC187 has been designed using LinBiCMOS technology and as a consequence the cells developed are available in the Texas Instruments LinASIC library. The SN75LBC187 is characterised over 0°C to 70°C temperature range.

3.22. LT1039; The Listening Device

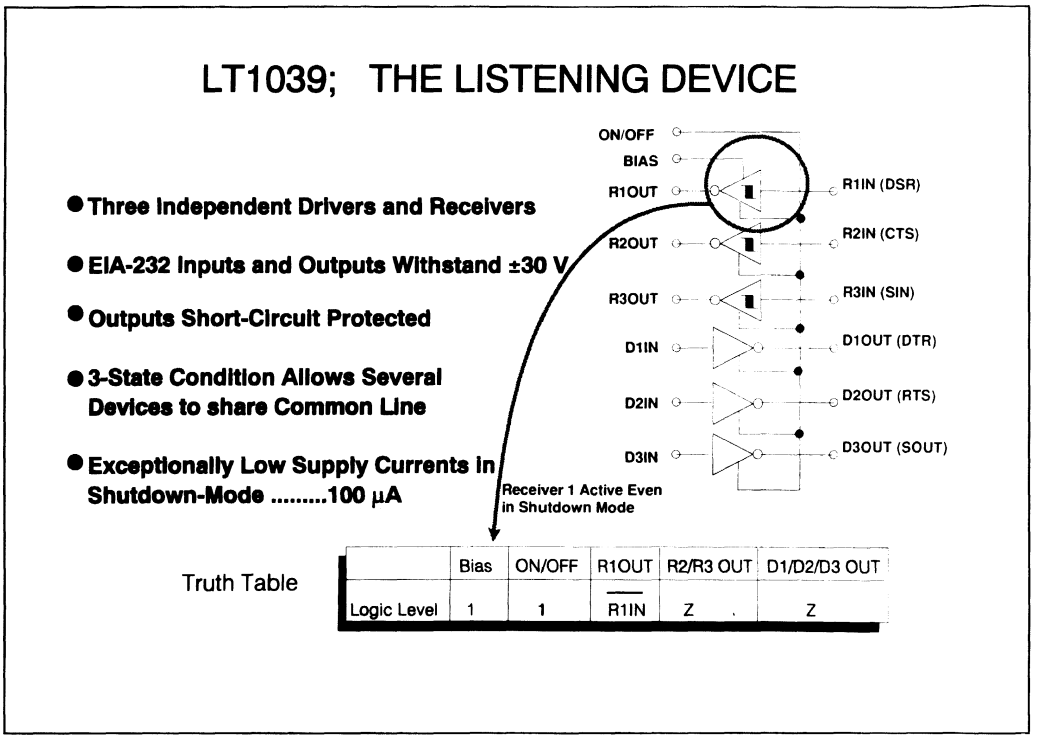


Figure 4.39 - LT1039; The Listening Device

The LT1039 is a triple line driver/receiver designed to meet the requirements of the EIA-232 and CCITT V.28 standards.

All outputs are fully protected against voltage overloads or outputs short circuits. A major advantage of the LT1039 is the high-impedance driver output state, that allows low quiescent supply currents when the device is either off or powered down. This feature also allows several devices to share a common bus.

An important additional feature is the bias control pin that allows receiver 1 to remain active even when the device is shutdown. This permits the device to permanently monitor the handshake lines for communications activity.

3.23. The Texas Instruments ACE Family

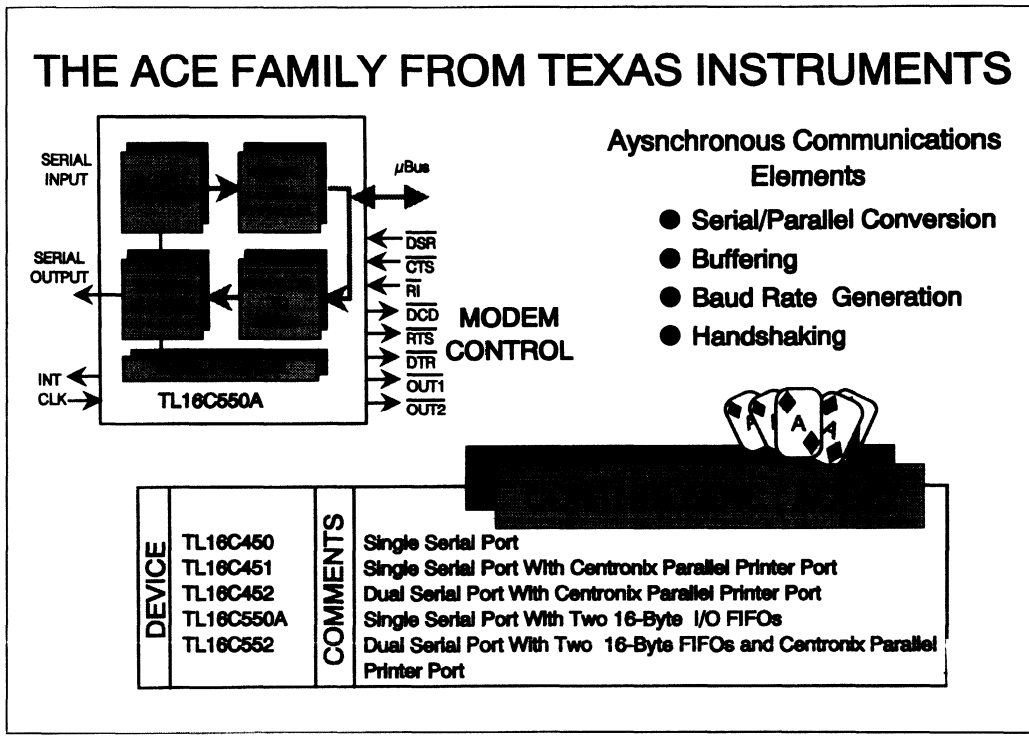


Figure 4.40 - The Texas Instruments ACE Family

Most EIA-232 systems use dedicated communication controllers. Termed ACEs (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter), these devices are responsible for controlling the exchange of information over the EIA-232 interface.

The ACE

The ACE is a dedicated asynchronous communications controller designed to off load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add or delete start and stop bits and provide odd/even parity code generation and detection. Industry standard devices such as the **TL16C450** family contain many extra features as listed below:

- **Programmable bps-rate generator**
- **Adds and deletes standard asynchronous communication bit**
- **Fully programmable serial interface characteristics**
- **Data communication diagnostic capability**
- **Modem-control functions**
- **Simple interface to microprocessors**
- **Maximum data rate of 256 k bits per second**

All devices are designed using Texas instruments EPIC^{TM} CMOS process and operate from a single 5 V supply. The **TL16C450** is the most common choice for standard PC applications as well as many other asynchronous serial applications. The TL16C450, housed in a 40-pin package, contains all the necessary facilities for implementing a single asynchronous serial port. The CPU within the system can read and report on the status of the ACE at any point in the ACEs operation. Reported status information includes the type of transfer operation in progress, the status of the operation, and any error conditions encountered, parity, overrun etc.

The TL16C450 ACE includes a programmable, on-board, bps-rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} -1) and producing a 16 x clock for dividing the internal transmitter logic. Provisions are included to use this 16 x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimise the computing required to handle the communications link. The **TL16C451** is similar to TL16C450 with the single serial port, but also contains a Centronix parallel printer port. The IBM PC AT/XT sets the standard for this parallel printer interface that all "compatible" manufactures have to follow. TTL-level signals are presented on a 25-pin D-type socket. Apart from the choice of connector, this parrallel printer port is directly compatible with the "Centronix" standard printer interface. The **TL16C452** has two serial ports plus a parallel Centronix printer port. Using this ACE together with two SN75C185s provides a simple three chip complete solution for the two EIA-232 ports plus a printer port that is common on basic PC configurations.

3.23.1. The FIFO (First-In-First Out)

The CPU can send data at much faster rates than a normal ACE can handle. This is particularly true for today's multitasking applications that demand high performance microprocessors. This can be expensive in CPU overheads as the CPU will be tied to the speed of the serial interface, i.e., data will be transferred over the interface through the ACE and onto the CPU bus. This is true also when the data is exchanged from the CPU to interface via the ACE.

Devices like the **TL16C550A** and **TL16C552** alleviate this problem by including buffer registers and FIFOs in series with the ACE's transmitter and receiver. These are quick access registers that hold data until the CPU can be freed. The CPU can then execute a block read or write.

The ACE is, in effect, isolated from the slow communications channel.

The TL16C550A is similar to the TL16C450, but two 16-byte FIFOs are included to buffer the transceiver and receiver data stream, further reducing the number of interrupts from the

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microprocessor.

3.23.2. Forward-Looking Performance With Backward Compatibility

By allowing two modes of operation, the TL16C550A allows users to maintain software compatibility with earlier industry standard ACEs such as the TL16C450. In addition to the TL16C450 mode, the TL16C550A can operate in the FIFO mode. In FIFO mode, two 16-byte FIFOs (First-In-First-Out) are enabled to relieve the CPU of excessive software overheads. The independent receive and transmit FIFOs act as buffers, vastly reducing the number of interrupts required. Furthermore two dedicated pins serve as handshaking lines to a DMA (Direct Memory Access) controller, thus allowing the FIFOs to load and unload data without direct intervention from the CPU.

The flagship of the range is the TL16C552, which is similar to the TL16C452 in structure but with the added advantage of input/output FIFOs as in the TL16CC550A

This device serves two serial input/output interfaces simultaneously in either microcomputer or microprocessor-based systems. In addition to its dual asynchronous serial communication capabilities, the TL16C552 provides a fully bi-directional parallel data port that fully supports the parallel Centronix-type printer. The parallel port and the two serial ports provide IBM PC/AT compatible computers with a single low-power device to serve the three-port system. Like the TL16C550A, the TL16C552 contains 16-byte receive and transmit FIFOs that act as buffers to reduce the number of interrupts on the CPU. Also in common with the TL16C550A, the device contains two pins for each ACE that serve as handshaking lines for DMA control. The TL16C552 is housed in a 68-pin plastic-leaded chip carrier, PLCC.

Integration of FIFO and DMA signalling circuitry onto a single chip makes the TL16C550A and TL16C552 one of the most efficient solutions for higher performance multitasking systems.

3.24. Interfacing Between the TL16C550A and the SN75C185

The circuit shown demonstrates the simplicity, in hardware terms, in implementing an asynchronous serial interface with the SN75C185 driver/receiver and the communications controller TL16550A.

When interfacing between the TL16C550A ACE and the Intel CPU bus, minimal glue logic is required. Namely an 'LS245 Octal bus transceiver is used to provide drive current to an 'off-card' CPU, and programmable array logic (PAL) to decode address lines and generate a chip select signal. While an exhaustive description of this interface is beyond the scope of this section, a discussion of key interface lines can be useful.

Xin/Xout:
External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$,RCLK:

The transmitter reference clock is available externally via the $\overline{\text{baudout}}$ pin. In this application bpsout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock rate is established by the reference oscillator clock frequency (xin) and divided by a driver specified by the bps generator divisor latches.

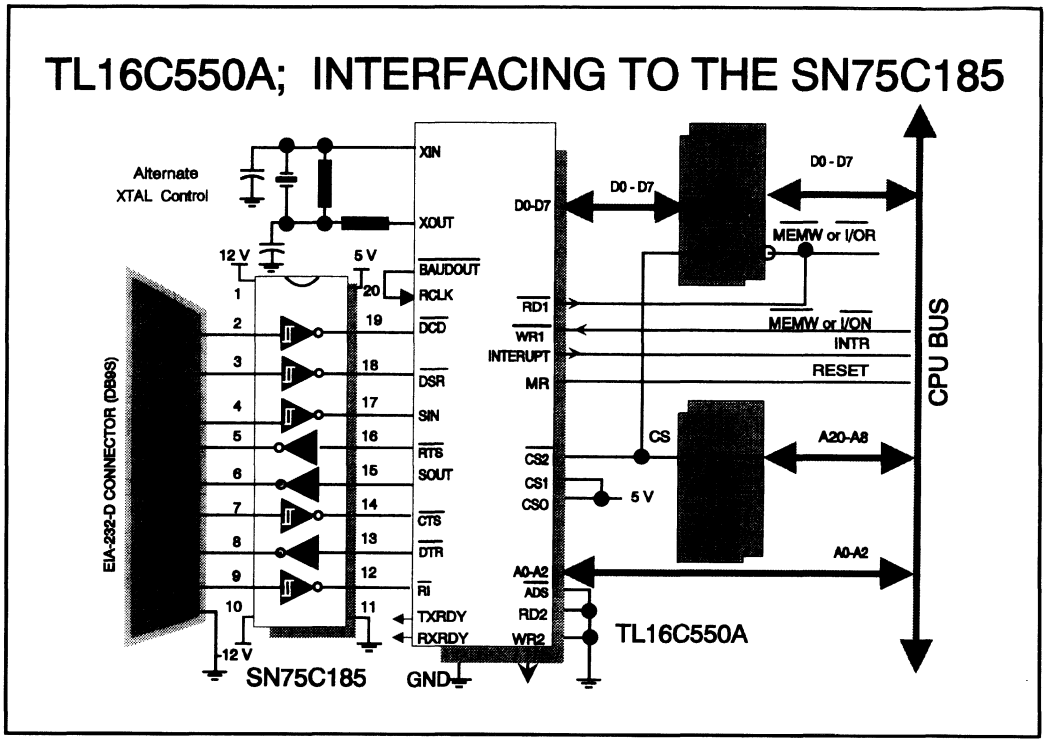


Figure 4.41 - Interfacing Between the TL16C550A and the SN75C185

$\overline{\text{TXRDY}}$:

Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$:

Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7:

Databus. Eight 3-state data lines provide the bi-directional path for data, control, and status information between the ACE and CPU bus.

$\overline{\text{RD1}}$, RD2:

Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from the selected ACE register. Since only one of these inputs is required for the transfer of data during the read operation, RD2 is tied to its inactive state, i.e., low.

$\overline{\text{DCD}}$, $\overline{\text{DSR}}$, SIN, $\overline{\text{RTS}}$, SOUT, $\overline{\text{CTS}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$:

These signals are the EIA-232 compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between ±5 V to ±15 V. The signal can then be transmitted over distances of up to 15 m.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example, driving/receiving combinations precisely match the interface requirement, plus the pin-out is aligned directly to the DB9S connector.

$\overline{\text{WR1}}$, WR2:

Write inputs. A logic applied to $\overline{\text{WRI}}$, during ACE selection allows the CPU to write either control words or data into a selected ACE registers. WR2 is tied in active, i.e.: logic low.

INTERRUPT:
When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

- **Receiver error**
- **Received data available or time-out (FIFO mode only)**
- **Transmitter holding register empty**
- **Enabler modem status interrupt**

The interrupt is reset (deactivated) either when the interrupt has been serviced or by a master reset (MR).

MR:
Master reset. When active (high), MR clears most ACE registers and sets the states of various outputs (i.e. interrupt).

CS0, CS1, $\overline{\text{CS2}}$:

Chip Select. An active low on the $\overline{\text{CS2}}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{\text{CS2}}$ chip select. A logic high on $\overline{\text{CS2}}$ will de-select the ACE.

A0 to A2:
Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example, providing the correct write/read operation had taken place at logic 0 at A2, A1, and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{\text{ADS}}$:

Address strobe. An active low on $\overline{\text{ADS}}$, the register select signals (A0 TO A2) and chip-select signal ($\overline{\text{CS2}}$) drive the internal logic directly.

3.25. EIA-232 Products Summary

Texas Instruments is continually developing new products in support of the EIA-232 standard. As can be seen from the products discussed, particular emphasis has been placed on devices offering high levels of system integration, optimisation and robustness of design. All designs have been made with today's low-power requirements in mind. Detailed discussion of all key parameters is beyond the scope of this text, so for more detailed information and an overview of Texas instruments complete range of devices, the reader's attention is drawn to the current Linear Interface Circuits Data Book. The following tables show the current range of devices for the EIA-232 standard, new device featured in this section are shown in the accompanying figure.

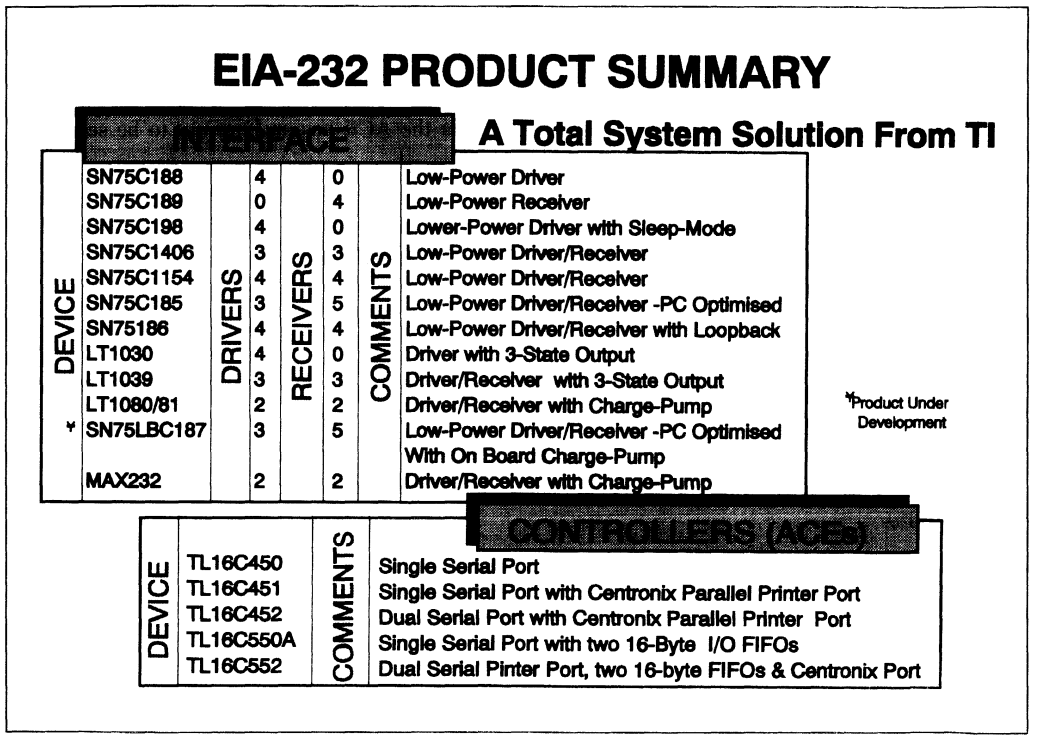


Figure 4.42 - EIA-232 Products Summary

3.25.1. Selection Guide

Data Transmission Circuits

Function	Per Package	Type	Features
	2	SN75150	Industry Standard
		UA9636AC	Industry Standard
Line Driver	4	LT1030	Robust bipolar design, with 3-state driver outputs
		SN55188	–55°C to 125°C temperature range
		SN75188	Industry standard
		SN65C188	–40°C to 85°C temperature range
		SN75C188	Low-power BiMOS
		SN65C198	–40°C to 85°C temperature range
		SN75C198	Low-power BiMOS with sleep-mode

Line Receiver	4	SN75154	Industry standard
		SN55189	-55°C to 125°C temperature range
		SN75189	Industry standard
		SN55189A	-55°C to 125°C temperature range
		SN75189A	-55°C to 125°C temperature range
		SN65C189	-40°C to 85°C temperature range
		SN65C189A	-40°C to 85°C temperature range
		SN75C189	Low-power BiMOS
		SN75C189A	Low-power BiMOS

Line Driver/ Receiver	1/1	SN75155	On-chip 5-v regulator
	2/2	MAX232	On-chip charge pump
	2/2	LT1080	On-chip charge pump and 3-state outputs
	2/2	LT10801	On-chip charge pump
	3/3	LT1039	Robust bipolar design, with 3-state outputs
	3/3	SN65C1406	–40°C to 85°C temperature range
	3/3	SN75C1406	Low-power BiMOS
	4/4	SN75186	Robust bipolar design, with loopback
	4/4	SN65C1154	–40°C to 85°C temperature range
	4/4	SN75C1154	Low-power BiMOS
	3/5	SN65C185	–40°C to 85°C temperature range
	3/5	SN75C185	Optimised for DB9S (9-pin) connector
	3/5	SN75LBC187	Optimised for Laptop Applications¥

Notes

Control Circuits

Function	Type	Features
ACE+	TL16C450	Single ACE
	TL16C451	Single ACE with parallel port
	TL16C452	Dual ACE with parallel port
	TL16C550A	Single ACE with FIFO§
	TL16C552	Dual ACE with parallel port and FIFO

+ ACE: Asynchronous Communications Element.
§ FIFO: First In First Out.
¥ Product currently under development, contact TI representative for further details.

Of particular note is not only the range of products that are offered but that both line driving/receiving functions and controller elements are supported – ***a total system solution.***

Future developments will see an ever-increasing use of the LinBiCMOS process. That by combining the benefits of both bipolar and CMOS will allow line driving/receiving functions to be merged with the high-density controller functions. Furthermore the low power of LinBiCMOS will allow multiple line driving/receiving functions to be integrated along with voltage charge pumps, 1992 will also see the release of devices capable of 3 V EIA-232 operation.

4. Interface Circuits For EIA RS-422 & RS-485

4.1. The Need for Balanced Transmission Line Standards

This section focuses on two of industries most widely used balanced transmission line standards, the EIA RS-422 and the EIA RS-485. After reviewing key aspects of these standards, the reader will be introduced to the practicalities of implementing a differential transmission scheme. Finally, several new additions to Texas Instruments EIA product range will be discussed and where appropriate, their application.

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-422 and **RS-485** are balanced (differential) digital transmission line interfaces developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to l0 Mbps and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

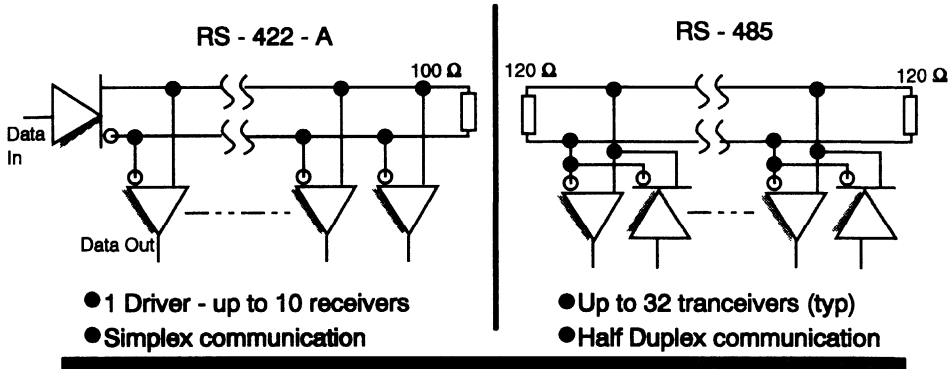
4.1.1. Application Areas

RS-422 offers a reliable multi-point one way communication. A typical application area is its use in transmitting data from a central computer to multiple remote monitors, printers or stations, such as airport arrival and departure monitors.

RS-485 is an upgraded version of RS-422 extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bi-directional multi-point party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the electrical specification of their standard. Examples include the ANSI (American Nationals Standards Institute) Small Computer Systems Interface (SCSI).

4.2. EIA RS-422-A and EIA RS-485 Differences



Maximum common mode voltage	- 7 V to + 7 V	-7 V to + 12 V
Receiver input resistance	4 kΩ	12 kΩ
Driver load	100 Ω	60 Ω
Driver output short circuit limit	150mA to GND	150mA to GND 250 mA to -7 V or 12 V

Figure 4.43 - EIA RS-422-A and EIA RS-485 Differences

4.2.1. EIA RS-422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422-A) in December 1978 bringing it in line with its present specifications.

A RS-422 line allows for only one way communication (simplex mode) but by using a differential twisted pair transmission media (not specified in std.) and a RS-422 receiver with its minimum 7 V common mode voltage capability makes it less susceptible to noise picked up in hostile environments, via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10 Mbps are supported and a line length up to 1200 metres is given as guide-line, but not at the maximum data rate.

When operating at low data rates (below 200 kbps), or at any speed where the ratio of the driver's output rise time to the one-way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedance's lie in the range of 100Ω to 120Ω. A termination resistor with an impedance similar to the cable's characteristic impedance should only be connected at the furthest end of the cable.

4.2.2. EIA RS-485

The Increased use of balanced data transmission lines in distributing data to several system components and peripherals over relatively long lines brought about the need for multiple driver/receiver combinations on a single twisted pair line. Hence, an upgraded version of EIA RS-422-A , named EIA RS-485, was introduced in 1983.

RS-485 takes into account RS-422 requirements for balanced-line data transmission plus additional features allowing for multiple drivers and receivers. The guide-lines for data transmission speed, cable lengths and media are the same as for RS-422.

The Differences

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multi-point communications.

Driver features

i. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

ii. The driver output, off-state, leakage current shall be 100 µA or less with any line voltage from -7 V to +12 V.

iii. The driver shall be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from -7 V to 12 V.

iv. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

Receiver features

i. High receiver input resistance, 12 kΩ minimum.

ii. A receiver input common-mode range of -7 V to 12 V.

iii. Differential input sensitivity of ±200 mV over a common-mode range of -7 V to 12 V.

4.3. EIA RS-485 /422 Product /Application Trends

Propriety systems designers are beginning to recognise the inherent advantages of a balanced, differential, transmission scheme over the single ended interface. Such advantages are higher noise immunity, lower noise emissions and improved signal quality. These facts are also not lost on

independent standards committees which are starting to embrace RS-485 as the electrical part of their overall specification. Furthermore those systems not following the RS-485 specification verbatim are recognising the virtues of Texas Instruments' range of differential driver/receivers, particularly the high speed/low power ALS options.

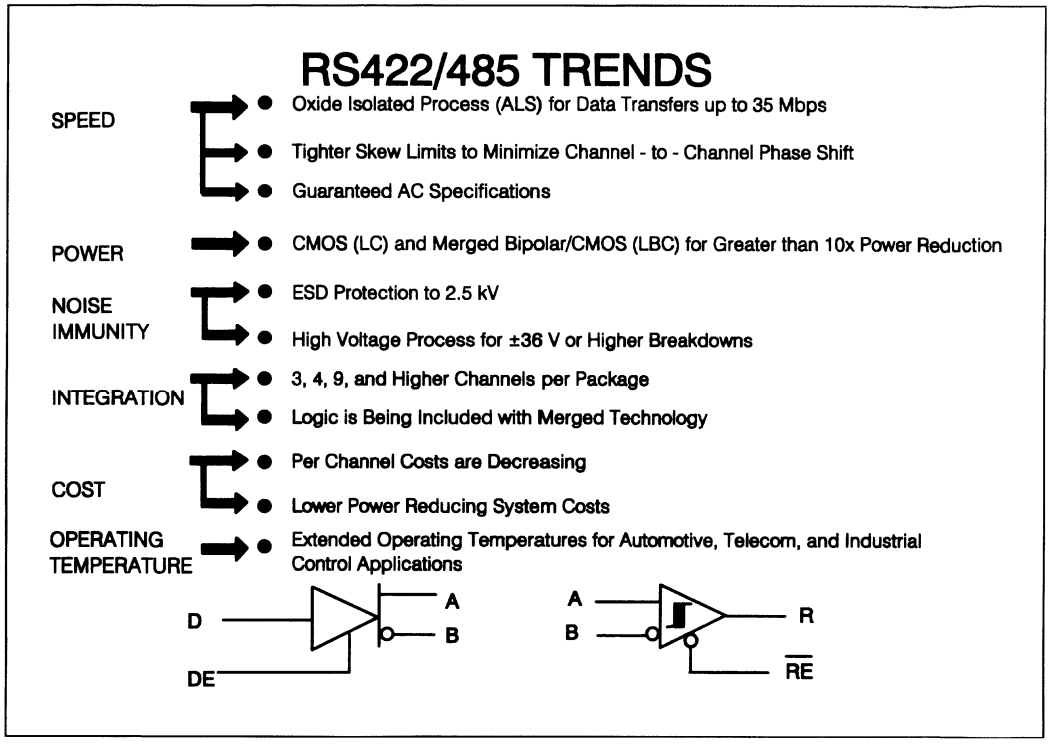


Figure 4.44 - EIA RS-485 /422 Product /Application Trends

Representatives of those standards bodies employing a differential transmission scheme can be found in most industries, some examples are listed below;

i) **Computer;** The ANSI-X3T9.2-1986 Small Computer Systems Interface (SCSI)

ii) **Computer;** ANSI X.3129-1986 Intelligent Peripheral Interface (IPI)

iii) **Automotive multiplex Wiring;** CAN, VAN and SAE J1850

iv) **Telecommunications;**

v) **Factory Automation;** P-Net (A derivative of Field bus)

Each one of these application areas makes its own demands on the processing technology used. Examples of these demands are guaranteed AC specifications and increased data rate capability. In particular, tighter skew specifications are needed for both telecommunication and computer applications, however the interpretation of skew can differ. For example, telecommunication

applications are more concerned with device skew, that is the difference between the positive and negative edges of the differential output voltage. A low skew value in this case would represent a lower likelihood of noise radiation. For the computer application, SCSI, a low bus skew is required. In a SCSI there can be as many 18 differential lines, obviously for timing purposes it is desirable to have low skew between each channel. For these types of applications a high speed bipolar process like the advanced low power Schottky would be required.

A key requirement across most application areas is low power consumption, particularly with the emergence of battery backed or operated equipment's. This requires a low power technology, for example CMOS. However although fine for controller applications, CMOS is not generally suitable for line drive / receive functions, here a more robust technology is needed, for example, a bipolar or merged technology like Texas Instruments' LinBiCMOS (combination of analogue bipolar and analogue CMOS).

Due to the increasing use of differential systems, particularly in electrically hostile environments, increased common mode voltage ranges and low susceptibility to ESD (Electro-Static Discharge) damage is required. Furthermore, extended temperature ranges are required particularly in automotive applications where the line drive/receive functions may be located under the car bonnet (hood). All new devices in Texas Instruments' range of line drivers and receivers contain temperature range options for both commercial, 0° C to 70°C and industrial, -40°C to 85°C. Some devices like the SN65076 have been designed especially for automotive applications by offering a -40 0°C to 105°C temperature range.

One final demand made by all types of equipment is for increased integration. Designers are requiring increased functionality from semiconductor chips and, perhaps an even more importantly require that these chips be less expensive than the solution(s) they replace.

4.3.1. Differential Line Considerations

A differential communication system requires the use of two 'signal carrying' wires between driver and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the *difference* in voltage between the two wires. The absolute value of the dc common mode voltage of the two wires is not important. In practice, drivers and receivers have a finite common mode voltage range within which they can operate.

The use of a differential communications interface allows data transmission at high rates and over long distances to be accomplished. This is because effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output voltage to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

4.3.2. Transmission Line Considerations and Effects

Before design of a digital data link can take place application constraints and an understanding of the signal's characteristics must be understood. More specifically, a method of identifying the class of data link, and any special design techniques required must be made.

A digital data link can be classed in two modes;

i) A transmission line (distributed parameter model)

ii) Short wire (lumped parameter model).

A distributed parameter model considers the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wave front at any point as it travels along the line.

The transmission line will always consist of two conductors, with the current flowing in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The type of cable used will provide the limit to the actual speed.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the driver's output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the driver terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the rise time , t_r, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from driver to receiver and back to driver, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd}, to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of drivers and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

In the case of the lumped parameter model, the line tends to represent a pure fixed load to the driver device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a driver device that can supply a finite amount of current to the line.

4.3.3. Line Termination

It is generally good design practice to terminate the ends of lines which are classified as transmission lines. Here the golden rule is to match the impedance from the source of the driver to the characteristic impedance of the cable, and from the cable to the characteristic impedance of the receiver. If there is an impedance discontinuity at any junction, then the signal will be reflected from the mismatch. This will lead to signal distortion which in turn leads to either a falsely triggered receiver or excessive propagation delay. Calculation of a suitable value for this termination value will be dealt with later in this section whilst a more detailed discussion can be found in the transmission line fundamentals section at the front of the data transmission section.

4.4. Data Rate and Line Length Limitations

Most application areas will demand some kind of compromise between the line length used and the data rate required, particularly if distortion in its many guises is to be avoided. A first, all important, step in understanding what compromises are necessary is to recognise the various forms of distortion and why they occur.

No transmission line is perfect, even by sending current down the line some voltage drop will occur due to the resistive nature of the line, this in its most simplistic form is distortion. This is compounded when longer line lengths are used where the attenuation from source to destination can cause quite severe distortion. This places a limit on the line length even at low data rates. A typical cable of 24 SWG can have a series resistance of 80 Ω per km, and so the line length will be limited to the order of 1200m (series resistance equals the line's characteristic impedance).

Other Effects

Other effects acting upon the transmission line are due to phase distortion introduced on the driver's transition edges. The high speed edges, necessary for high speed systems, have a high frequency harmonic content. The inductive and capacitive (and resistive) nature of the line introduces delay and distortion into these harmonics. This in turn reduces the clarity of the signal being sent down the line, thus increasing the probability of error.

This effect is normally measured using eye patterns which measure the jitter and distortion in the signal being sent down the line. It is this effect that causes the predominant reduction in data rate as the line length increases. Another limitation can be caused by incorrect termination of the line, causing reflections. These reflections can cause errors due to loss of timing information.

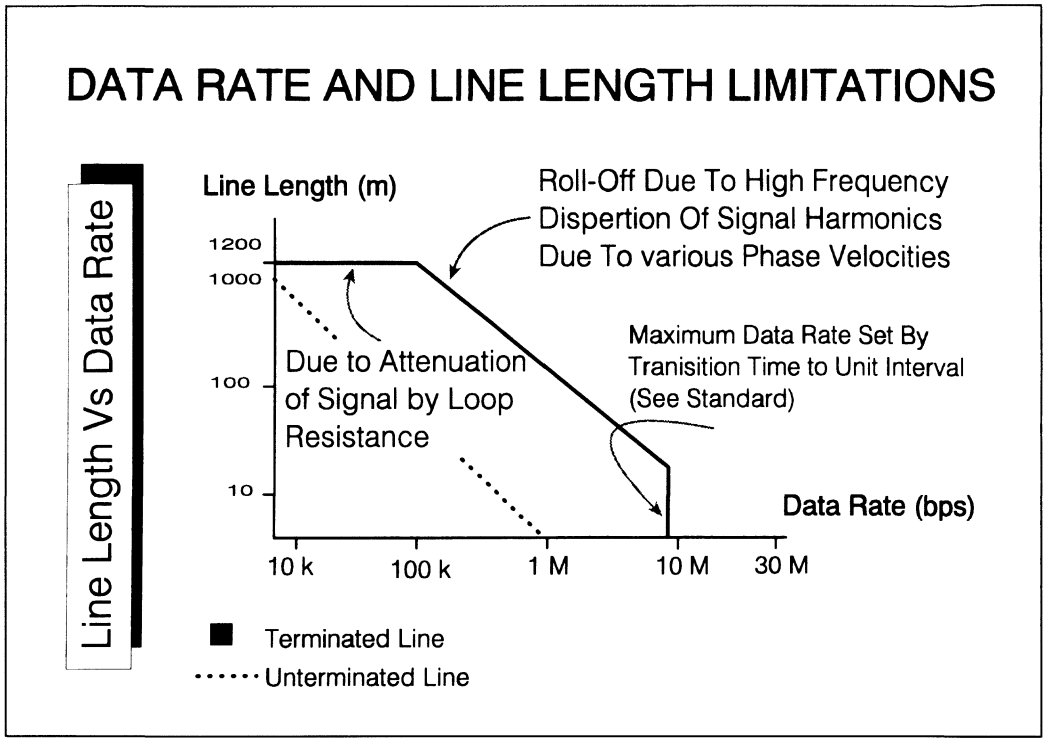


Figure 4.45 - Data Rate and Line Length Limitations

In conclusion, distortion and thus data integrity is a function of signal rise time and line attenuation. Signal rise time and attenuation are often quoted in manufactures data, and can be used to determine the line distortion.

4.5. RS-422/RS-485 Data Rate Definition

Another limitation of system performance are the speed limitations of the line driving elements themselves. No device, no matter what technology used, will have zero propagation delays and transition times. The trick is to ensure that any delay introduced by these devices is insignificant in comparison to the line propagation delay. To ensure the device does not introduce distortion, i.e. to maintain signal shape, it is good design practice to set a ratio between the unit interval, t_b, and the transition rise time, t_T. This limitation is often specified in the standard being used. For RS-422-A the ratio of t_T to t_b is 1:10, and for RS-485 1:3.

Note these calculations only give an indication of the drivers data rate capability, obviously the receivers propagation delay needs to be considered for the system data rate. Furthermore in multi channel systems the slowest driver and receiver in the system set the overall system data rate (see the differential ac specifications section following)

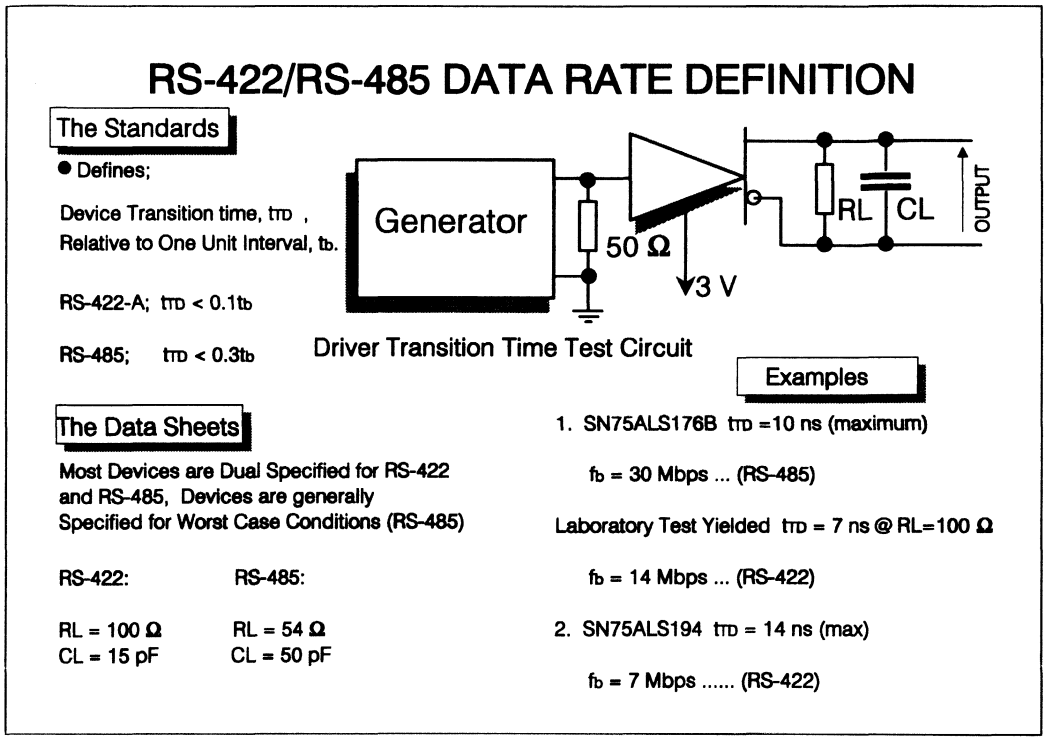


Figure 4.46 - RS-422/RS-485 Data Rate Definition

Many devices within the Texas Instruments' range are specified for both RS-422 and RS-485 operation. The differing specifications of relating t_T to t_b between the standards makes an understanding of data rate capability for RS-422 operation difficult to ascertain, since these devices are tested to the worst case conditions of the RS-485 specification. That is, the driver output is driven into a resistive load of 54 Ω in parallel with a capacitive load of 50 pF.

An example of such a device is the SN75ALS176 which can be used for both RS-422 or RS-485.

Examples

1. **SN75ALS176B** has a differential-output transition time t_T of 10 ns(Max). Therefore; $t_b = 3.33 \times 10 \times 10^{-9} = 33.3$ ns giving a minimum theoretical frequency of **30 Mbps.**

As the data sheet specifies a minimum t_T = 5 ns the maximum theoretical data rate could be as high as 60 Mbps.

Using the RS-422 data rate test for this devices does not give a clear picture as the standard requires a lighter load to be applied. However, laboratory test using the RS-422 load gives a t_T for the ALS176 of 7 ns (RS-485 load = 14 ns) indicating a RS-422 data rate of 14 Mbps.

2. **SN75ALS194** has a differential-output transition time t_T = 14 ns(Max). Since this device is specified solely for RS-422 we can clearly calculate the minimum theoretical data rate.

Therefore; $t_b = 10 \times 14 \times 10^{-9} = 10 \times 14 \times 10^{-9}$ giving a minimum theoretical frequency of **7 Mbps.**

Again a more aggressive data rate could be achieved if the typical specified value for t_T = 8 ns was used. Giving a typical frequency of 12.5 Mbps.

4.6. Differential AC specifications

For multi channel systems, like SCSI, consideration of the drivers differential transition time is not sufficient to determine the systems data rate capability. More specifically the slowest driver/receiver within the system will usually set the limit.

Although much detail is contained within multi channel standards, such as the ANSI SCSI standard, concerning most aspects of the electrical interface, ac considerations are not. Many of these standards define the overall bus timing requirements but the budgeting of timing error contributions is left to the system designer.

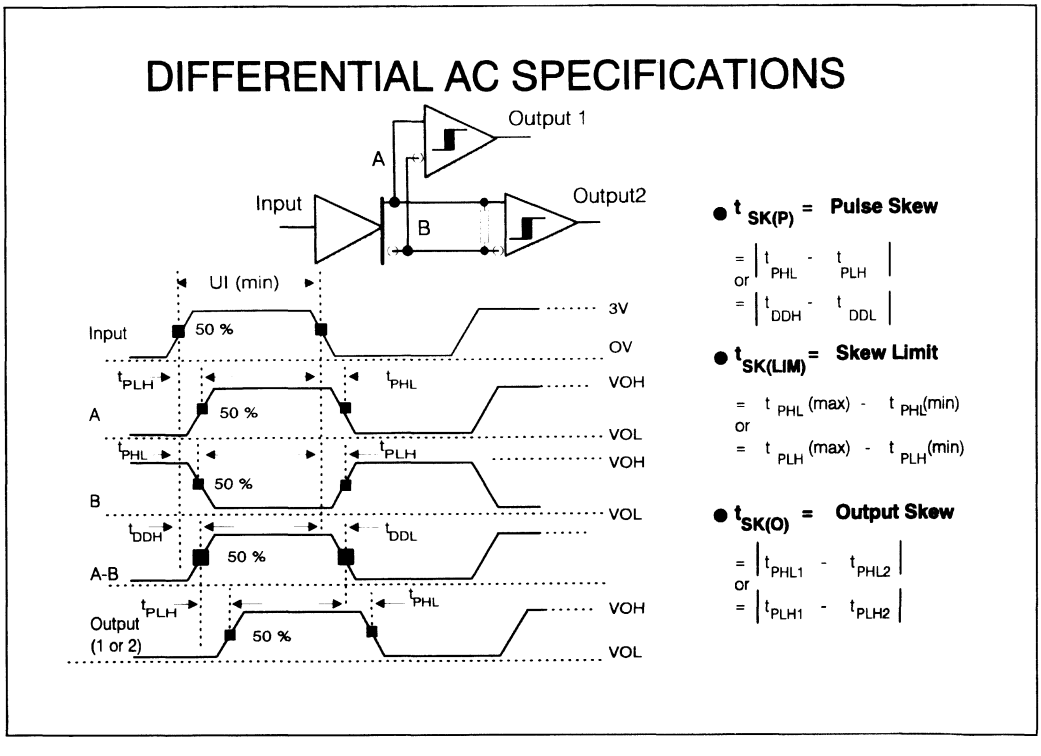


Figure 4.47 - Differential AC specifications

When driving the line at high speeds the effects of the driver and receiver on the system become more apparent. The magnitude of the driver and receiver propagation delays relative to the unit interval increase, causing asymmetries in the edges. These asymmetries have three main effects;

i. **Decreased data rate capability**

ii. **Decreased noise immunity**

iii. **Increased risk of noise radiation**

Figure 4.47 shows how these delays manifest themselves in a differential data transmission scheme.

4.6.1. A Discussion of Skew

There are many catagories of delay, termed skew, in a differential line system. This understanding is further complicated when you consider that a driver is really a single ended input to differential output converter, while the receiver is a differential input to single ended converter.

Skew measurements are either **propagational,** single ended (t_P), or **differential, single ended to differential** (t_{DD}).

Pulse Skew; $t_{SK(P)}$

Propagational Pulse skew ($t_{SK(P)}$) is measured between the 50% level of the input pulse and the 50% level of the driver single ended output pulse (either A or B in the figure). Differential pulse skew is measured between the 50% level of the input pulse and the 50% level of the driver differential output pulse (A-B).

In the ideal situation where $t_{PHL} = t_{PLH}$ or $t_{DDH} = t_{DDL}$,, pulse skew effectively displaces the signal on the line in time, and no signal distortion should occur - although these delays will need to be allowed for when synchronising data in multi channel systems. However if the rise and fall time delays are not the equal then the resultant differential signal may become distorted. Typically this distortion will cause the differential signal to flattern out around the receivers transition region, i.e. at the common mode voltage of the line. As a result the system will have a lower noise immunity and increased likelihood of RFI radiation.

Propagation pulse skew or differential pulse skew may be specified for either drivers or receivers. Normally propagation pulse skew is specified in older driver data sheets whilst differential pulse skew, a more meaningful measurement, is specified on more modern devices. For example Texas Instruments' SN75ALS176B, best in the industry, has a pulse skew of 2 ns. .

Although the figure shows differential pulse skew measurement, production testing is usually carried out as a propagation skew measurement. This is due to the difficulties in generating a true differential signal. This parameter is tested with one input tied at a reference voltage and the other toggled, giving a single ended propagation delay.

Skew Limit; $t_{SK(LIM)}$

Skew limit is the greater of either the difference between the maximum and minimum specified values of t_{PLH} (or t_{DDL}) or the difference between the maximum and minimum specified values of t_{PHL} (or t_{DDL}). In effect this is the maximum range that the driver or receiver delay time will vary over temperature, V_{CC}, and device-to-device. This is a particularly useful parameter for determining the data rates in multi-channel bus systems, since it sets a limit on signal delays between channel to channel.

Output Skew; $t_{SK(O)}$

This is simply the delay between the t_{PLH} or t_{PHL} receiver output levels within a multi-channel system.

4.7. Defining the Minimum Unit Interval (UImin)

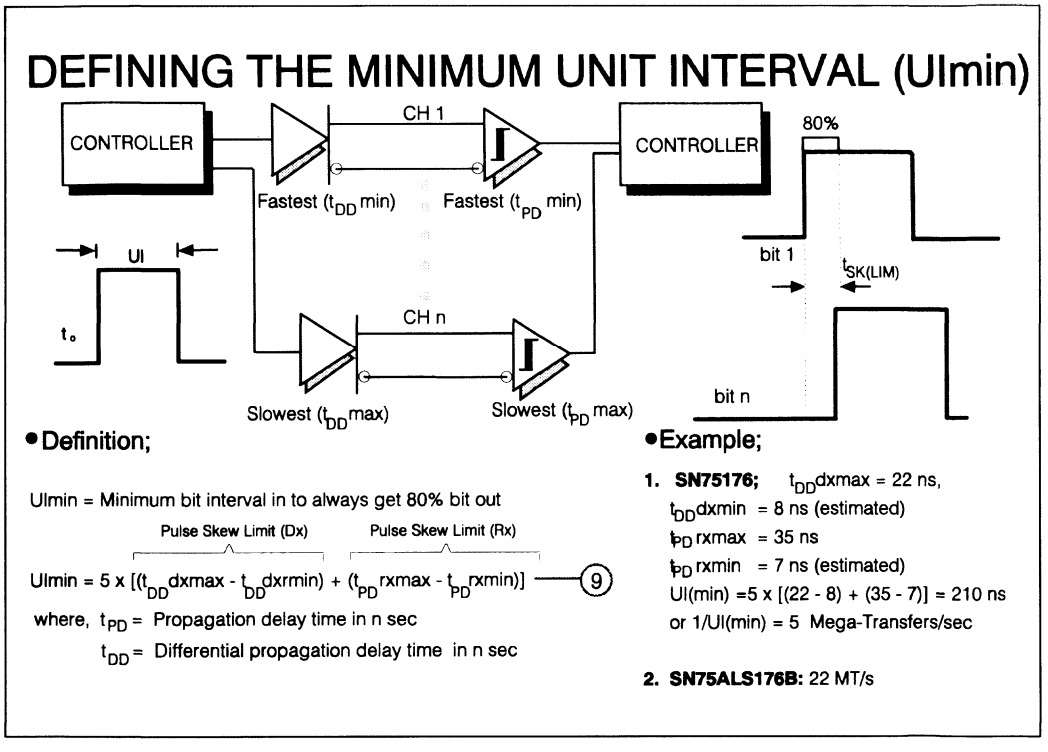


Figure 4.48 - Defining the Minimum Unit Interval (UImin)

Figure 4.48 shows the application of the skew limit test to a multi-channel system in order to calculate the maximum data rate capability, this is shown as equation 9. To maintain synchronisation and signal integrity there must be a minimum overlap between the signals on each channel. As a basic rule the skew limit must be no greater than 20% of the unit interval.

The calculations compare the data rate capability of the low power Schottky SN75176 to the advanced low power Schottky SN75ALS176,

4.8. Fastest Differential Transceiver

Figure 4.49 (uses equation 9) to compare the data rates of various differential devices available from Texas Instruments. The fastest RS-485 compatible differential transceiver available today is the SN75ALS176B.

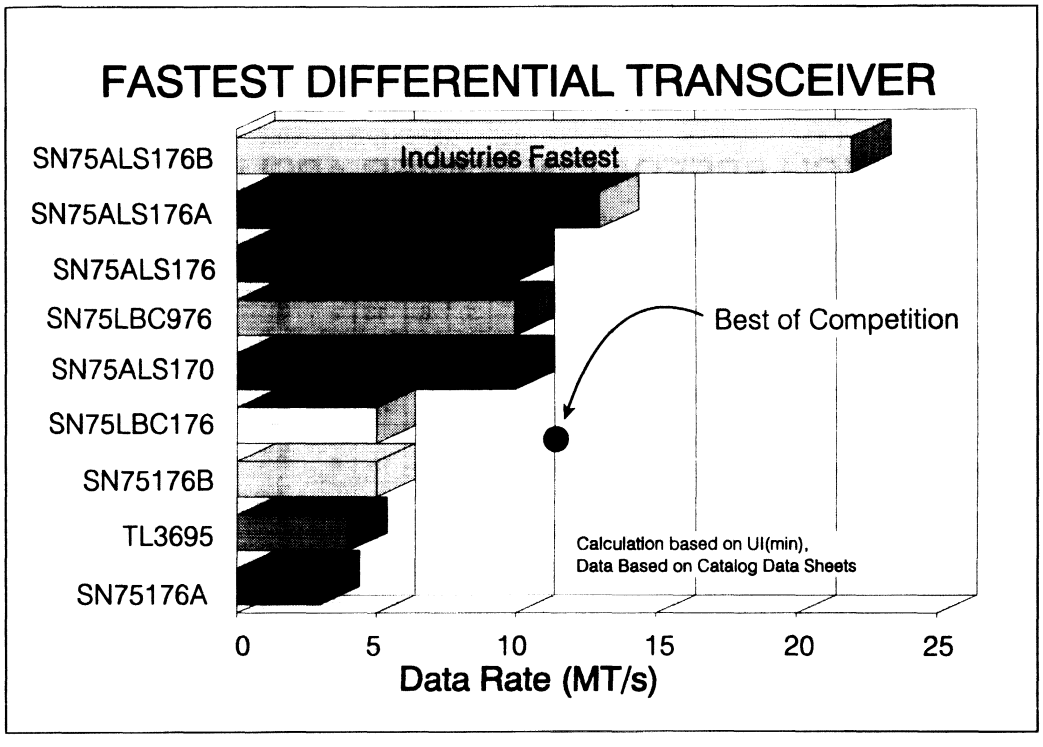


Figure 4.49 - Fastest Differential Transceiver

4.9.SN75ALS For High Speed/Low Power Applications

The SN75ALS176 forms just part of a range of high performance single line driver/receiver options available for RS-422 and RS-485 applications. Some key benefits of this range are discussed in the following text.

The range of devices shown in the figure are all high speed low power monolithic integrated circuits, designed for bi-directional data communication on multi-point bus transmission lines. The SN65ALS176, SN75ALS176 series and TL3695 are single differential transceivers, while the SN65ALS180 and SN75ALS180 are a single differential driver/receiver pair.

All devices are designed for balanced transmission lines and meet EIA standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

The SN65ALS176, SN75ALS176 series and TL3695 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port

features a wide positive and negative common-mode voltage range making the device ideal for party line applications. All devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging.

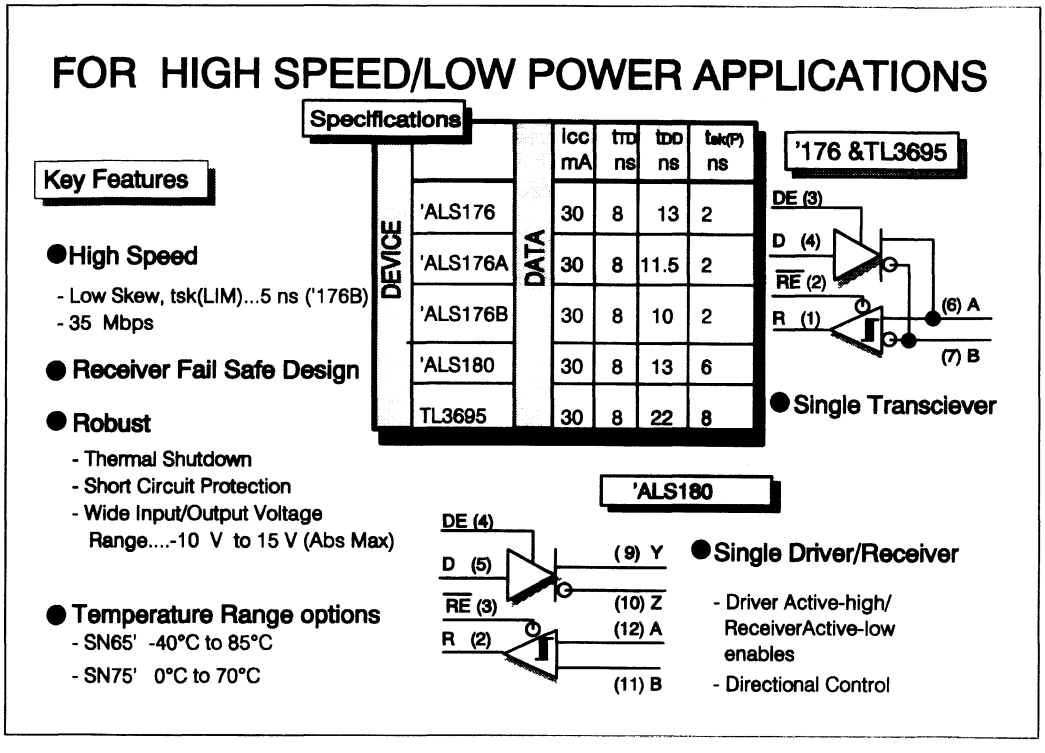


Figure 4.50 - For High Speed/Low Power Applications

The SN75ALS180 contains many of the same features listed above. However, the driver outputs and receiver inputs are not internally connected together but are brought outside the chip, offering a separate driver and receiver function. For this reason the SN65ALS180 and SN75ALS180 are housed in a 14-pin dual-in-line plastic and 14-pin small outline plastic packages. This arrangement makes the SN75ALS180 ideal for full duplex operation.

4.9.1. Product Differentiation

The SN75ALS176 series allows the designer to select between ac performance levels. The figure shows the maximum propagation delays and skew specification for the range. The SN75ALS176B offers the highest speed performance with a maximum differential output delay time of 10 ns. With a minimum specified value of 5ns the device is capable of data rates in excess of 60 Mbps (as per RS-485 specification).

Perhaps even more importantly, especially for high speed multi-channel applications (for example SCSI), is the low skew value, $t_{sk(LIM)}$. In this instance skew is specified as the difference between the

maximum and minimum differential output delay times, T_{DD}. The SN75ALS176B has a minimum $t_{sk(LIM)}$ value of 5 ns. This value is used to determine the delays in signals between channels in the system. The pulse skew, $t_{sk(P)}$, is specified as a minimum value of 2 ns (see previous discussion of skew).

The TL3695 provides the same functionality as the 'ALS76 series of devices, but is aimed at lower performance lower cost systems.

4.10. Low Skew Reduces EMI

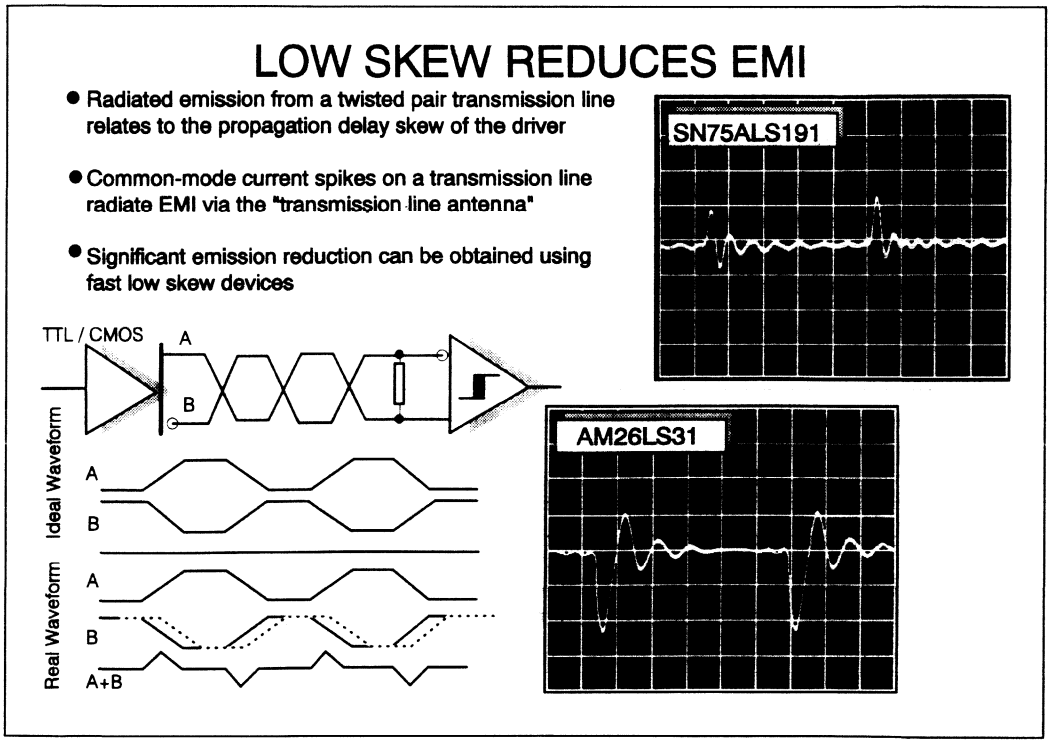


Figure 4.51 - Low Skew Reduces EMI

Further justification for low skew designs is set out in the following paragraphs;

4.10.1. EMI Related to Differential Transmission Lines

Radiated emissions from electronic systems has been receiving more attention as mutual disturbances between electronic equipment increase and the subsequent need for EMC regulations becomes more apparent. This is compounded by the increased use of high clock rates and high currents which generate high frequency EMI. Applications placed on printed circuit boards are normally enclosed in a confined space making the problem easier to solve, but when transmitting data signals to the outside world through cables, increasing the total radiated emission by the system is difficult to avoid.

In large computer systems, Inter-unit cables within the system have been found to be responsible for much of the radiated emission. Further studies have revealed that the noise itself is a function of common mode current spikes, brought about by the skew between the outputs of clocked differential drivers. Significant improvements in system-wide emissions were seen in practice after replacing high skew driver devices with others those which had less skew.

The effect seen is not only related to large computer systems but is saleable to all systems using differential transmission lines. Differential drivers and receiver are designed to operate under conditions with high common mode signals. Low frequency common mode signals usually cause no problems, but high frequency common mode spikes cause EMI and in systems with inter-unit cabling an antenna is readily available increasing the radiated emission. Clearly, twisted pair cables used to interconnect boards within the same cabinet, or to establish data transmission between various equipment, using for example the popular standards RS-422-A or RS-485, are likely to radiate EMI if the driver's complementary outputs are not exactly symmetrical. This is true for the single differential line in an industrial system as well as for the many parallel differential lines used in a SCSI interface cable.

Low Skew Devices Reduce EMI

Ideally, a differential driver should not generate common mode signals due to the nature of the differential output and the twisted cable cancelling the common-mode currents but in practice, small differences between the complementary outputs occur which produce fast common mode pulses on the line.

The skew specification, specified as the propagation delay difference from the input of the differential driver to the driver's respective inverting and non-inverting outputs is a good measure for how much or how little radiation that can be expected from high frequency common mode signals during switching. However, a low skew specification on its own does not guarantee negligible common mode signals as the signals can still be non symmetrical due to different rising and falling wave forms. In such cases Significant current spikes can be measured on the line.

Use Fast Devices Even in Low Data Rate System

Even in systems where low data rates are used, EMI can still cause problems with EMC regulations. These problems are best solved by employing high speed devices usually having a significant lower skew than slower drivers.

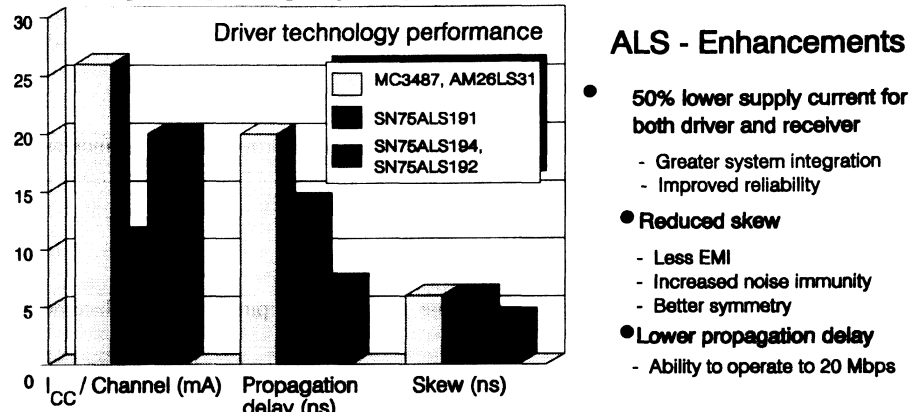
Consequently, previous low power schottky (LS) designs like, AM26LS31 or SN75176 will in general radiate more emissions than newer Advanced Low Power designs like SN75ALS192 and SN75ALS176 or even the new BiCMOS designs like AM26C31 and SN75LBC176. A measurement was made to demonstrate this effect comparing AM26LS31 with SN75ALS192. Evidently, the negligible common mode signals resulting from switching the SN75ALS192 are significantly smaller than the clearly visible common mode current spikes produced by the AM26LS31.

4.11. SN75ALS19x Series For RS-422

4.11.1. Product Description

The well proven SN75ALS19x series of drivers and receivers for RS-422-A represents some of the best speed versus power consumption alternatives in the industry today for reliable balanced line

transmission over short as well as long distances. The series has found wide use in telecommunication as well as in computer applications.



DRIVERS	TYPE	IND. STD	REPLACING
SN75ALS192	QUAD	RS-422-A	AM26LS31
SN75ALS194	QUAD	RS-422-A	MC3487
SN75ALS191	DUAL 8-PIN	RS-422-A	UA9638

RECEIVERS	TYPE	IND. STD	REPLACING
SN75ALS193	QUAD	RS-422-A	AM26LS32A
SN75ALS195	QUAD	RS-423-A	MC3486
SN75ALS197	QUAD	V.10 V.11	AM26LS32A
SN75ALS199	QUAD	X.25 X.27	MC3486

Figure 4.52 - SN75ALS19x Series For RS-422

ALS Technology Advantages

All ALS products employ Advanced Low-Power Schottky or Impact™ processes. These have been derived from the digital processes and trimmed for linear applications requiring wide common mode voltage operation, tough protection and accurate receiver input threshold voltages. ALS technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs - in short; speed without the usual power penalties. Standby current is typically reduced by 50%

although switching speed has gone up by more than 30% compared with previous LS (Low Power Schottky) parts.

50% Lower Supply Current

The significant reduction in power consumption allows for a higher board packaging density and hence greater system integration without increasing temperature due to power dissipation. In addition, a lower operational temperature improves system reliability.

Lower power consumption also permits devices to operate in an extended temperature range (-55°C to

+125°C) with fewer constraints.

30% Improvement in Data Throughput

Lower propagation delays and reduced skew, combined with lower standby power consumption, allows these devices to operate in excess of 20Mbps. For example; a SN75ALS192 quad driver is capable of transmitting data at 20Mbps (50% duty cycle) while only dissipating the same power as an AM26LS31A in standby mode. The maximum achievable data rate is usually determined by maximum power dissipation at the maximum operating temperature. Reference should be made to the data sheet's Dissipation Rating Table.

Reduced Skew

The SN75ALS19x series has been designed with minimum skew to improve symmetry, increase noise immunity and radiate less EMI (Electromagnetic Interference) caused by non-common mode currents in the transmission cable. The high-speed dual driver, SN75ALS191 in an 8-pin package features a typical differential skew of 1.5ns (4ns maximum).

Products

A wide range of SN75ALS19x products are available as improved pin for pin replacements for industry standard devices.

The main difference between the quadruple drivers, SN75ALS192 and SN75ALS194, is related to their enabling configuration. SN75ALS192 has a common pin enabling all four drivers, whereas independent enabling schemes are possible for each pair of drivers in the SN75ALS194. Similarly, different enabling schemes distinguishes the quadruple receivers, SN75ALS193 and ALS195. The SN75ALS192 and SN75ALS193 form complementary devices as do the SN75ALS194 and SN75ALS195 devices. Using complementary drivers and receivers together should provide optimum performance.

The quadruple receivers, SN75ALS197 and ALS199 have relaxed input sensitivity specifications of ±300mV, compared to ±200mV for SN75ALS193 and ALS195. However, they are available in low cost D (surface mount) or N (DIL) packages and meets CCITT Recommendations V.10, V.11, X.26 and X.27.

4.12. AM26C31/32....Old Name New Benefits

4.12.1. Product Description

Improvements in Power Consumption and Speed

Industry has long been aware of the advantages gained from using the quadruple driver AM26LS31 and the accompanying quadruple receiver AM26LS32 for RS-422 type applications . However the old low power schottky (LS) process is no longer capable of keeping pace with today's demands for high speed and low power. The AM26C31 are AM26C32 are modern upgrades, fabricated using a low power BiCMOS process.

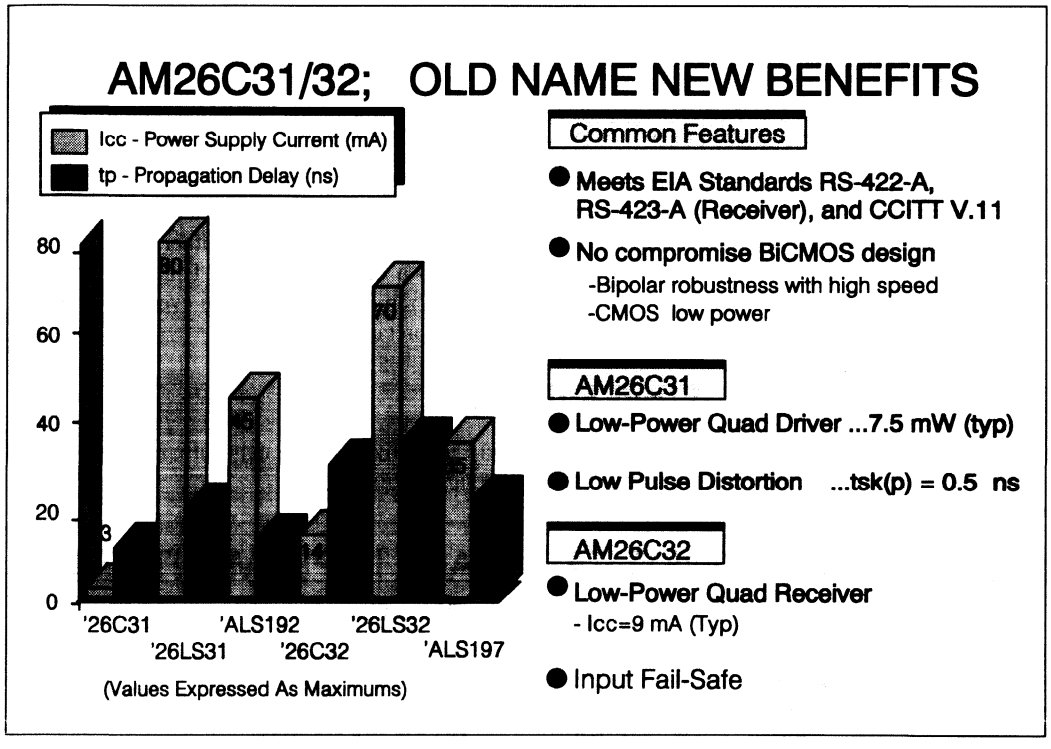


Figure 4.53 - AM26C31/32....Old Name New Benefits

These devices find applications where high speed and low skew are crucial, for example in disk drive and Telecommunication applications. One particular application which would benefit from the low power consumption will be the Central Office Exchange, where due to the shear number of devices used, power consumption becomes a critical issue - especially when the rest of the system is implemented in low power CMOS.

The figure shows some key benefits of these new designs and compares the power consumption and propagation delay against industry standard devices. It can easily be seen that the BiCMOS devices not only exhibit a dramatic reduction in power consumption, from 80 mA to 2 mA, but there is also an improvement in ac performance. The AM26C31 driver has a lower propagation delay than any of the devices shown in the graph.

Description

Both the AM26C31 and AM26C32 have been manufactured using a BiCMOS technology which is a combination of bipolar and CMOS transistors. This process provides the high voltage/current drive of bipolar with the low quiescent power consumption of CMOS. The graphs in the figure show that the power consumption of the AM26C32 receiver is reduced to approximately one-fifth of the standard LS part.

The AM26C31 is a quadruple complementary-output line driver designed to satisfy the requirements of EIA RS-422-A and CCITT recommendation V.11. The three-state outputs have a high-current drive capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable input.

The AM26C32 is a quadruple line receiver for balanced and unbalanced digital data transmission. Conformance to the EIA standards RS-422-A and RS-423-A and CCITT recommendation V.11 is guaranteed. The enable function is common to all receivers and offers a choice of either active-high or active-low inputs. Three-state outputs permit connection to a digital data bus. Fail safe circuitry design on the receiver input side ensures that the outputs will remain in a high state even if the inputs are left open. This reduces the chances of incorrect data interpretation.

4.13. RS-485 Hard Wired Fail Safe

The feature of fail safe protection is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

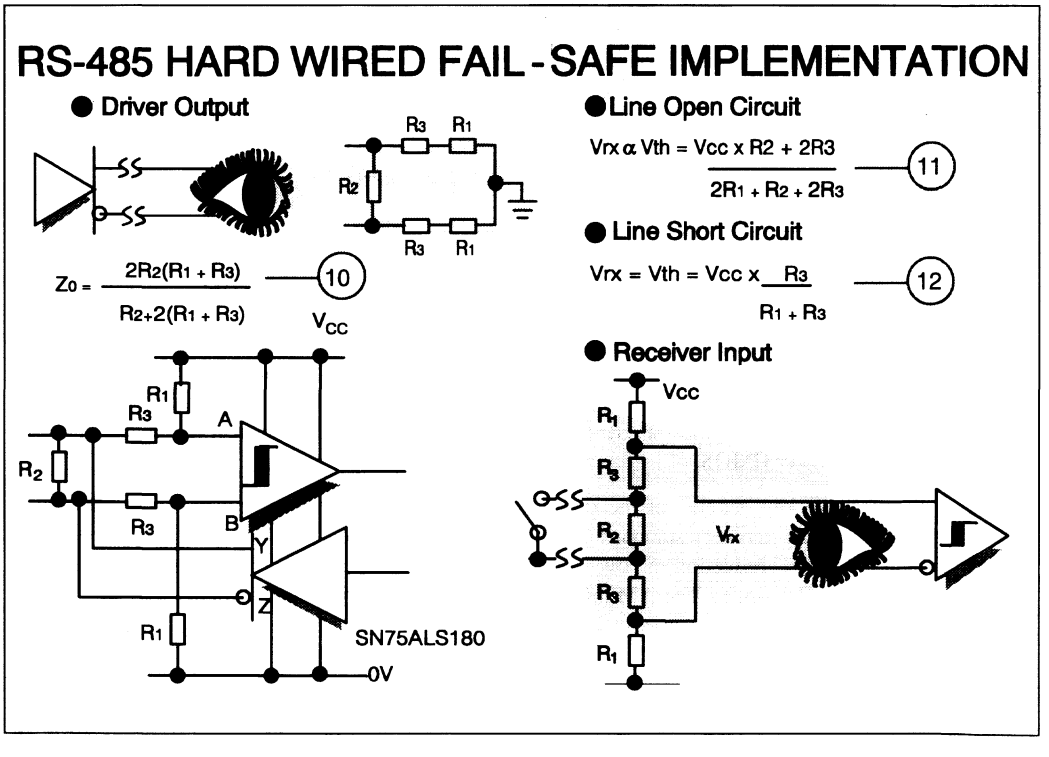


Figure 4.54 - RS-485 Hard Wired Fail Safe

4.13.1. The need For Fail Safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or a low logic state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe**. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method and are discussed in more detail following this section. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input whether or not the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination network when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of open line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting input of the receiver. These resistors are normally in the range of 100kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few milli volts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. In effect, to use these internal resistors no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an ac. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedance's. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance, Z_O , produces a potential divider between $2R_1$ and Z_O. The voltage formed across the line, V_{OC}, equals

$$V_{oc} = V_{cc} * \frac{Z_o}{2R_1 + Z_o}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{oc} to be greater than 200mV . From this the relationship of R_1 to Z_o can be derived:-

$$R_1 = Z_o * \frac{1}{2} * \frac{V_{cc} - V_{oc}}{V_{oc}}$$

With V_{cc} = 5V, V_{oc} = 200mV and Z_o = 100Ω, yields R_1 = 1.2kΩ.

Biasing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers it is not possible to provide shorted line fail safe configurations, this is a result of the driver and receiver sharing the same I.C. pins. Hence for devices like the SN75ALS176 this open line configuration the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in the figure, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The ALS180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{cc} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 and 422A applications the standard specifies V_{rx} to be greater than 200mV. So $V_{rx} = V_{th}$ = 200mV. Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \quad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = \tfrac{1}{2}R_2 \times [\{(V_{cc} - \alpha\ V_{th})(V_{cc} - V_{th})\}/\{(\alpha - 1)\ V_{th}\ V_{cc}\}]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_o, therefore

$$Z_o = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \quad \textbf{(c)}$$

Combining equations **(a), (b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = \tfrac{1}{2}Z_o \times \frac{(V_{cc} - V_{th})^2}{(\alpha - 1)\ V_{th}\ V_{cc}}$$

$$R_2 = Z_o \times \frac{V_{cc} - V_{th}}{V_{cc} - \alpha V_{th}}$$

$$R_3 = \tfrac{1}{2}Z_o \times \frac{V_{cc} - V_{th}}{\alpha - 1\ V_{th}}$$

In this application assuming the supply voltage is 4.5 V and Vth = 200 mV with an a value α of 1.5 and driving a line with characteristic impedance of 120 Ω yields the following values:-

R_1 = 2.2k Ω

R_2 = 120 Ω

R_3 = 110 Ω

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers

are the same, all R_1 resistors are the same, and that all R_3 resistors are the same. Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 18k Ω.

4.14. Use of Protocols- Synchronous Serial Communication

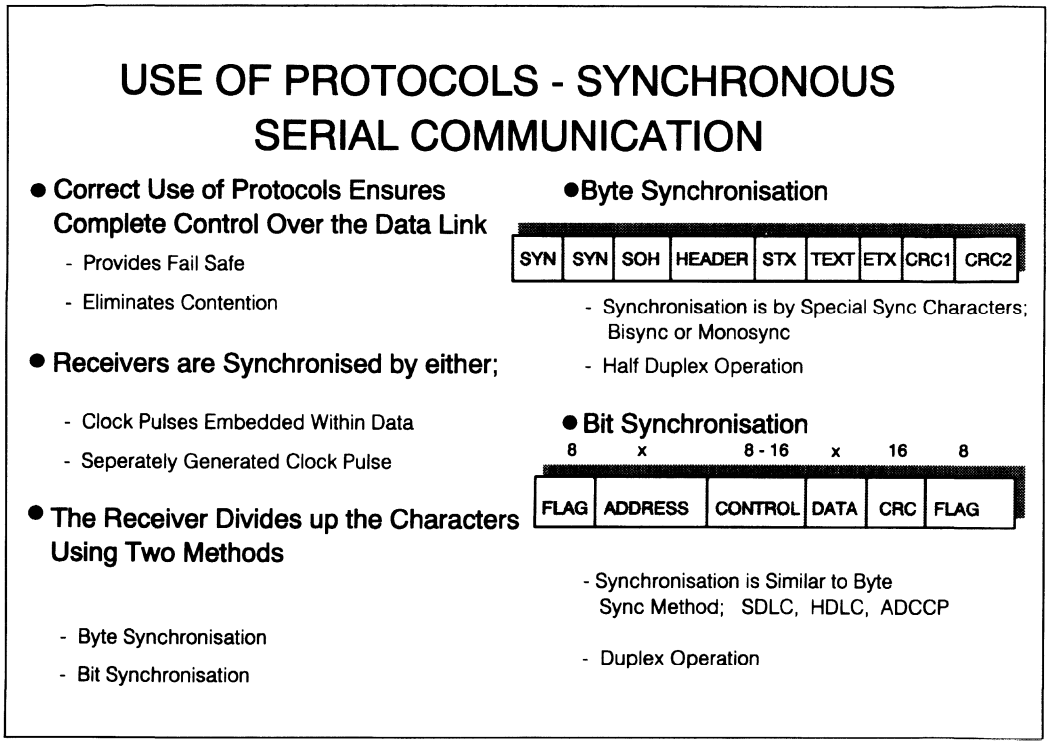


Figure 4.55 - Use of Protocols- Synchronous Serial Communication

The use of line terminations to effect a fail safe is not a recommended practice. The recommended practice is to use software protocols. Protocols come in many forms (two of which are explained below) and provide a set of rules which define the meaning and order in which data should be sent. In particular, they can be used to provide a fail safe feature and be used to avoid contention. Contention occurs when several drivers try to address the link at the same time. This can lead to high current sinking or souring leading to excessive thermal dissipation in the drivers. Fail safe is ensured by allowing the receiving station to respond to valid data only., This is achieved by sending a preamble before each data packet . The preamble consists of a pre-determined pattern of bits, which signals to the receiver that valid data is about to follow. Anything other than this preamble should be ignored by the receiver.

4.14.1. Party Line Protocol Formats

Party line applications use either half duplex or full duplex transmission. Half duplex's transmission mode is where two terminals (a driver and receiver) can communicate with each other bi-directionally over the same link, but they cannot transmit simultaneously. A party line transmission line format can be achieved using half duplex by multiplexing between a number of driver/receiver pairs. Full duplex communications involves the simultaneous, two way flow of data from driver / receiver pairs.

A communication line used in a multiplexed operation such as the half duplex party line system reduces wiring costs when compared to the simplex operation (simplex one driver for one receiver). Only one line is needed to implement the communication system, though control of the multiplexing does require complex protocol or handshaking circuits.

A typical (simplified) protocol sequence would contain the following elements;

i) **Driver requests access to communication link (bus)**

ii) **Link controller responds to request and gives go ahead when bus is free**

iii) **Driver gains bus master ship and sends data which is preceded by a destination code**

iv) **Receiver sends an acknowledgement**

v) **Driver receives confirmation and releases the bus**

4.14.2. Synchronisation

Some form of synchronisation is necessary for the receiver to determine the start and finish of the received bits. Two schemes, with many variations, are adopted; **Asynchronous** and **synchronous**. Asynchronisation, or start-stop bit communication, uses a system where characters are sent one at a time, without necessarily having any fixed time relationship between each other. In such a case the driver sends start bits followed by the information field, followed by one or more stop bits. This informs the receiver that information data will follow the start bit and will end prior to the stop bit. The data is usually broken into small groups of 8-bits, one byte, which is proceeded with a start bit and concluded with a stop bit. This is one of the schemes employed by EIA-232.

Synchronous transmission is used to transmit complete blocks of data at one time. In synchronous transmission the duration of each bit is the same. With all characters being the same length the receiver only has to identify the first character and then clock the others in at a predetermine rate.

Serial synchronous communication uses a similar scheme and either embeds the timing information in the data or provides a separate clock signal. However the bit stream still has to be divided up into the individual characters. There are two main methods of achieving character synchronisation: **Byte synchronisation** and **bit synchronisation.**

Byte synchronisation, one of the first synchronous methods to be introduced is best known by IBM's bisync and monosync . Synchronisation is achieved by using special **SYNC** characters which are transmitted in between data packets. The receiver continually monitors this transmission and uses it to synchronise itself . After receiving one (monosync) or two (bisync) sync pulses the receiver is said two be in the synchronised mode and is ready to receive data. Synchronisation is ensured by re-sending

the sync bits every few hundred characters, for this reason data is grouped together in frames or packets which start with sync characters. Each frame is 8-bits long

The bisync protocol also defines a structure for a frame that includes control information and error checking capability. The figure shows the basic frame structure with the sync characters followed by the header field. **SOH** identifies the beginning of the header block. The *header* field is user defined and generally contains control specific information such as rest data link, message numbering priority ..etc. Start of text, **STX**, identifies the end of the header field and defines the beginning of the text field. The text or data field contains application specific information which must be sent to the application controller intact. **ETX** signals, end of text, and CRC1 and CRC2 are used as cyclic redundancy check bits. Notice that STX, ETX etc.. are the standard ASCII control codes. Bysync is essentially a half duplex system because each frame requires an acknowledge from the receiver before commencing with the next frame. Obviously sending acknowledging codes back and forth reduces the data rate, and to overcome this bit synchronisation was developed.

SDLC (synchronous data link control), again made popular through IBM, was one of the first bit synchronisation protocols available. The CCITT also adapted this standard for their high level data link (HDLC) protocol. Both are very similar to the CCITT X25 layer 2 packet switching local area networking standard. Initially bit sync looks very similar to byte sync , i.e. during data null periods sync pulses are sent over the link to synchronise the receiver and driver. However after the sync period the data may be grouped in any number of bits. Byte-sync systems are restricted to 8-bit packets. In SDLC and HDLC, messages are formatted into frames with each frame being divided into fields. The start flag is the sync data while the address field contains the destination address to select the required receivers. The control field can be configured as either an information field or supervisory field. The information field, which is the usual format, contains status information on the number of frames sent or received. Data field follows and contains application specific code. The supervisory or management frame is used to acknowledge successful receipt of data. CRC is used for error checking and flag is the next sync signal.

Party Line Considerations

The following points should be considered for correct party line operation;

i. Each driver must have a three-state logic capability, two logic states and a high impedance mode. Also at any one instance it is likely that all drivers could be in the high impedance state, thus leaving the bus floating. A receiver should be able to detect this situation and protect against any spurious information - fail safe design.

ii. Receivers may oscillate if left unconnected, which might affect other used receivers in the same package. Therefore it is recommended that all unused receiver inputs should be tied to defined logic states.

4.15. Input Protection In Noisy Environments

In addition to fail safe protection, applications often require protection against excessive noise voltages.

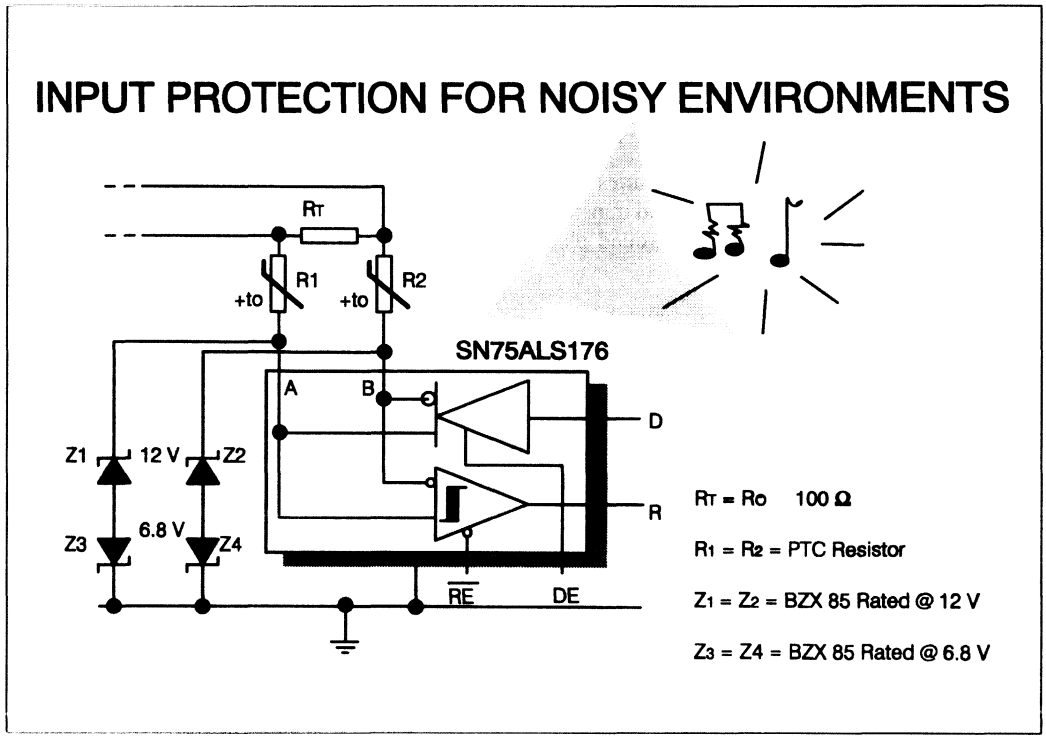


Figure 4.56 - Input Protection In Noisy Environments

Often when sending data over long distances or in electrically hostile environments, i.e. factory automation, the noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 is insufficient. This figure shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

4.16. Calculation of Termination Resistance

The previous examples show the use of terminating resistors, the following text explains how to calculate this value..

To give better performance the transmission line needs to be terminated by a resistor of a value close to its characteristic impedance. One question that immediately arises is the value of terminating

resistance required if the line is loaded by other receivers. More specifically, does the receiver's input impedance have any effect?, especially when many receivers may grouped together at the far end of the line. The following text sets out to prove that for the majority of applications the loading effect of receiver stations can be ignored and as a rule of thumb (working approximation) the value of R_T should equal the characteristic impedance of the line.

In fact, the characteristic impedance varies very little with respect to the physical dimension of the cable. For example a wire over-ground transmission line with a wire diameter equal to the diameter of an electron and a height above the ground plane of 500,000Tm (50 light years) has a characteristic impedance, Z_O, of 300 Ω.

Each input of the receivers has a nominal input impedance of 18 kΩ feeding into a diode-transistor-resistor biasing network, this is equivalent to an 18 kΩ input resistor tied to a common mode voltage source of 2.4 V. -It is this configuration which provides the large common range of the receiver required for RS-485 systems.

Due to the fact that the each input is biased to 2.4V, the normal common-mode voltage of balanced RS-485 systems, the 18k Ω resistors on the inputs can be taken as being in series across the input of each individual receiver.

If thirty such receivers are placed close together at the end of the line, they will tend to react as thirty 36 kΩ resistors in parallel with the termination resistor. This overall effective resistance will need to be close to the characteristic impedance of the line.

The effective parallel receiver resistance, R_P, will therefore be equivalent to;

$$R_p = 36 \times 10^3 / 30 = 1200\ \Omega .$$

While the termination resistor, R_T, used will be equal to;

$$R_T = R_O / [1 - R_O/R_P] .$$

Thus for a line with a characteristic impedance of 100 Ω, the termination resistor R_T should be:

$$R_T = 100 / [1 - 100/1200] = 110\ \Omega$$

Since this calculated value is within 10% of the line characteristic impedance the value chosen for the line termination resistor, R_T, will normally be equal to the characteristic impedance, Z_O.

4.17. Methods of Connection

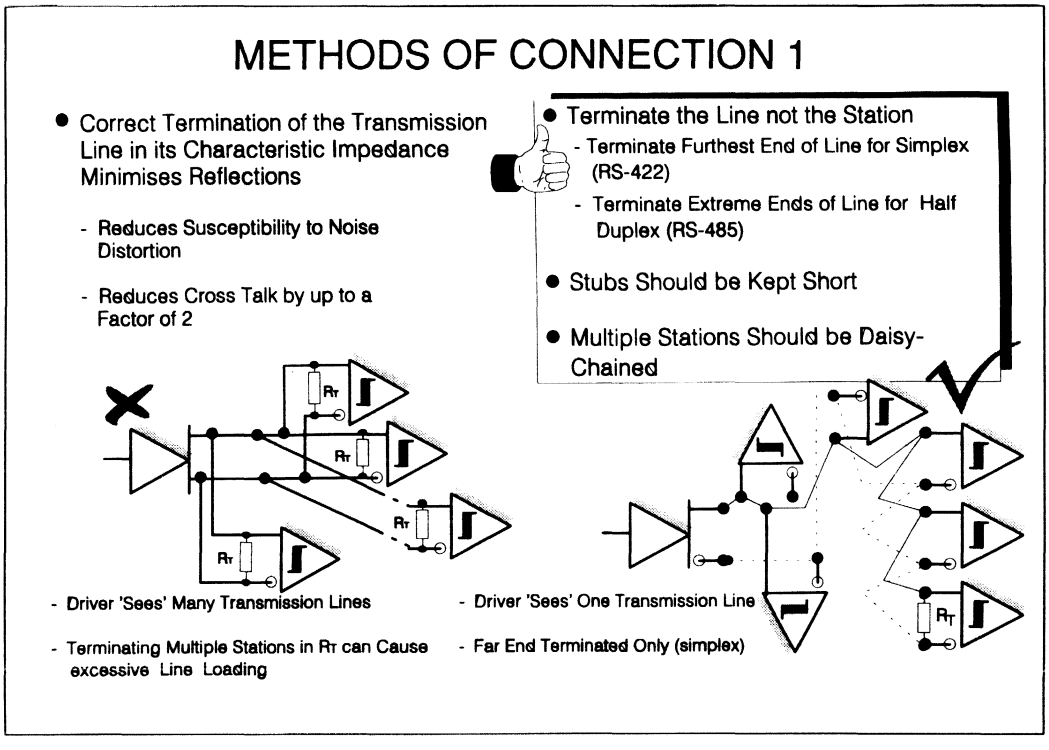


Figure 4.57 - Methods of Connection 1

As well as line termination the way in which stations are connected to the line needs careful consideration. Furthermore the position of the line termination resistor and device positioning must be considered. There are two basic methods of connection;

i. The star connection

ii. The daisy chain connection

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with

only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

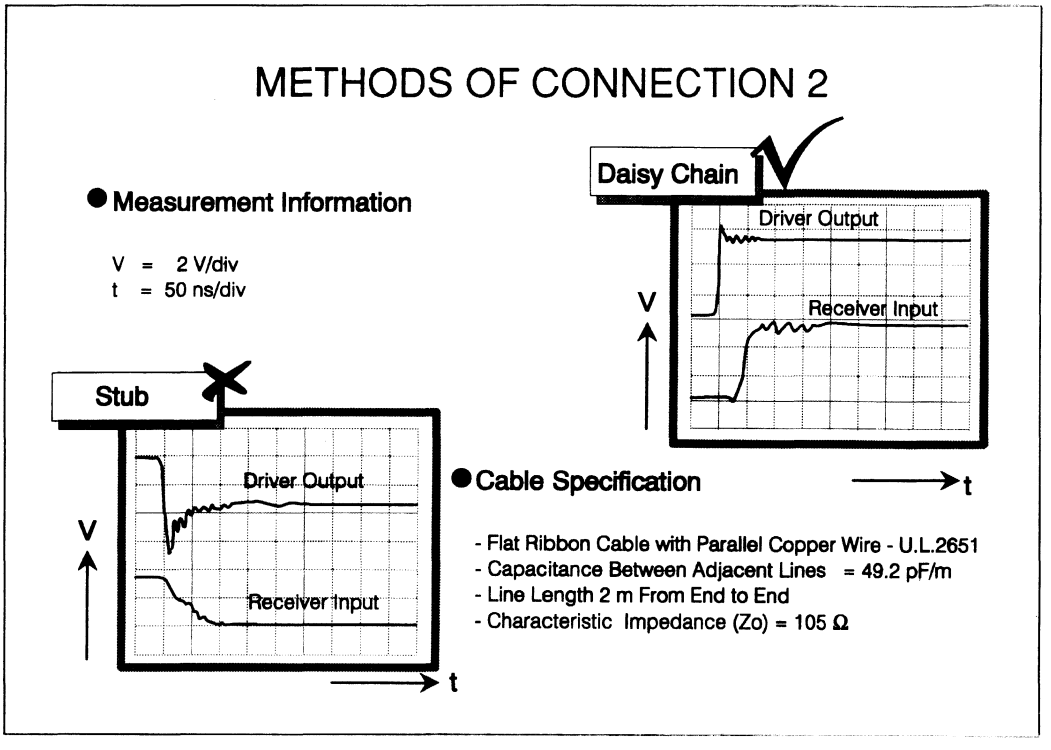


Figure 4.58 - Methods Of Connection 2

The figure shown further confirms the need to keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

4.18. Calculation of Stub Length

In the earlier section a rule of thumb was developed which stated that if signal distortion is to be avoided, all connections to the main line must be kept as short as possible. Distortion in this context could be both amplitude and phase distortion - leading to reflections amongst other undesirable factors.

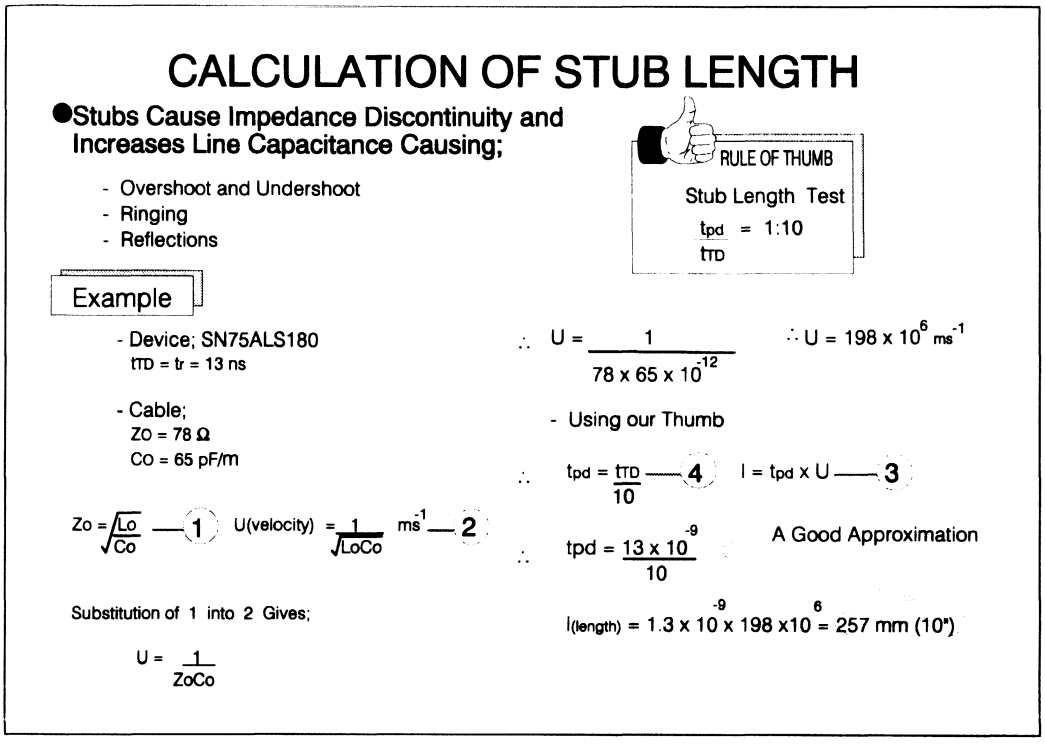


Figure 4.59 - Calculation of Stub Length

These connections are usually termed stubs. A stub is a connection to the transmission line from either a driver or a receiver . However, even when short in comparison to the length of the main transmission line it too could exhibit transmission line effects. Any connection to the line will cause an impedance discontinuity, leading to reflection at the stub/transmission line boundary.

To minimise these effects the stub should be kept as short as possible, so that the stub is seen as a lumped (non transmission line) rather than a distributed (transmission line) load to the line.

4.18.1. How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, t_{pd} ,is more than 5 times the transition times of the driver, t_T. The converse is true if the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given below.

The figure shows a calculation for determining the maximum length of the stub. The rule of thumb states that the transition time of the pulse sent down the line should take ten times the time taken for the pulse to propagate to the end of the stub. As a resulting any reflections will be incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used.

The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, l_S , as;

$$l_S = t_{TD}/(10)$$

Using the SN75ALS180 and its transition time of 13ns, a cable with a characteristic impedance of 78Ω and line capacitance of 65pF, gives a maximum stub length of 254 mm or ten inches.

The main effect in this case will be a slight increase in the capacitance loading of the line.

4.19. The Unit Load Concept

4.19.1. Line Loading Considerations

One final consideration needed to implement a digital data link is the number of driver / receiver elements that can be connected to the line. This is now discussed;

The maximum number of drivers and receivers that can be placed on a single communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V . The loads may consist of drivers and/or receivers but does not include the termination resistors, which may present additional loads as low as 60Ω total.

The first example shows a unit load calculation for the dual SN751178 driver/receiver which offers a unit load value of 1.1 U.L - meaning 29 such devices could be connected on one line. In the second example the TL3695 transceiver is used. Since this device is internally connected as a transceiver, i.e. driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 18 kΩ, giving a transceiver current of 0.6mA. This can be taken to represent 0.6 U.L. which will allow up to 47 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designers risk.

The graph in the top right corner of the figure is used to define the boundaries of the unit load, and works by superimposing the voltage and current characteristics of the load upon a reference trace. A line from - 3 V is drawn at a tangent to intercept receiver input current at the 12 V point. Similarly, a line is drawn from -7 to intercept the driver leakage current at the 5 V point. The currents indicated at - 7 V and -12 V are then compared to the currents specified by the standard. The larger of the two voltage to current ratios forms the unit load value.

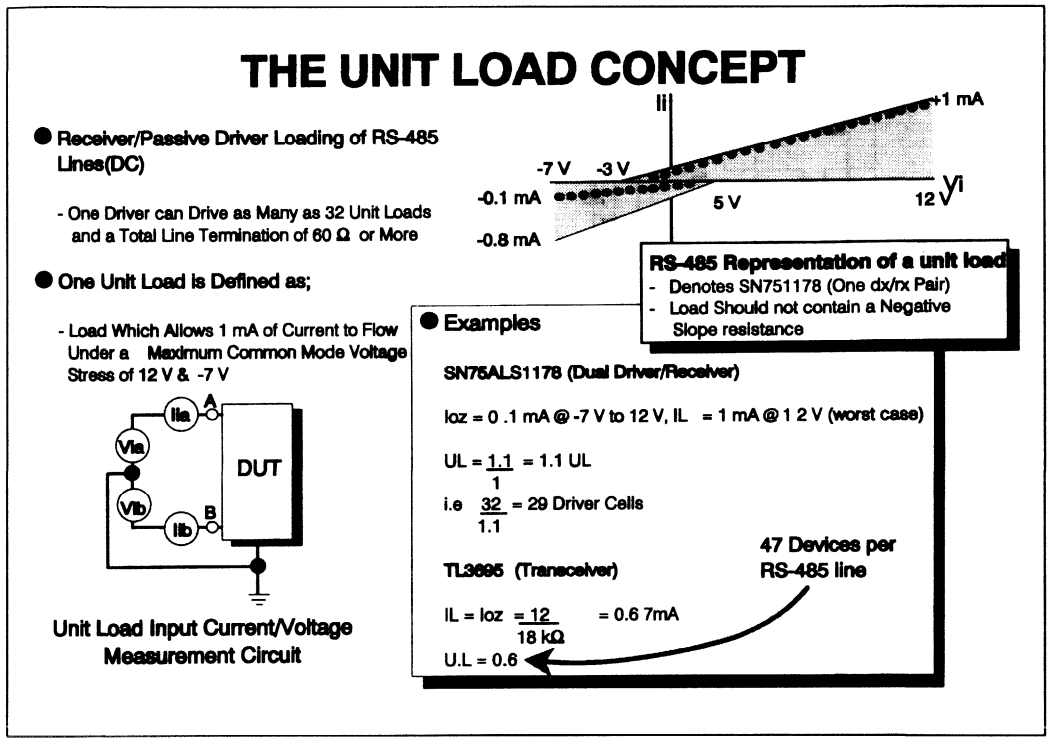


Figure 4.60 - The Unit Load Concept

The electrical characteristics should not show any negative resistance otherwise instability and spurious oscillations could occur.

4.19.2. Total Load Characteristic Limits (RS-422)

In RS-422 the dc load characteristics is specified much more simply;

The total load including multiple receivers, fail safe circuitry, and cable termination shall have a resistance greater than 90 Ω between its input points (A and B), i.e. across the line, or when the cable is left un-terminated the resistance shall be greater than 400 Ω, and shall not require a differential input voltage of more than 200 mV for all receivers to assume the intended binary state.

Of the many application areas for data transmission perhaps one of the most demanding in terms of robustness is that of process automation.

4.20. Process Control Application

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application.

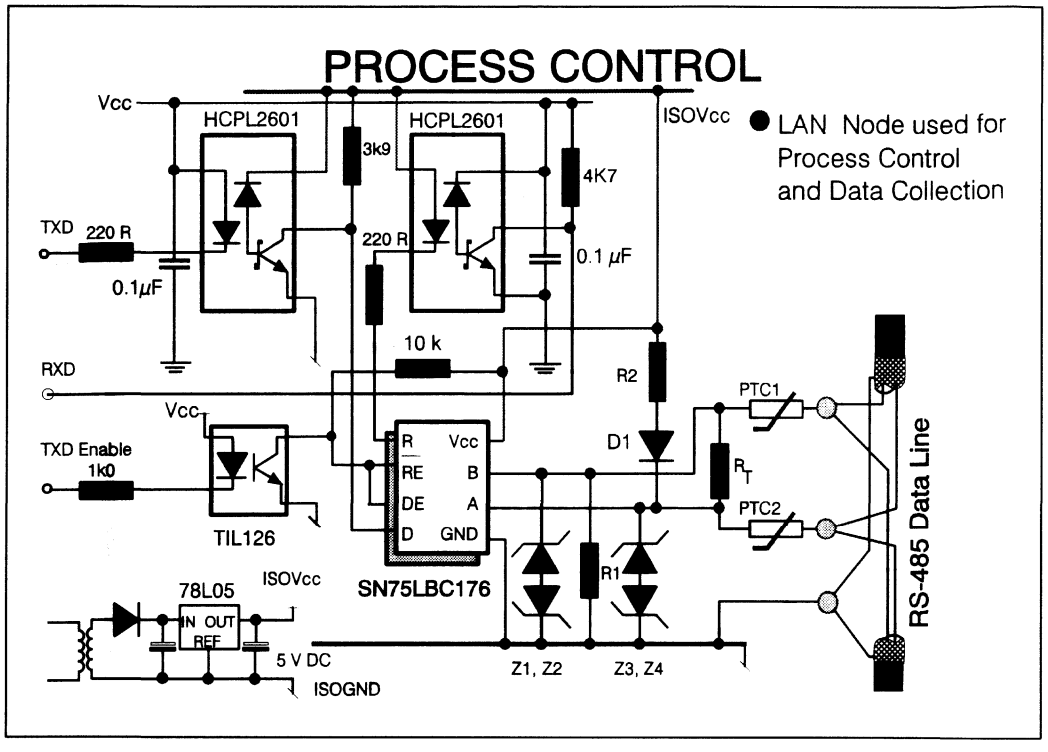


Figure 4.61 - Process Control Application

4.20.1. The need For Galvanic Isolation

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

Taking a more practical view of where problems are likely to occur when using a galvanic interface, can be found in the industrial environment. For example consider the case when the interface node, shown in the figure, connects between a data logger and a host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for

the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a 'Field bus' type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit. Other nodes, master or slaves, may be distributed along the bus in an arbitrary fashion and may be separated hundreds of metres in distance.

The bus driver used is the **SN75LBC176**, chosen for its low power consumption and high data rate capability. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability.

Transceiver protection circuitry is formed by Z_1,Z_2,Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows:

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

Using a cable with a characteristic impedance of Z_O = 120 Ω and a desired V_{TH} of 200 mV, requires $R_1 = R_2$ to be around 1.6 kΩ in value. The terminating resistor, R_T would be in the order of 124 Ω.

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions. The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/opto isolators. The HCPL2601 is chosen for its high data rate capability, t_p = 75 ns (max), and its high voltage isolation.

The HCPL2601 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The HCPL2601 consists of a GaAsP light emitting diode and integrated light detector, composed of a photo diode, a high gain amplifier and a Schottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13mA (eight 1.6mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-pin dual-in-line plastic package the HCPL2601 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000V/µs.

A 0.1 µF capacitor has been connected between V_{CC} and ground to improve switching performance.

4.21. SN75LBC176; Ultra Low Power

The SN75LBC176 has the lowest power consumption in the industry; 1 mW vs 2.5 mW offered by the nearest low power competitor. The ac performance is also significantly better; T_{DD} of 25 ns(max) vs 60 ns (max).

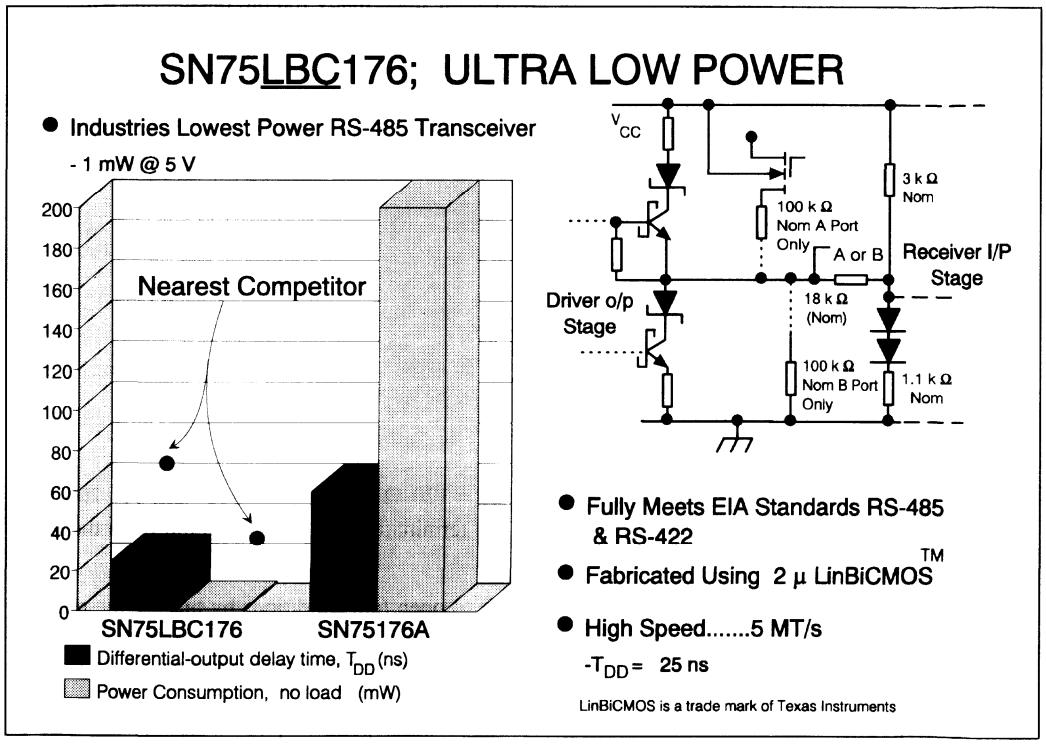


Figure 4.62 - SN75LBC176; Ultra Low Power

4.21.1. Improve MTBF

Although not representing the most glamorous end of the semiconductor design spectrum, reliable

line interface circuits are crucial if the overall system mean time between failure (MTBF) is to be minimised. System designers have long been aware that often the week link in ensuing system reliability has been line interface circuits. This vulnerability is due in part to the circuits close proximity to the outside world via the edge connector. Consequently interface circuits are particularly

susceptible to failure from high external voltages caused by noise, ESD or incorrect insertion of cables. For this reason the technology of choice for many Texas Instruments emerging interface products is LinBiCMOS.

LinBiCMOS, the Technology of Choice

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3 µm pure CMOS technology with 16 V capability, making it ideal for the design of low power analog products such as op-amps and analog-to-digital convertors (many examples of which are discussed elsewhere in this book). By shrinking the geometries to 2 µm and adding a high performance 30 V bipolar structure, a new änalog"merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost , as many "nice to have"features can make a process too expensive to address a wide range of opportunities.

By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective. Modules available for LinBiCMOS

include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and schottky diodes for clamping.

The Applications

With its high voltage capability and excellent switching speed LinBiCMOS is ideal to address standards such as EIA-232 and RS485. For example the RS485 standard, demands that driver output can be shorted to +12V and -7V without damage. this is particularly difficult to implement as RS485 devices are designed to operate from a single 5 V supply, meaning that parts of the chip must be designed to operate well outside its supply rails. Further more the "party line"nature of the standard requires devices that must be able to withstand contention (multiple drivers accessing the bus simultaneous) without failure. For this reason short circuit protection and thermal shutdown are built into the chip.

The Device

The SN75LBC176 and it's extended temperature range version (-40°C to 85°C) the SN65LBC176 are high speed and low power monolithic integrated circuits designed for bidirectional data communications on multipoint bus transmission lines. Both devices fully meet the EIA (Electronics Industries Association) RS-422 and RS-485 specifications. the devices contain a single transceiver with complementary driver and receiver enable schemes and is housed in a single 8-pin package.

Using the LinBiCMOS process allows the SN75LBC176 to achieve a power supply consumption of just 1 mW (200µA at 5 V) when in the passive state. Furthermore this is achieved without the usual speed penalties; the SN75LBC176 has a driver output rise time (TDD) of just 25 ns, making data rates of 5 Mbps possible.

This combination of low power and high speed is particularly relevant to todays demanding applications requiring multiple channel operation such as the small computer interface (SCSI) or telecommunication applications.

4.22. Synchronised RS-485 with handshake

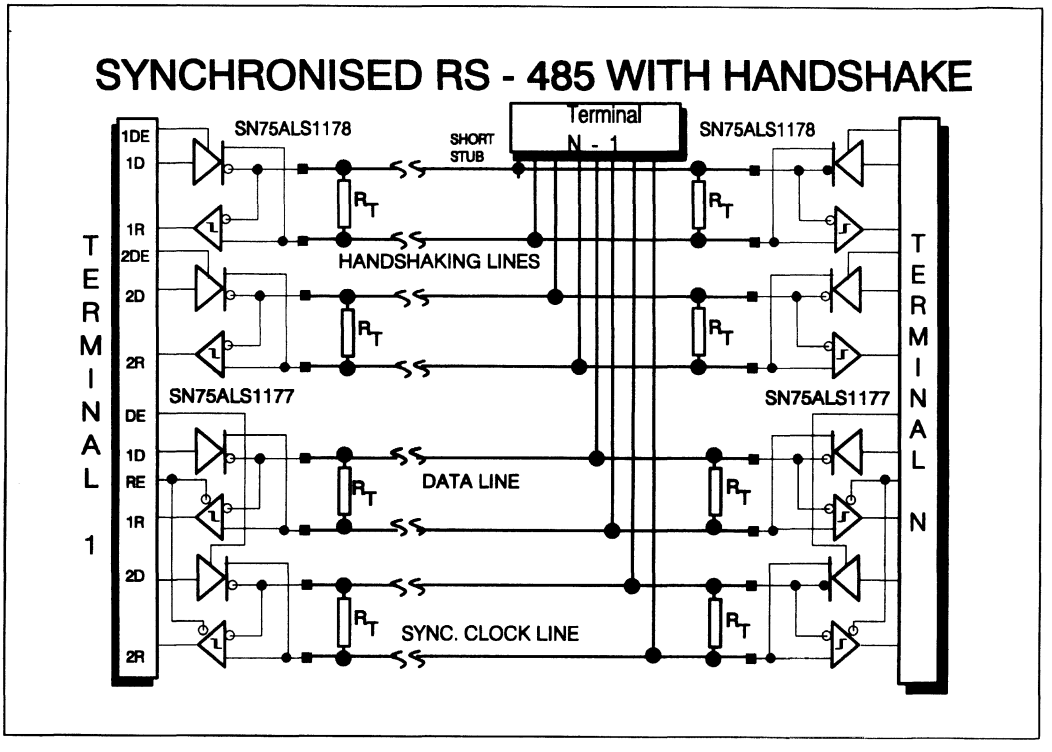


Figure 4.63 - Synchronised RS-485 with handshake

4.22.1. Boost the Data Rate

Most RS-485 systems operate with a single twisted pair as the data transmission medium limiting the data transfer to asynchronous mode. In addition, the single line must also transfer receiver address, start and stop bits and a preamble to enable the receiver logic to distinguish between data or rubbish on an idle line. These additional transferred bits impact the speed of operation on the data line.

Alternatively, synchronised data transfer can be implemented by adding an additional sync. clock line as shown on the figure, and can be further complemented with the addition of a couple of handshake lines. The overall transfer of the "real data" can be significantly speeded up, as most of the control bits used in asynchronous mode will be eliminated from the data path.

Specifically, synchronous data transfer benefits from applications where complete blocks of data can be transferred because the usual requirement in asynchronous transfer for breaking the data down in small groups of 8-bits (proceeded with a start bit and concluded with a stop bit) is eliminated.

Several terminals or station can be connected to this synchronised RS-485 system. The number of stations is only limited by the usual rules for RS-485. Daisy-chain connection between terminals is required unless each terminal is connected to the main data path via a short stub as the shown for terminal number N - 1.

4.22.2. Why use the SN75ALS1177 and SN75ALS1178 ?

The SN75ALS1177 contains two drivers and two receivers in a single 16-pin package. Each pair of drivers and receivers has a common enable line. Upon transmission, both the data and sync. clock drivers are enabled allowing synchronous transfer of data. When shifting to receiver mode, both drivers are disabled, and the two receivers are enabled simultaneously. Due to the complementary enabling schemes for drivers and receivers (logic 1 enables the drivers but disables the receivers, and logic 0 the opposite), it is possible to connect both driver and receiver enable signals to the same control output. This reduces the number of I/O's required.

The SN75ALS1178 also contains two drivers and two receivers in a 16-pin package, but offers a different enabling pattern. The two receivers are always active and listen continuously to the handshake lines as necessary. However, the two drivers can be independently enabled as required by a handshaking scheme.

In summary, the SN75ALS1177 and SN7ALS1178 offer a simple but versatile solution synchronous transfer of data at high speeds. Their configuration as two driver/receiver pairs adds to the effectiveness of the application

4.23. New RS-485 Releases

1991 saw the release of several new ALS designs. Targeted towards industrial and telecommunication applications these new ALS devices offer both speed and power improvements over their existing LS counterparts. The figure shows clearly the performance advantage gained by switching to ALS designs.

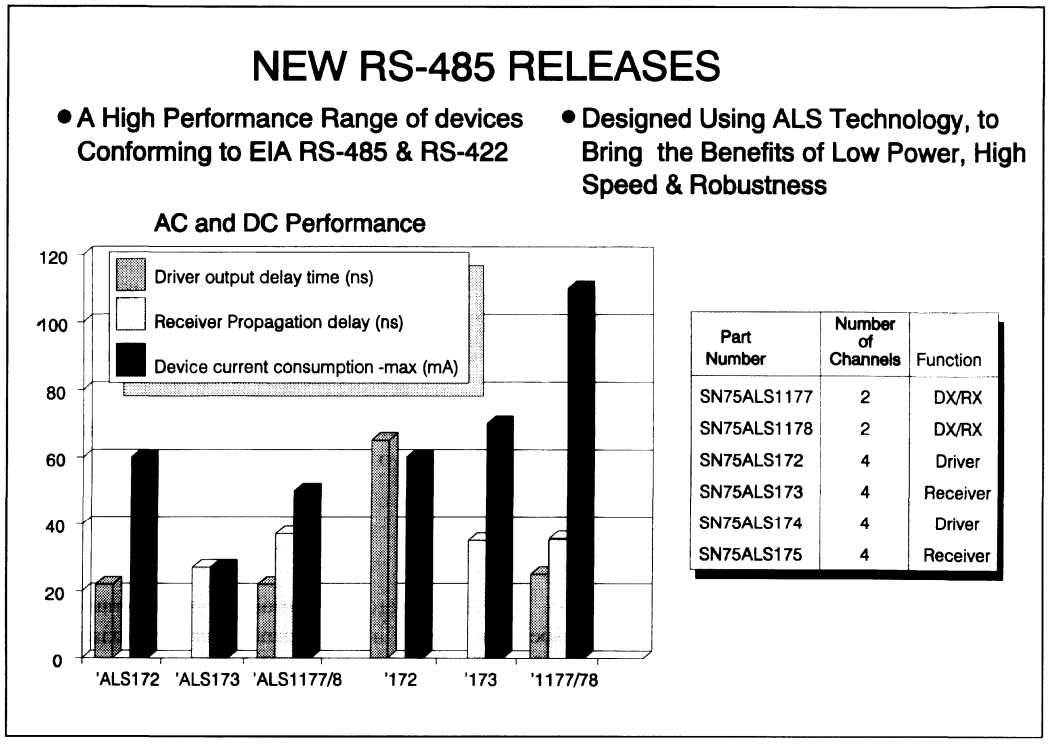


Figure 4.64 - New RS-485 Releases

4.24. Use of Repeaters

4.24.1. The Need for Repeaters

The major advantage of RS-485 is that it permits multiple drivers and receivers to operate over a 2-wire bus, thus setting up a party-line architecture. When such a data communication bus system is transmitting data over lines as long hundreds of meters or even thousands of metres, attenuation is often experienced between a driver at one end and a receiver in the other end (over long distances the cable's resistance does have an effect). Such systems can benefit from the use of signal restoration by means of bus repeaters.

Similarly, when more than 32 unit loads are connected to a bus, requirements for additional buffering arise. A bus repeater has in this function a different role from restoring the original signal namely to drive another 32 unit loads.

Repeater Solutions

Bus repeaters in data communication systems receives degraded signals from the transmission line, squares up the pulses, and re-transmits the signals onto the line to the receiving station. Because the

original transmitted signal is restored (squared up), the communication system becomes less susceptible to noise and other types of interference on the lines.

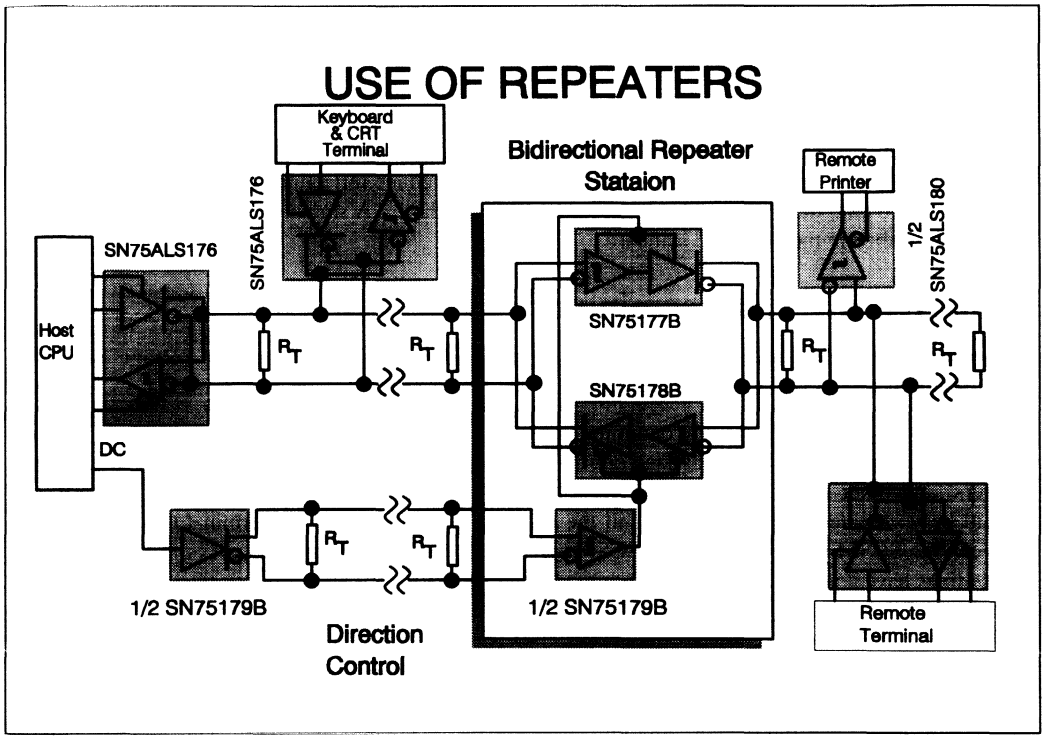


Figure 4.65 - Use of Repeaters

The shown "use of repeaters" application for bi-directional control of an RS-485 bus with long transmission lines is implemented with a bi-directional repeater station. Two types of repeaters are available: One version is enabled by a logic 1 control signal and the other by a logic 0. Thus, without any glue logic you can design a fully bi-directional repeater station that restores signals from both directions on a line

Enabling and disabling of the repeater drivers and receivers and thereby the data direction is controlled by the host micro-controller. In data communication systems where no host CPU controls the data direction, intelligence needs to build into the repeater station to maintain system control. This allows also for independent communication on each side of the repeater station providing additional flexibility and faster overall data exchange.

Recommended Products

Dedicated products designed specifically for repeater purposes are the SN75177B and SN75178B. Employing these repeater devices in simple repeater stations as the shown, completely eliminates the need for any glue logic due to their enabling scheme. For repeater stations including protocol

controllers may also benefit from devices such as SN75ALS1177 and SNALS1178 with their multiple drivers and receivers.

4.25. Products for the ANSI SCSI

SCSI is an acronym for Small Computer System Interface. SCSI is an industry-standard interface, defined by the American National Standards Institute (ANSI). SCSI is a parallel interface for computers and peripherals to communicate over short distances at very high-speed. The SCSI bus is bi-directional and is terminated at both ends of the cable to reduce reflections. An active and a passive termination are both described in the proposed SCSI-2 standard. A single-ended and a differential bus are also described in the proposed standard.

4.26. Active SCSI Terminators

Improve SCSI-2 Bus active termination with a fixed 2.85 V low drop out voltage regulator specifically designed for Active SCSI Termination.

The 8-bit or 16-bit SCSI-2 bus will communicate over a maximum distance of six meters, and contains 18 or 27 data and control lines that can communicate with up to 8 SCSI devices (computer, disk drives, printers, and other computers, etc.). These devices are daisy-chained through the SCSI ports and should be terminated at the computer and the most distant peripheral. A terminator is either added between the SCSI System Cable and a SCSI connector or to the last available port on the SCSI device. These lines have a nominal characteristic impedance of 110 Ω.

Passive Termination (Alternative 1).

The resistive divider shown in the figure is used to terminate the single-ended SCSI bus. The Schottky diode is used to protect the power source from reverse currents. The output impedance is 132 Ω, which does not match the transmission line characteristic impedance of 110 Ω. This line bias voltage is not regulated, and the resulting output voltage will vary with the supply and the load current. This fluctuating output voltage will reduce the data signal noise margin.

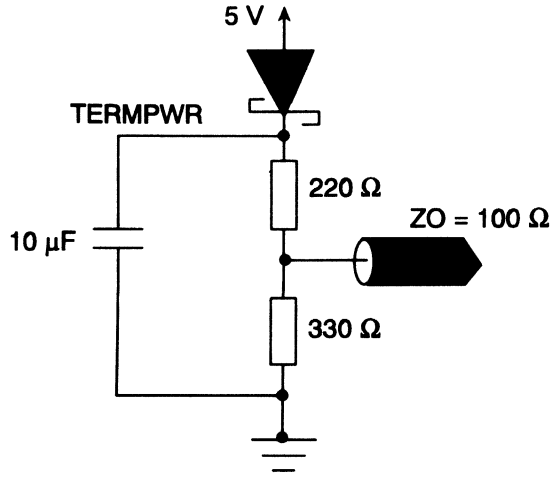
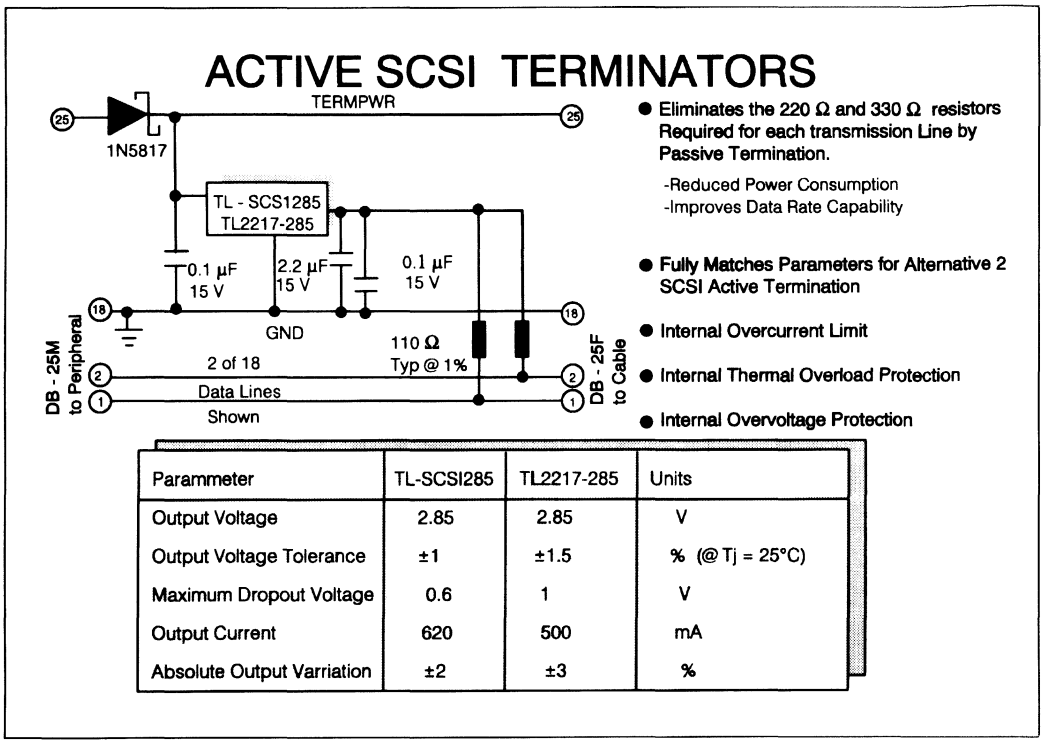


Figure 4.66 - Passive Termination (Alternative 1).

Active Termination (Alternative 2).

An active termination system using TL-SCSI285 low-dropout (0.6 V) regulators is shown in the following figure. The device is specifically designed for active SCSI cable termination, and the low-dropout characteristic provides a wide TERMPWR voltage range. The line regulation of the TL-SCSI285 provides immunity to variations in TERMPWR. Total tolerance in the 2.85 V output is only ±2 percent over temperature, including variations caused by line and load changes. The 110 Ω±2 percent series resistors match the typical transmission line characteristic impedance of 110 Ω, resulting in improved system performance from the resulting higher signal-to-noise ratio. Unlike the passive termination or active termination using adjustable regulators, the TL-SCSI285 termination system bus requires a very low quiescent current. The device has internal current limiting, over voltage protection, reverse transient protection, ESD protection, and thermal protection. A configuration of an active terminator for an 8-bit 18-line SCSI bus using the TL-SCSI285 is illustrated in Figure 4.67. A 27 line termination would require that a TO-220 package be used due to the increased power dissipation and 50 pin connectors would be needed.



Parammeter	TL-SCSI285	TL2217-285	Units
Output Voltage	2.85	2.85	V
Output Voltage Tolerance	±1	±1.5	% (@ Tj = 25°C)
Maximum Dropout Voltage	0.6	1	V
Output Current	620	500	mA
Absolute Output Varriation	±2	±3	%

Figure 4.67 - Active SCSI Terminators

4.27. SN75LBC976; Two Chip Differential SCSI

Much debate has taken place on differential versus single ended SCSI for data rates above 5 million transfers per second (MTps). The proliferation of active SCSI terminators such as the TL-SCSI285 is testimony to this fact. It clear however that for data rates approaching 10 MTps, differential SCSI is essential.

The SCSI interface is made up of 8 data lines, one parity bit, and 9 control lines, making 18 channels in total. See table. The only differential transceivers capable of transmitting at 10 MTps data rate have utilised the Low power and Advanced Low Power Schottky technologies. With 18 transceivers per interface the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

From a designers viewpoint. 2.4 watts is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where shear equipment size is the limiting element. A further factor is board area, using one discrete transceiver per channel, i.e. 18 8-pin SO packages, is unacceptable for many applications.

From a semiconductor designers viewpoint integrating a number of transceivers is of course possible however the limiting factor once again is power dissipation. The SN75LBC976 is designed to

overcome both the problems of power dissipation and integration. The device incorporates on a single IC nine RS-485 configurable transceivers each capable of transmitting at 10 MTps. This is made possible using a Linear BiCMOS technology called LinBiCMOS. With all drivers disabled the power consumption of the 'LBC976 is 1.5 mW, with all drivers enabled the consumption rises to 45 mW, a considerable saving over the LS and ALS parts. The package size has also been reduced to a minimum using the 0.635 mm pitch 56 pin SSOP package.

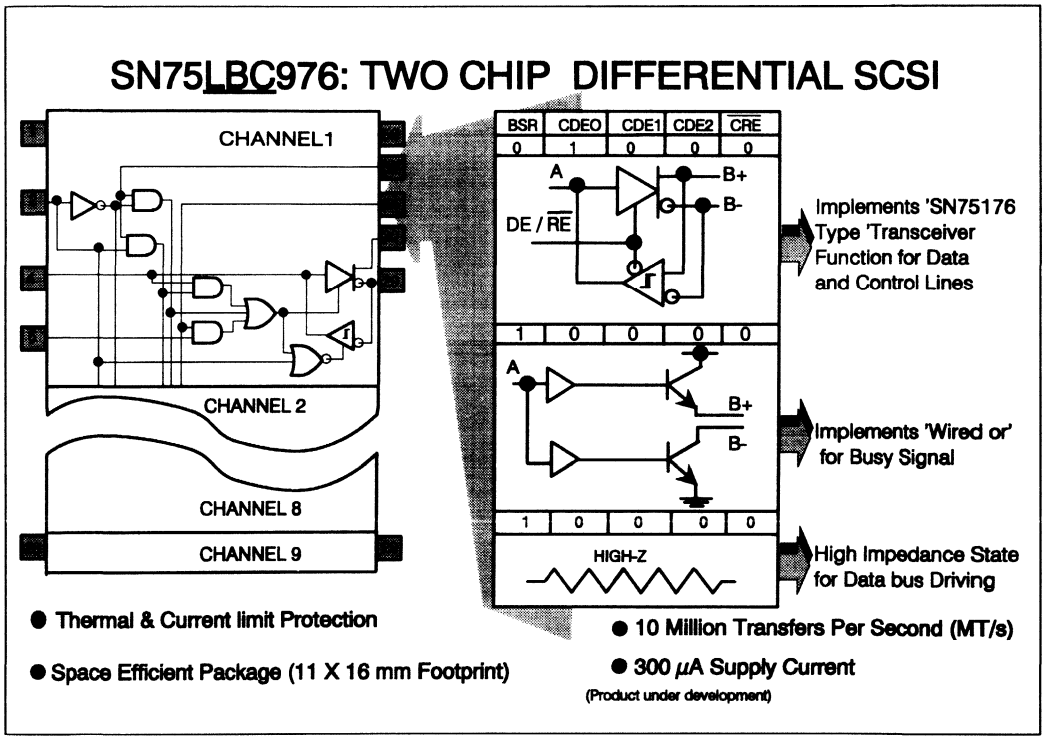


Figure 4.68 - SN75LBC976; Two Chip Differential SCSI

A secondary benefit of using a BiCMOS technology is by virtue of the robust bipolar transistors. Bipolar circuits are used on the line side of the driver and receiver. This yields excellent ESD protection compared with CMOS structures, 2.5 kV against the MIL-STD-883B specification.

The SN75LBC976 is fully configurable to facilitate connection to any type of SCSI system arrangement. The 9 channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, CRE control pins.

The 7 channel configurations are;

1. **Transparent, permanently enabled Receiver.**
2. **Transparent, permanently enabled Driver.**
3. **Bi-directional transceiver with direction control.**
4. **Driver with enable control.**
5. **Open ended driver for Wired OR control lines.**
6. **Driver with ORed data and enable lines.**
7. **Permanent high impedance state.**

Differential SCSI Bus Signals				
Mnemonic	**Pin**	**Pin**	**Mnemonic**	**Driven By**
Shield Gnd	1	2	Ground	Initiator/Target
+DB(0)	3	4	-DB(0)	Initiator/Target
+DB(1)	5	6	-DB(1)	Initiator/Target
+DB(2)	7	8	-DB(2)	Initiator/Target
+DB(3)	9	10	-DB(3)	Initiator/Target
+DB(4)	11	12	-DB(4)	Initiator/Target
+DB(5)	13	14	-DB(5)	Initiator/Target
+DB(6)	15	16	-DB(6)	Initiator/Target
+DB(7)	17	18	-DB(7)	Initiator/Target
+DB(P)	19	20	-DB(P)	Initiator/Target
DIFFSENS	21	22	Ground	Active High
Ground	23	24	Ground	
TERMPWR	25	26	TERMPWR	Any Device
Ground	27	28	Ground	
+ATN	29	30	-ATN	Initiator
Ground	31	32	Ground	
+BSY	33	34	-BSY	Initiator/Target
+ACK	35	36	-ACK	Initiator
+RST	37	38	-RST	Any Device
+MSG	39	40	-MSG	Target
+SEL	41	42	-SEL	Initiator/Target
+C/D	43	44	-C/D	Target
+REQ	45	46	-REQ	Target
+I/O	47	48	-I/O	Target
Ground	49	50	Ground	

4.28. The Total Peripheral Interface Solution

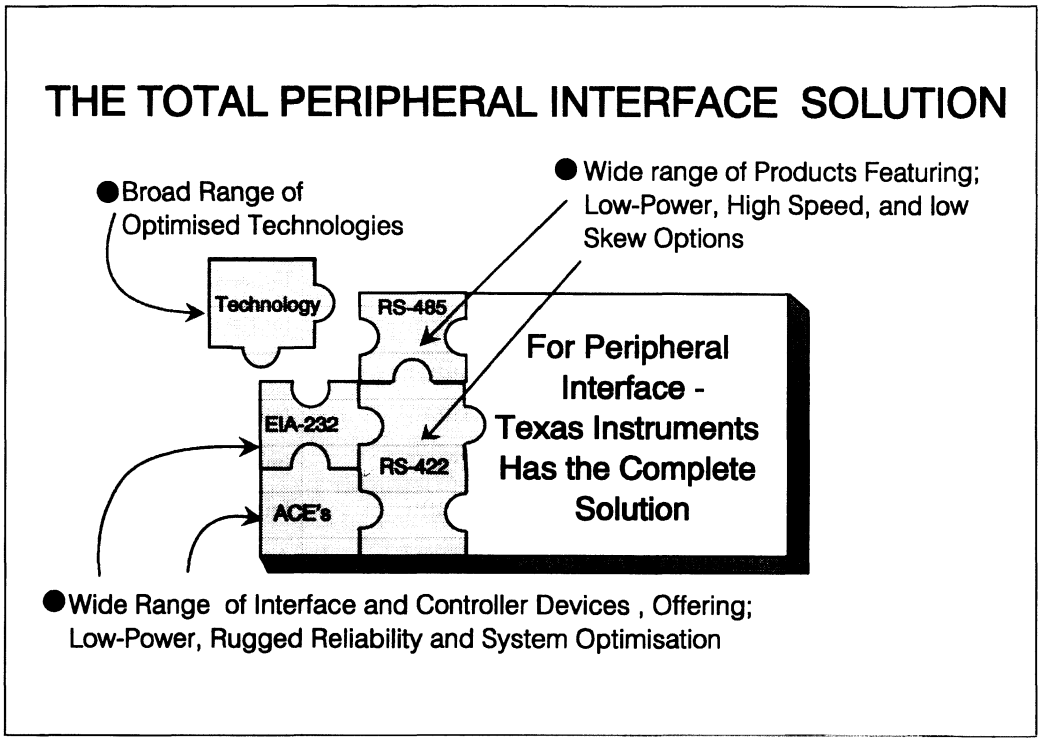


Figure 4.69 - The Total Peripheral Interface Solution

The range of products discussed throughout this section demonstrate the commitment made by Texas Instruments to the field of peripheral interfacing. Use of leadership technologies has enabled high performance line drive/receive functions to be produced and highly integrated controller functions. Key highlights are summarised below;

Technology

Broad range of technologies available from high density digital CMOS to high voltage, high speed analogue bipolar. Also increasing use of merged technologies offering the advantages of both bipolar and CMOS.

Products for EIA-232

Use of optimised bipolar process to give low-power BiMOS driver/receiver range of products, optimised for common EIA-232 applications. Highly integrated controller functions containing up to two serial ports, one parallel port and FIFO'S for high end applications.

Products for RS-422/RS-485

A wide range of devices suitable for many applications, from high speed disc drives to industrial and automotive applications. Particular emphases has been placed on low-power, high-speed devices offering low skew options for both telecommunications and disk drive applications.

4.28.1. Selection Guide

RS-422 Data Transmission Circuits

Device	Devices	Device	Key
Line Driver	2	SN75158	Industry Standard
		SN75159	Industry Standard
		SN75ALS191	High Speed, Low Power
		uA9638	Industry Standard
	4	AM26C31	Low Power
		AM26LS31	Industry Standard
		MC3487	Industry Standard
		SN75151	Industry Standard
		SN75153	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
		SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS192	High Speed
		SN75ALS194	High Speed

Line Receiver	2	SN75146	Bulit In 5 MHz L P Filter
		SN75157	Industry Standard
		uA9637	Industry Standard
		uA9639	Industry Standard
	4	AM26C32	Low Power
		AM26LS32	Industry Standard
		MC3486	Industry Standard
		SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS173	High Speed
		SN75ALS175	High Speed

Line Transceivers	1	SN75176A	Low Power
		SN75176B	Industry Standard
		SN75177B	Industry Standard Repeater
		SN75178B	Industry Standard Repeater
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
(Drivers / Receivers)	1/1	SN75179B	Industry Standard
		SN75ALS180	Industry Standard
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
		SN75ALS170	High Speed
	3	SN75ALS171	High Speed
		SN75ALS1711	High Speed
	9	SN75LBC976	Low Power¥

RS-485 & RS-422 Data Transmission Circuits

Device	Devices	Device	Key
Line Drivers	4	SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
Line Receivers	4	SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS172	High Speed
		SN75ALS174	High Speed
Line Transceivers	1	SN75176A	Low Power
		SN75176B	Industry Standard
		SN75177B	Industry Standard Repeater
		SN75178B	Industry Standard Repeater
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
	1/1	SN75179B	Industry Standard
		SN75ALS180	Industry Standard
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
(Drivers/ Receivers)	3	SN75ALS170	High Speed
		SN75ALS171	High Speed
		SN75ALS1711	High Speed
	9	SN75LBC976	Low Power

Notes

¥ Product currently under development, contact TI representative for further details.

5. Trouble Shooting Guide

PROBLEM	PROBABLE CAUSE (S)	CORRECTIVE ACTION(S)
1. Damage to line receivers	a) common-mode noise b) differential noise	a) eliminate overstress voltage or current b) change to wider Vcm line receiver
2. Damage to line drivers	a) common-mode noise	a) eliminate overstress voltage or current
3. Data corrupted after establishing connection	a) transient noise	a) error detect and resend data a) add transient noise immunity
4. Failing EM emission requirements	a) common-mode noise	a) add common-mode noise immunity a) eliminate source of noise
5. Damage to terminating resistors	a) transient noise b) insufficient power ratings	a) add protection circuitry b) derate power rating by 50%
6. Data corrupted when adding or removing nodes to bus	a) power up/down "glitch" b) low bus impedance with power off	a) use line drivers with power up/down glitch-free circuitry b) use line drivers specified for high impedance with Vcc=0
7. Crosstalk between adjacent cables in bundle	a) capacitive coupling	a) use balanced (differential) twisted pair interface a) add individual shields a) reduce driver output slew rate a) reduce driver output voltage swing

8.	Interface IC overheats	a)	load impedance too low	a)	remove extra terminating resistors
				a)	use higher Zo cable
		b)	bus contention	b)	fix arbitration software
9.	Impedance mismatches	a)	no impedance matching resistor at cable end(s)	a)	terminate cable with resistor equal to cable Zo
		b)	long stub lengths	b)	shorten stubs off of main data line (daisy chain)
		c)	non uniform twisting of cable	c)	use controlled impedance data cable
		d)	wrong value terminating resistor for cable being used	d)	lower data transmission rate or distance
10.	Differential noise	a)	signal wires not twisted	a)	used twisted signal cable
		b)	current flowing through shield	b)	terminate shield at one end only
		c)	non monotonic driver output		
11.	Common-mode noise	a)	capacitive coupling to outside world	a)	add over-all shield
				b)	eliminate ground loops
		b)	ground loops	c)	add shields to each signal pair
		c)	asymmetric driver outputs	d)	add protection circuit to data line
				e)	transformer couple to data line
				b)	terminate with Zo/2 from line to ground at receiver
				b)	specify differential driver with low delta Voc
12.	12.Open circuit fail-safe	a)	no or too large of pull-up and pull-down resistors on receivers	a)	use resistors low enough to maintain Vt max with lin max
				a)	use line receiver with fail-safe resistors internal

13.	Terminated fail-safe	a)	differential voltage not driven to Vt max at receiver	a)	change software to eliminate indeterminate state
		b)	protocol logic allows indeterminate state	a)	add offset voltage greater than Vt max
		c)	line pull-up and pull-down too large	c)	reduce line pull-up and pull-down resistor values
14.	Receive noise as data	a)	terminated fail-safe	b)	add terminated fail-safe offset voltage
15.	Transient noise	a)	lighting	d)	add common-mode noise immunity
		b)	adjacent high voltage or current equipment		
		c)	RFI		
16.	Bus contention	a)	arbitration protocol	a)	fix software
17.	Receive noise after disconnecting cable	a)	open circuit fail-safe	a)	add open circuit fail-safe circuit.

Section 5
Intelligent Opto Sensors

Section Contributions by:

Derrick Robinson

Contents Section 5.

1. Mixed Mode Light Sensors

1.1. Introduction

1.1.1. Visual World

A common theme in Linear seminars is that "The Real World" we all inhabit is Analogue. Despite continued increases in complexity, and reductions in cost, of digital information handling, we still need to capture analogue information to process. This drives the growing efforts on mixed-mode semiconductor technologies and designs.

Analogue information is often in a non-electronic form, and needs to be "sensed" or transduced. This looks at the application of Texas Instruments established mixed-mode LinCMOS(TM) and LinBiCMOS(TM) silicon technologies to create "Intelligent Opto Sensors". In such devices light sensor arrays are combined with precision analogue and digital elements to create functions that are easily combined with digital processing systems.

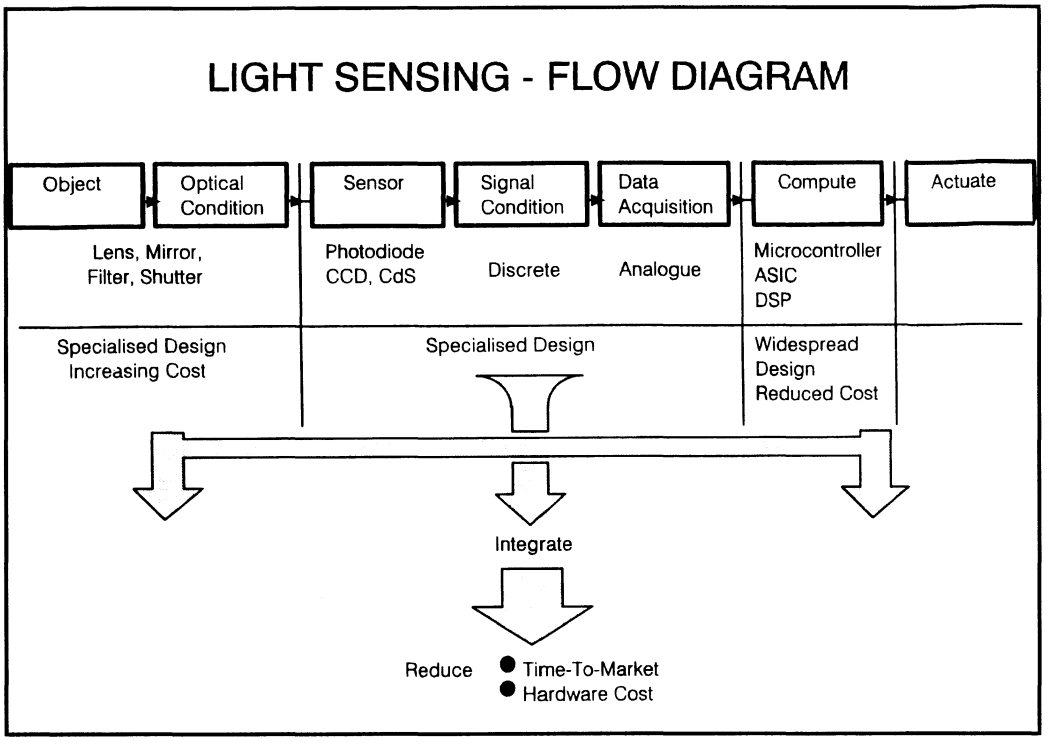
1.1.2. Visual Sensor Market

There is continued rapid growth (>40%/year) in Automatic Identification. Despite rapid growth in magnetic and rf coding of objects, the most widespread code probably still remains the visual printed barcode label. Because of the low cost of printing , optical recognition may well be a dominant identification technology for many years to come.

Further examples of recent volume applications of visual sensor input to electronics are the VCR and facsimile transmission (fax). In industry, process control is often effected by automatic visual inspection and data collection; visual position and motion control of motors by means of rotary or linear shaft encoders is also widely used.

The widespread pervasion of computer technology over recent years has not reduced the amount of paper-based information -- rather the contrary. One broad area of application where effective optoelectronic sensing is needed is in paper-handling - in printing -in copying -in locating specific printed information. There is a widespread need for paper edge location, paper orientation , printed line location , and optical character recognition. In many other areas of application, input information may be found in visual form and will be need to be electronically acquired.

There is thus a growing need to link digital electronic systems more effectively to the visual structure of the outside world.



1.2. Light Sensing - Flow Diagram

Figure 5.1 - "LIGHT SENSING - FLOW DIAGRAM "

1.2.1. Process

Although a wide range of information about the world around us is available in "visual" form, it is generally not immediately capable of being processed by digital electronic techniques. The sequence of activities to transform the visual structure of an object into electronic information and action, is shown in Figure 5.1.

1.2.2. Optical Conditioning

In general, the visual information from the object needs to be conditioned - by means of traditional lenses, mirrors, filters and shutters- to present it to the active surface of the sensor. These conditioning techniques are long established, frequently expensive, and require specialist mechanical and optical skill.

1.2.3. Analogue Conditioning / Data Acquisition

In general also, the output of an electronic light sensor is not in a form that can be directly processed digitally. The analogue visual structure of the object has been transduced merely into electronic analogues of current or charge. This electronic analogue output has to be conditioned - amplified, referenced, compared - then digitised for processing.This signal conditioning and data acquisition task requires analogue electronic engineering experience.

The cost of computation continues to fall rapidly, and progressively system design variants may be executed cost effectively in software.

1.2.4. Mixed-Mode Value

The challenge is to deploy mixed mode silicon technologies to make light sensors that can present information directly to a microprocessor or another digital processing technique.Not only may such components enable designs to be cost effectively manufactured. They may also simplify the design task to reduce Time-to-Market and save that most scarce of resources, the engineer's time.

As more of a design resides in software, it may also be possible to reduce costs right at the object end of the information flow. For instance, one may dispense with an expensive lens; simply by measuring, storing and correcting digitally the aberrations in the optical conditioning. As the cost of digital computation rapidly falls - the utility of an of "intelligent" light sensor rises.

1.3. Intelligent Opto Sensor Road

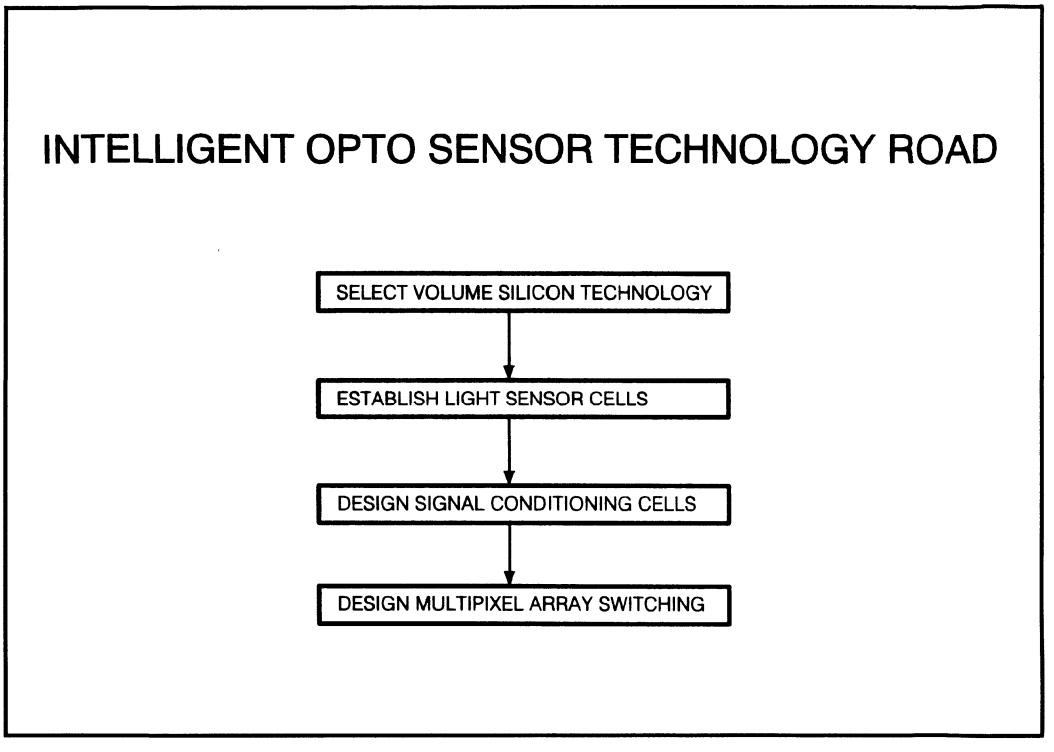


Figure 5.2 - INTELLIGENT OPTO SENSOR ROAD

1.3.1. Technology

The silicon wafer technologies chosen for Intelligent Opto Sensors, were LinCMOS (TM) and LinBiCMOS (TM). These are volume wafer technologies used by Texas Instruments to support a large number of mixed analogue-digital device designs. The technologies enable the combination on the same die of high precision analogue cells (such as low offset operational amplifiers, high precision analogue/digital converters etc) with complex digital functions.

Designs are cell-based, so that for most new designs much of the circuit structure on the device can be synthesised from existing proven functional cells. The technologies are fully supported by high volume wafer production of many device types, so there is high predictability of process yields, costs and delivery.

1.3.2. Sensor Cell

Hitherto, wafer designs using LinCMOS (TM) and LinBiCMOS (TM) had not included light sensing functions. The first task was to verify that efficient light sensing cells or pixels could be created from these technologies.

Two light sensing modes were established. These were current mode and charge mode which will be described later. It was also necessary to realise an effectice light barrier (so that the analogue and digital cells of a complex function would not be affected by incident light) and a channel stop structure (to separate the currents or charges on neighbouring pixels in an array).

1.3.3. Signal Conditioning

The simple current or charge analogue of incident light must in general be conditioned. Functions to be established were simple buffer amplifiers in combination with the light sensing cell, together with comparators and reference structures (to reference analogue outputs to a video black zero).

1.3.4. Data Acquisition

Lastly switching cells were designed to switch out the contents of different pixels in a light sensing array. Requirements here were that the analogue contents of one pixel should not affect the content of another, that switching should not lose any information and meet practical speed and efficiency requirements. Cells were also developed to present the pixel data in a form that could be easily handled by digital processing techniques.

1.4. Current Mode Light -Sensing Cell

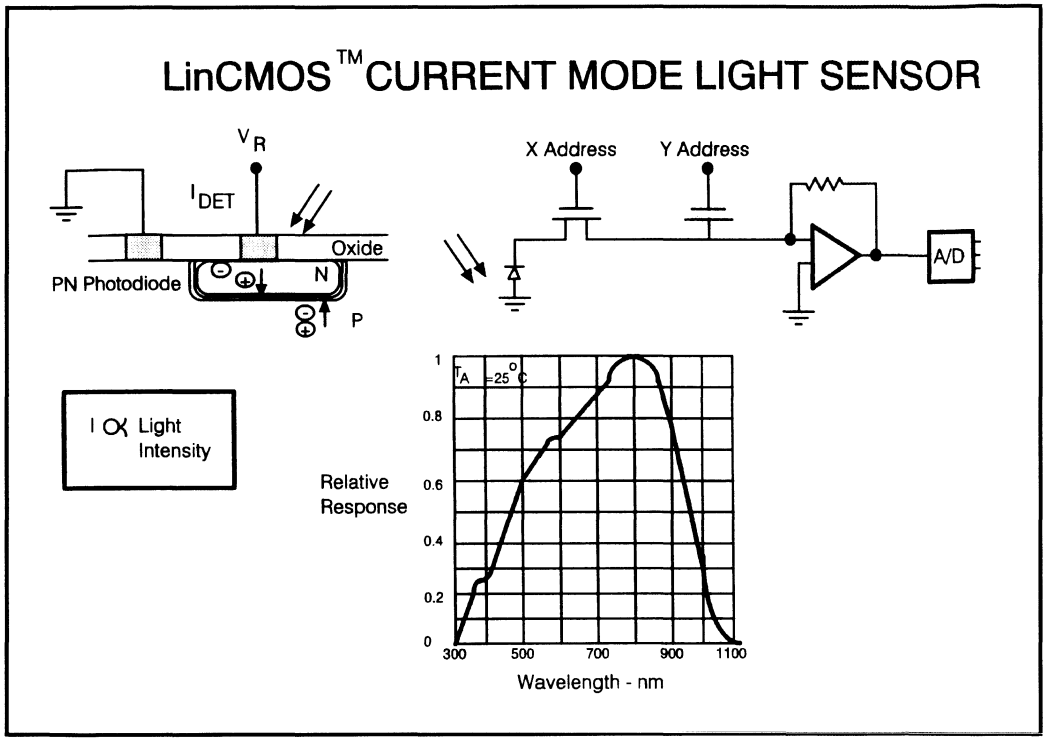


Figure 5.3 - CURRENT MODE LIGHT -SENSING CELL

1.4.1. Principle

Current mode light sensing is that used by photodiodes and phototransistors. Incident radiation is absorbed by silicon , generating electron-hole pairs which result in a photocurrent across a reverse-biassed p-n junction.

For a current mode sensor:

The current is proportional to the incident light intensity.

The current is also proportional to the diode area.

1.4.2. Scope

The current-mode photodiode cell is a quantum detector, usefully sensitive between 350nm and 1050nm. Peak responsivity is around 800nm. The photodiode cell can be applied in to visible radiation applications such as lighting level control (the human eye responds to the octave 400-800nm), and also in short infrared security applications (800-1050nm).

By suitable filtering, some interesting applications have been realised comparing the radiation at different wavelengths.

Note that silicon quantum detectors such as the photodiode are not useful for measuring long-wavelength infrared. Detectors of changes in low temperature infrared radiation (such as detection of body heat, in security systems) often use a phonon sensor such as a pyroelectric detector.

1.5. Charge Mode Light-Sensing Cell

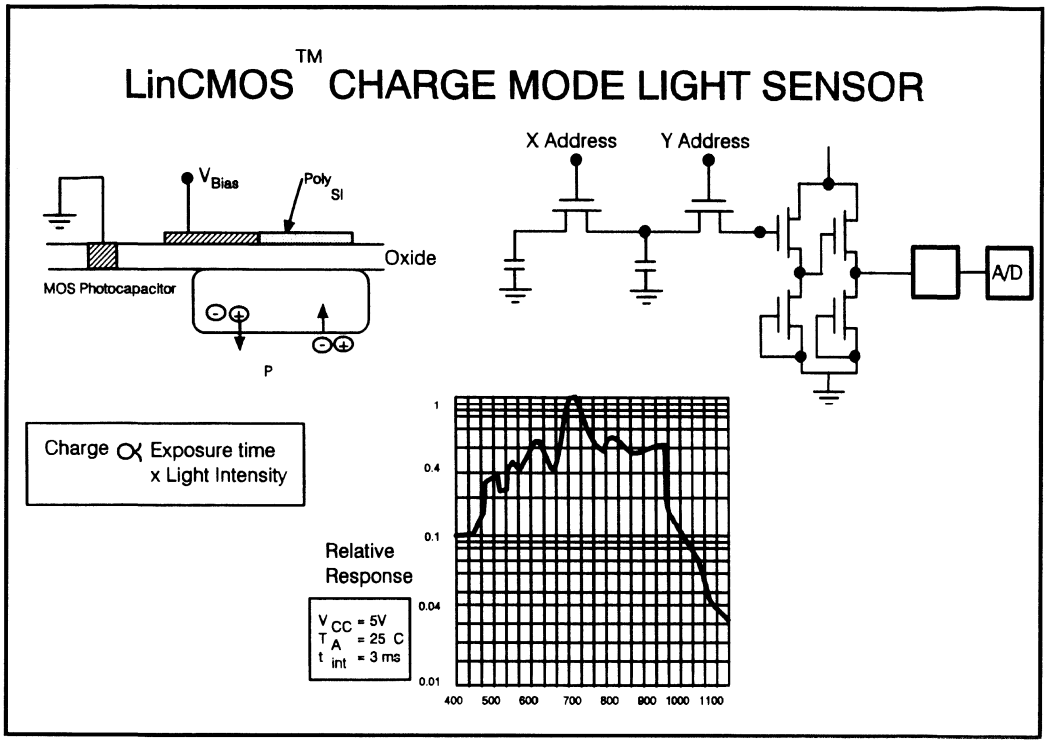


Figure 5.4 - CHARGE MODE LIGHT-SENSING CELL

1.5.1. Principle

In a silicon charge mode light-sensing cell, light is incident on a MOS capacitor. The photons are absorbed, and electron-hole pairs are created. The electrons are held in the capacitor cell, and the holes swept out to the substrate.

Unlike the photodiode, the charge-cell is an integrating sensor. Light-generated charge is built up on each pixel during the exposure period. At the end of the exposure period the analogue charge is switched out of the array. Generally the output sensing node is a diode, where the pixel charge is converted to an analogue voltage level.

For a charge-mode sensor:

Output Voltage is proportional to pixel Charge.

Charge is proportional to Light Intensity x Exposure time.

1.5.2. Scope

The LinCMOS (TM) charge mode sensing cell has good responsivity between 400nm and 1000nm. Like the current-mode sensing cell it can be used for both visible and short-infrared detection.

Note that the responsivity curve with wavelength is less smooth than that of the current-mode photodiode. This is caused by interference effects across the thin silicon dioxide surface film that makes up the MOS capacitor. In general, the characteristics of this film are very stable and predictable. It is possible to acquire and store spectral response characteristics in the output digital processing circuit, for spectroscopic applications.

2. TSL250 Light-To-Voltage Converter

2.1. The TSL250 Device

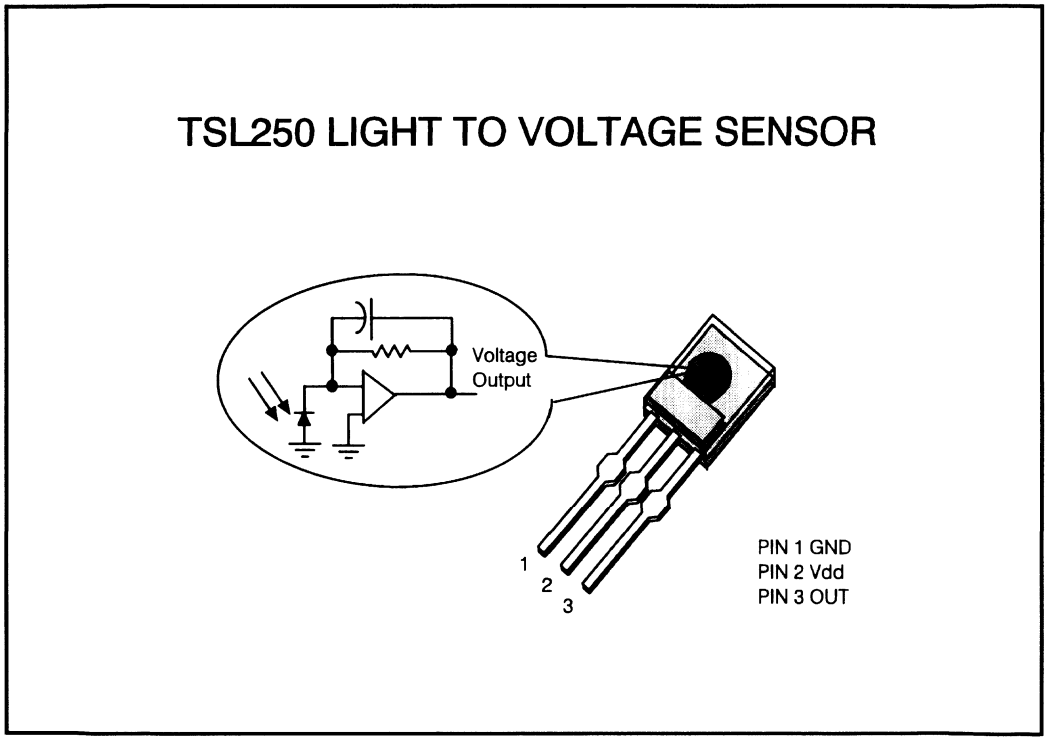


Figure 5.5 - TSL250 LIGHT-TO-VOLTAGE CONVERTER

2.1.1. Summary

In this section , we shall describe how a current mode sensor is combined on a chip with relatively simple signal conditioning elements, to make a useful device. The device, the TSL250 light-to-voltage

converter, solves some basic application needs. It is particularly suitable for analogue measurement of low light levels in an electrically noisy environment.

In the TSL250, a large area photodiode is combined with a transimpedance amplifier, so the photodiode current output is converted to an output voltage.

Three versions of the device are produced, with different photodiode areas, and internal feedback resistor values.

2.1.2. Sensitivity Variants

TSL250gives 2V output for 25 microwatts/cm^2

TSL251 " " for 60 microwatts/cm^2

TSL252 " " for 425 microwatts/cm^2

To get some idea of what these incident light levels mean, we can consider a photometric equivalence (for visible radiation) of **90 lux = 14 microwatts/cm^2.**

Dusk, when street lights are turned on , is about 70 lux. The TSL250 gives 2V output at 150 lux. Office lighting at a work surface is typically 300-400 lux, where a TSL251 would give 2V output. The TSL252 would give 2V output in outdoor daylight illumination.

2.1.3. Application

The TLS250 family is appropriate for a wide range of light sensing applications in light level control over a wide range of light levels, for security aplications, and for boiler flame control in gas or oil heaters.

2.1.4. Characteristics

The LinCMOS (TM) transimpedance amplifier (like the well-established Texas Instruments operational amplifier TLC272) provides stable low input offset. The TSL250 offers high dynamic range, with linear output up to 3V, with only 3 mV output in the dark.

The TSL250 has a significant advantage over discrete photodiode light sensors under low illumination, since the high impedance output node of the diode is internal to the device. This makes the TSL250 inherently less sensitive to external electrical noise, so a highly stable sensitive detector can be realised without expensive and cumbersome screening techniques. Similarly the TSL250 is inherently less prone to current leakage problems in detector circuit assemblies.

In summary, the TSL250 family has a highly linear, stable, low-impedance voltage output. The TSL250 output is stable with temperature, changing by 1 microvolt per degree Celsius. This is because the temperature coefficient of the polycrystalline silicon feedback resistor compensates the temperature coefficient of the photodiode.

The TSL250 operates off a single supply voltage (it is characterised at VDD= 5V , but will operate between 3V and 9V), and consumes little current (800 microamps at VDD=5V when illuminated).

The TSL250 family is offered in a high-volume clear plastic sidelooker package.

2.2. TSL250 Output Characteristics.

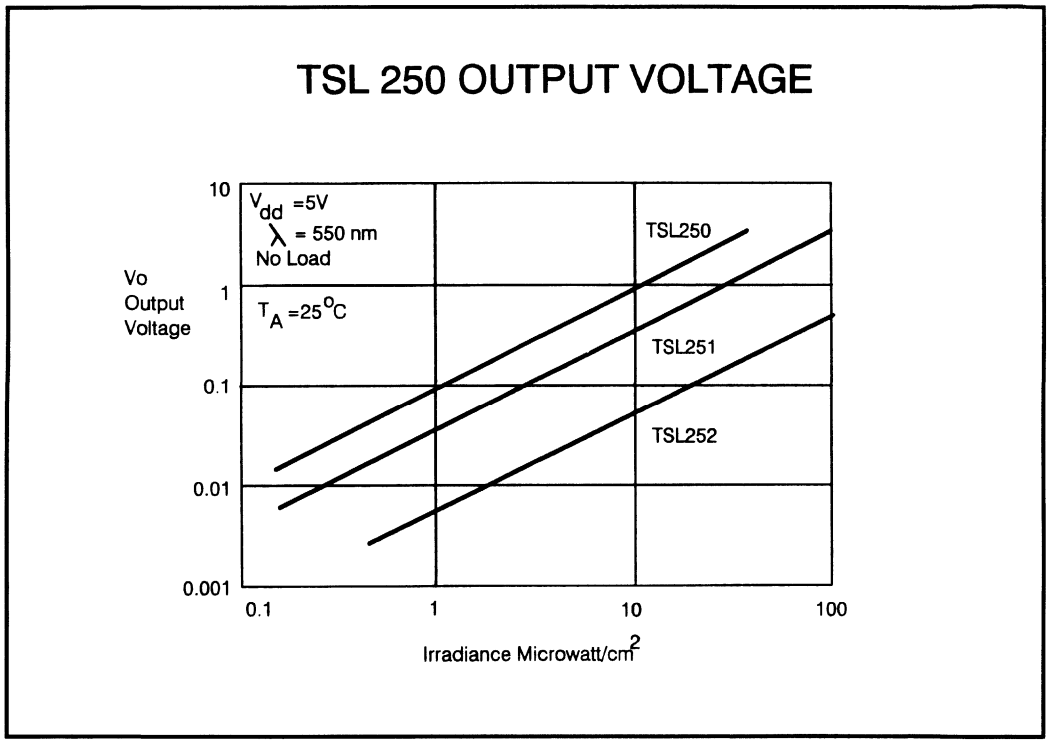


Figure 5.6 - TSL250 OUTPUT CHARACTERISTICS.

2.2.1. Speed vs Responsivity

Figure 6 shows the linear output characterisitcs of the TSL250, TSL251 and TSL252. The internal feedback increases from the TSL252 to the TSL250. As the feedback is increased the speed is reduced. The TSL252 output rise and fall times are typically 7 microseconds, for the TSL251 they increase to 90 microseconds, and for the TSL250 they are 360 microseconds. The basic design could be extended to higher speed operation, trading responsivity for speed, by reducing the diode area and the feedback resistor and capacitor values -- the extremely low dark voltage resulting from the LinCMOS (TM) technology would permit this.

3. TSL220 Light-To-Frequency Converter

3.1. The TSL220 Device

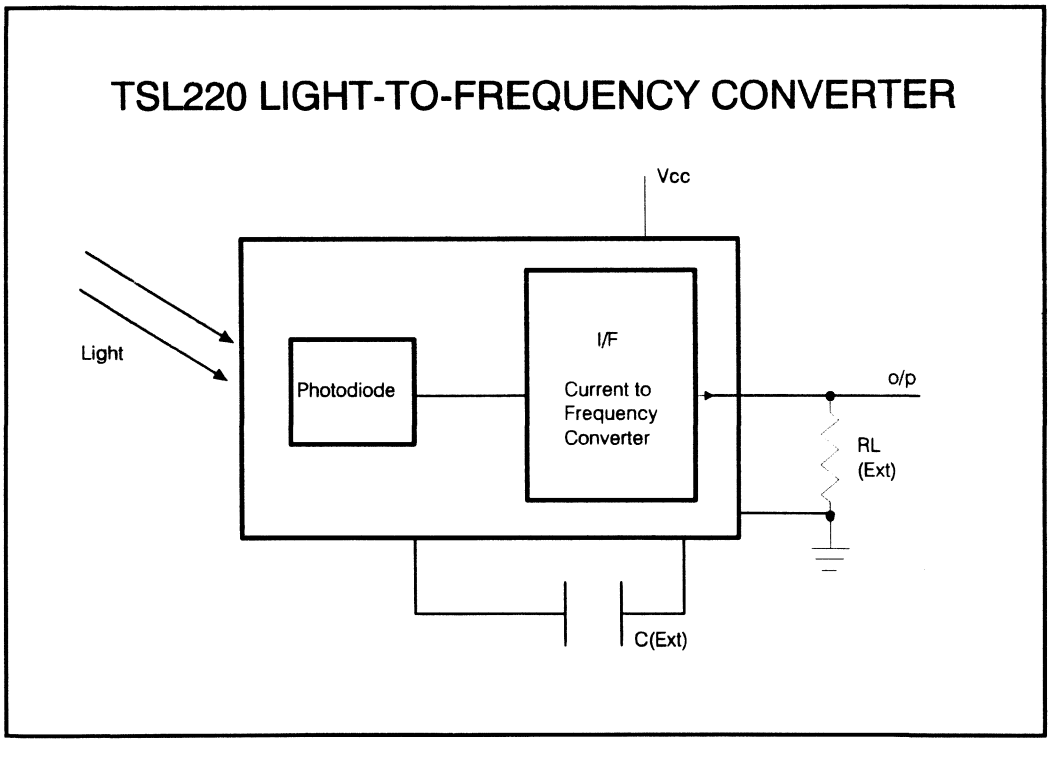


Figure 5.7 - TSL220 LIGHT-TO-FREQUENCY CONVERTER

3.1.1. Summary

In this section we describe how the process of developing an Intelligent Opto Sensor is carried a step further in the TSL220. The TSL220 is a light-to-frequency converter, and combines a large area photodiode with a patented light-to-frequency converter to provide an output that is very convenient for a microcomputer,or indeed any digital technique, to handle.

3.1.2. Characteristics

The output of the TSL220 consists of a train of 4-volt pulses, the output frequency being proportional, over a wide range , to the intensity of the light incident on the photodiode surface. The TSL220 is extremely linear from 1Hz to 1MHz, and has an extremely high dynamic range -- under office illumination the output frequency is typically 150 KHz, while in the dark the frequency is typically 1 Hz !

The TSL220 operates off a single supply voltage (guaranteed performance at 5V, operable between 4 and 10 volts) , and the output is CMOS compatible. TheTSL220 is offered in a high volume clear plastic 8-pin dual-in-line package.

3.1.3. Application

The TSL220 is very suitable for precise measurement of light level. Since one can measure how much of the photodiode area is covered, the TSL220 can also be used as a precision (0.2 micron) analogue edge sensor.

The form of the output is very easy to handle, as pulses can be easily counted over a measured time set by a clock circuit.

The TLS220 is thus particularly suitable for applications where precision light or position measurement forms parts of a micropocessor- or digital- control system. Such applications include light metering, mechanical registration, printer paper positioning, smoke and dust detection, vibration detection, and coin control.

3.2. TSL220 Output

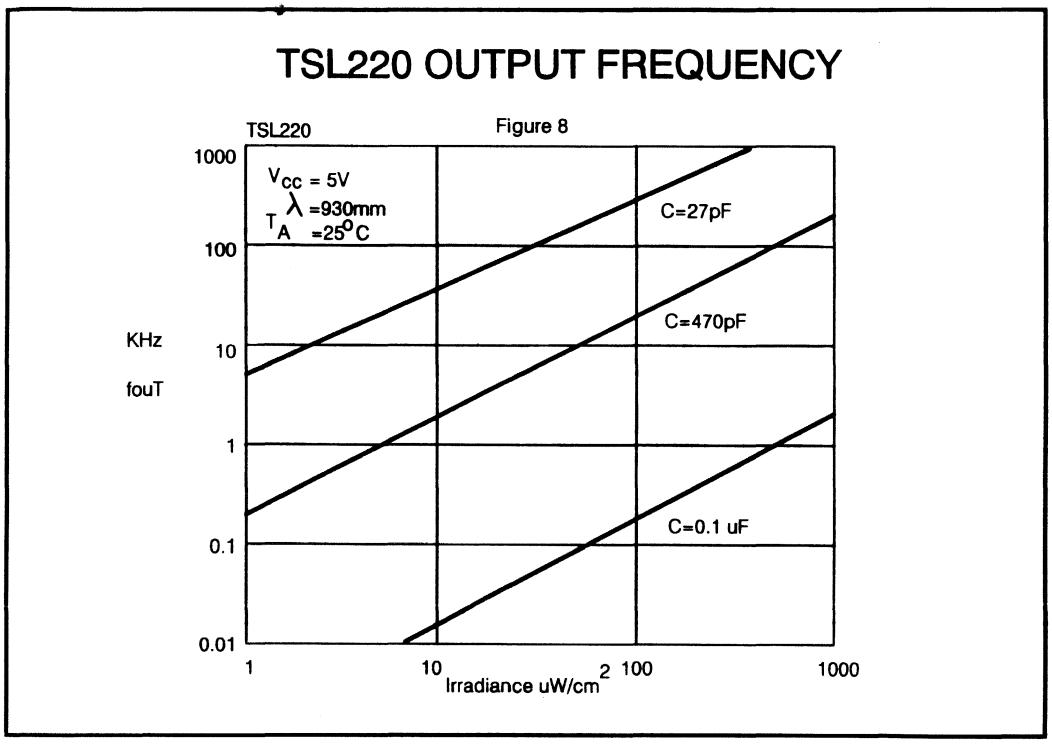


Figure 5.8 - TSL220 OUTPUT

3.2.1. Frequency Adjust

Many low cost digital and microprocessor techniques are not capable of being run at the high output frequencyrates of which the TSL220 is capable. The frequency range of the TSL220 can be adjusted bymeans of a single external capacitor.

3.3. TSL220 Light Metering Using A Programmable Microcontroller

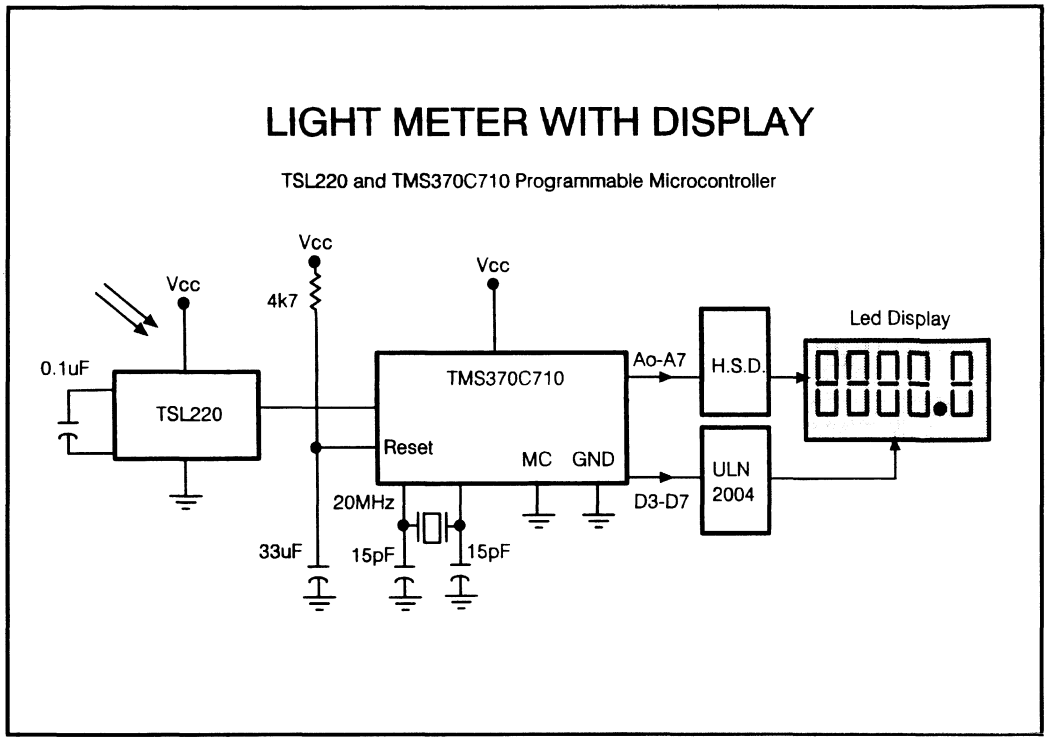


Figure 5.9 - TSL220 LIGHT METERING USING A PROGRAMMABLE MICROCONTROLLER

3.3.1. Summary

Many simple application examples of the use of the TSL220 are given in the data sheet. A further example of the ease with which the TSL220 output can be handled by a microcomputer is given in Figure 5.9

In this example thelow-cost Texas Instruments field programmable 8-bit microcontroller TMS370C710 is used.

TheTMS370C710 features 4k bytes of program EPROM, 256 bytes RAM, 256 bytes data EPROM, a 16-bit timer and an on-chip watchdog for system integrity. It is supplied in a low cost 28-pin PLCC package.

3.3.2. Schematic

In this example of a calibrated light-(lux-)meter, the pulse train from the TSL220 is fed directly to the Timer 1 input capture pin of the microcontroller. A 20MHz crystal is supplied to the microcontroller, and the external capacitor of the TSL220 is set to 0.1 microfarad. The timer prescale is set to 2ee18 (/4) , giving a 16 bit overflow at 0.052 seconds.

70 lux (20Hz) resolution is 15 bits, and at 3000 lux (1kHz) resolution is 10 bits.

The 5 digit multiplexed LED display is driven by the microcontroller. Spare CPU power of the microcontroller would allow lux level to be directly displayed and film speed to be entered. Calibration parameters can be stored in EEPROM to make use of the high resolution. A 5 x 3 user keypad can be attached to the system, and strobed using interrupts 1, 2, 3 and the 5 remaining spare I/O's.

4. TSL214 64-Pixel Array

4.1. TSL214 Functional Block Diagram

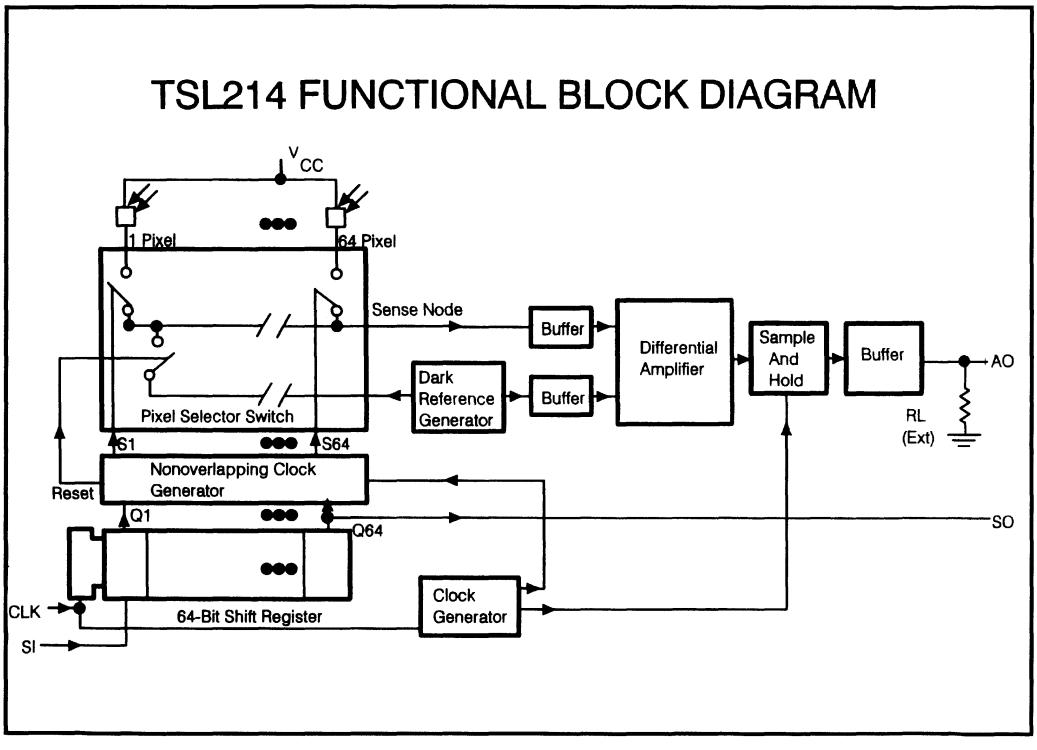


Figure 5.10 - TSL214 FUNCTIONAL BLOCK DIAGRAM

4.1.1. Summary

The TSL214 array illustrates how a complex sensor, which integrates light-sensing , analogue and digital elements, can offer the prospects of low system cost, and ease of design.

The TSL214 is a 64-element line sensor, fabricated from the established Texas Instruments LinCMOS(TM) mixed-mode volume wafer technology. The pixels have a 125 micrometre centre-to-centre spacing. The TSL214 is a charge-mode sensor. That is, during an exposure period , a charge is developed on each pixel proportional to the product of the light intensity and the exposure time. (In this it is like a CCD imager, and analogous to photographic film).

On a single TSL214 die are integrated the light-sensing pixels, analogue signal conditioning, and digital address and switch elements (equivalent to approximately 2500 gates).

The internal complexity of the die has been chosen, to make the device easy to use in a microprocessor or digital processing system environment. To operate the TSL214, only a single 5V supply and integration (exposure) and pixel output clock pulses are required.

4.1.2. Characteristics

The TSL214 operates at data rates between 10kHz and 500kHz. The relatively large pixel size permits assembly in a high volume low cost 14-pin plastic dual-in-line package.

The TSL214 is recommended as a real alternative to either discrete photosensor arrays or to CCD line imagers in sensing systems where more than one sensor is required, and the sensors form part of a digital control system. Typically the pixel size in a line CCD imager is 10 microns, and for a discrete photodiode or phototransistor is 1000 microns. At 125 microns pixel size, the TSL214 is appropriate for many applications.

4.1.3. Function Blocks

The functional structure of the TSL214 is shown in Figure 10. There are 64 pixels in a line array, which are addressed individually (unlike CCD where all pixel charges are switched along an analogue register simultaneously).

The exposure or integration period is defined as the time between clock pulses on the Serial Input (SI) pin. The integration period is chosen in each application to give a suitable output level for the light intensity available.

The charge in each pixel is transferred to the output sense node by means of the Clock Pulse (CLK). The sense node generates a signal voltage directly proportional to the charge.

A 64-bit shift register controls the transfer of charges to the output and provides timing signals for the non-overlapping clock generator (NOCG). The NOCG provides internal control for the sensor elements , including charge sensing and reset. The reset establishes a known voltage at the sense node in preparation for the next pixel charge transfer. This voltage is used as a dark reference level for the differential signal amplifier.By means of the NOCG, feedthrough clock noise is eliminated at the output. The sample-and-hold signal generated by the NOCG holds the voltage analogue output of each pixel constant until the next pixel is clocked out.

4.2. TSL214 Timing Diagram

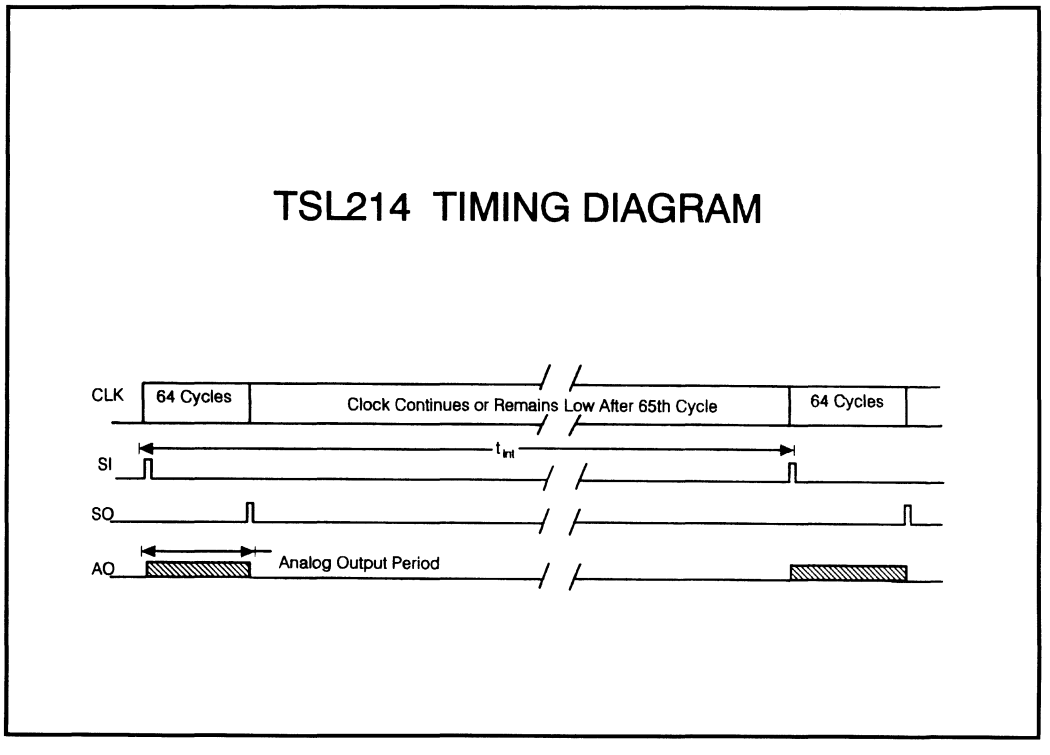


Figure 5.11 - TSL214 TIMING DIAGRAM

4.2.1. Combination Of Arrays

The architecture of the TSL214 enables more than one array or die to be connected in series or parallel configuration. Thus a 128 pixel device (TSL215) and a 192 pixel device (TSL216) may be easily created. The 64 pixels of the TSL214 die are in groups of 8 pixels; the outputs of different groups may be balanced by means of resistors which can be fused to one of 5 levels at multiprobe. This enables long uniform arrays of pixels to be realised -- practical 1728 pixel 200 dpi A4 facsimile contact sensors can be made by serial connection of TSL214 dice.

4.2.2. Serial Connection

For serial connection, the Analogue Outputs (AO) must be connected together and the Serial Output (SO) of each sensor array connected to the Serial Input (SI) of the next array. The externally applied SI pulse is applied only to the first array of the series. For n arrays in cascade the SI pulse is applied after each n x 64 positive going clock transitions.

4.2.3. Parallel operation

Parallel operation of multiple arrays is achieved by supplying clock and SI pulses simultaneously. The outputs of each device may then be processed separately.

4.2.4. Initialization

At power up, or after a period of SI or readout clock inactivity exceeding the integration time, the sensor elements may need to be initialised. This consists of 15 consecutively performed output cycles to clear the pixels of any charge which has accumulated during the inactive period.

4.3. TSL215/TC102 Comparison

COMPARISON OF 128 PIXEL IMAGERS

	TSL215 (Addressed Array)	TC102 (CCD Imager)
Pitch Speed	125Micrometer 1MHz o/p data	12.7 Micrometer 10MHz o/p data
Input	5V digital supply, integration & readout clocks	+2V, -16V clock +16V VDD, +7V REF. Needs mos-drivers (Ext.)
Readout	Pixels individually addressed	All pixel charges simultaneously moved
Output Conditioning	Analog video output	Needs video clamp, external sample/hold to remove clock noise.

Figure 5.12 - TSL215/TC102 COMPARISON

4.3.1. Summary

Two TSL214 dice may be combined serially within a single device to make the TSL215 128-pixel line sensor array. The TSL215 is here compared with a 128-pixel CCD line array , the TC102.

4.3.2. Pixel Size

The most obvious difference is that the active optical length of the TSL215 is almost 10 times that of the TC102. The TC102 is a CCD array where all the pixel charges of an integration period are clocked out together down transport registers, while the TSL215 is an addressed array where pixel charges are individually switched out. The coarser pitch of the TSL215 derives from the physical size of the switching elements (including the NOCG) associated with each individual pixel. For the standard LinCMOS(TM) technology the relatively fine optical resolution of the CCD cannot be realised.

4.3.3. Data Rate

The maximum data output rate of the TSL215 has been set by the switching design at 1 MHz, whereas with careful driver circuit design the TC102 can deliver data out at up to 10MHz. However, the TSL215 is far simpler and more economical to drive, and its output is more easily handled.

4.3.4. Drive Requirement

The TSL215 drive requirement is a single 5V supply, an integration pulse and a output clock . The TC102, however, requires positive (+2V) and negative (-16V) clock pulses, +16V VDD, and a 7V reference. The registers must be driven through a dual MOS-driver such as the TLD369.

4.3.5. Output Requirement

The output of the TSL215 is also much more convenient , being an analogue video envelope. With the TC102, the analogue voltage levels of the video pixels are offset by the output buffer amplifier, and must be externally clamped to a video black reference using a train of black reference pixels provided. External sample-and-hold must be done on the clamped voltage output, to eliminate the clock feedthrough noise between the valid pixel levels.

4.3.6. Cost

These input and output tasks with the CCD device make it much more expensive in a system, on top of the higher cost of the CCD device itself. (One advantage of the relatively coarse pixels is that a low cost plastic packaging technique may be used). For applications where arrays of discrete photosensors, or low resolution CCD were hitherto used, the TSL214/TSL215 provides an attractive alternative.

4.4. PC404 Evaluation System

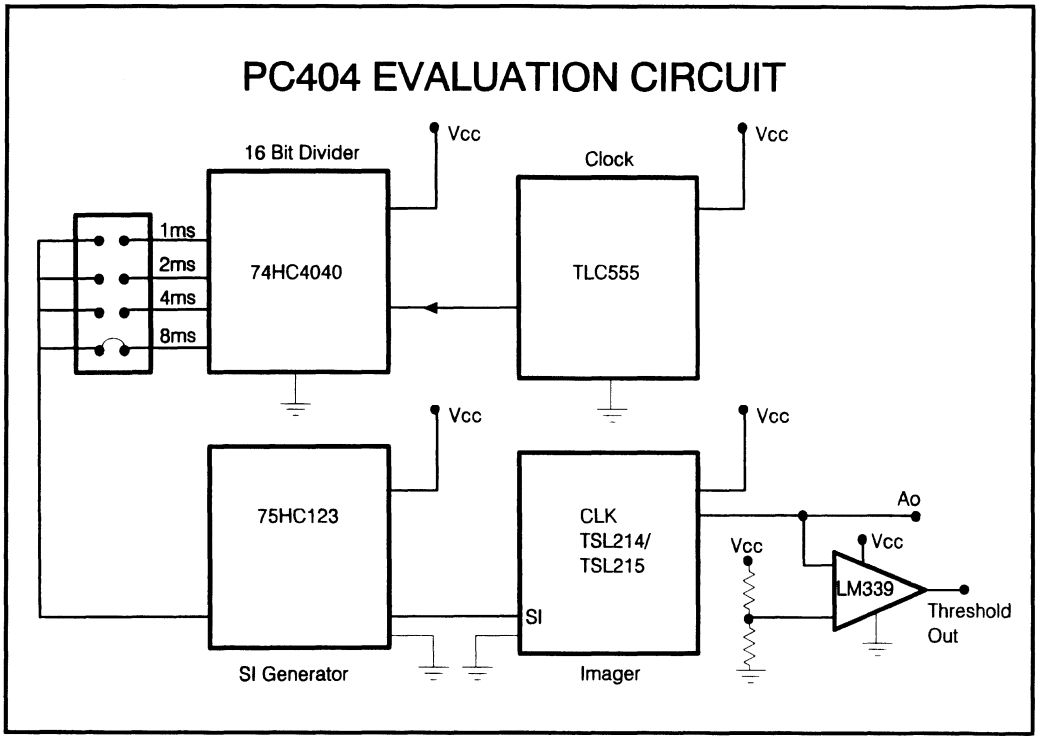


Figure 5.13 - PC404 EVALUATION SYSTEM

An evaluation kit, PC404, is available to facilitate initial evaluation of the TSL214 64-pixel integrated array.

4.4.1. Schematic

The PC404 consists of a TSL214, a circuit board with drive and output circuitry, and a detachable 10 x magnification lens in a housing. The circuitry of the PC404 comprises an oscillator, a counter/divider, a one-shot pulse generator and a comparator. The oscillator is built round a TLC555 timer and generates a 500kHz output data clock pulse. the clock output of the oscillator is routed also to a 74HC4040 divider. This has a set of jumper terminals to four of the outputs, and 1ms, 2ms, 4ms or 8ms Integration Time may be selected. The chosen output is connected to the 75HC123 one-shot pulse generator, which provides the TSL214 with the SI pulse.

Trimming potentiometers and test points are provided. Two alternative outputs are provided. One is the Analogue Output (AO); for the other - Threshold Out - the AO is routed to an LM339 comparator, which squares up the output for digital compatibility.

4.5. Absolute Rotary Encoder Using TSL214 - Mechanical Layout

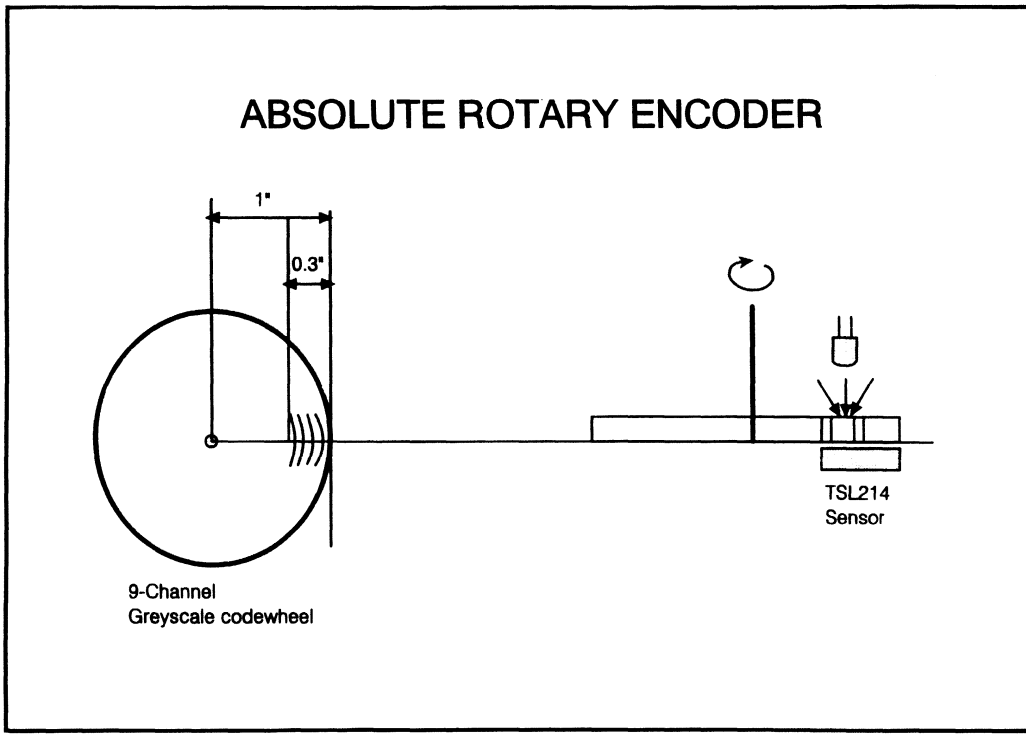


Figure 5.14 - ABSOLUTE ROTARY ENCODER USING TSL214 - MECHANICAL LAYOUT

The ease with which the TSL214 can be used to provide an input to a microprocessor system , can be illustrated in an example of an absolute rotary encoder, such as may be used to feed a panel setting position to a process control system.

4.5.1. Layout

In this simple illustration each sector of the wheel is defined by a unique grey-scale code. For each of 360 degrees to be read out, 9 coding channels are required. (2EE9 = 512). The 9 channels occupy 0.32 " of the radius of the wheel (see Figure 14). The TSL214 is positioned along a radius so that the 9 channels pass over the sensing area. The coding mask is printed on a clear coding wheel.

4.5.2. Sensor

The TSL214 consists of 64 pixels. The sensing length is divided into 9 groups of 7 pixels , corresponding to the 9 channels of the coding wheel. The 7 pixels consist of two unused pixels at start and finish, with 3 active pixels in the centre (This sets very loose alignment requirements in this simple demonstration). The code, 0 or 1, for each channel is set as the value taken by 2 of the 3 active pixels.

Each degree of the circumference of the wheel will generate a unique positional code, which can be decoded by a microprocessor, and displayed on a group of three LED displays.

4.6. Absolute Rotary Encoder Using TSL214 -- Electrical Layout

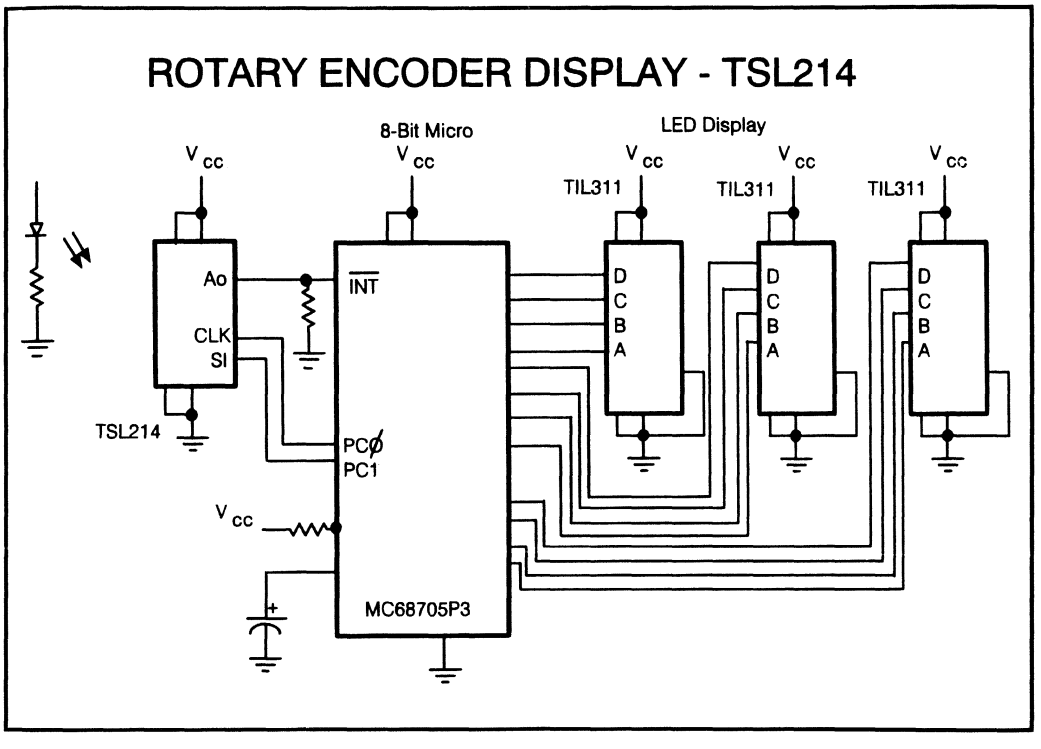


Figure 5.15 - ABSOLUTE ROTARY ENCODER USING TSL214 -- ELECTRICAL LAYOUT

4.6.1. Summary

The electrical realisation the the rotary encoder described above, is extremely simple. A MC68705P3 8-bit microprocessor is programmed to provide the SI and CLK pulses directly. The Analogue Output (AO) of the TSL214 is fed directly to the Interrupt line of the microprocessor. The decoded rotary position of the wheel is the directly fed from the microprocessor to three TIL311 visible LED displays.

Section 6
Lighting Products

Section Contributions by:

Mick Maytum
Ross Hugo

Contents
Section 6.

1. Introduction

1.1. Section Overview

The following section focuses on a range of power products for fluorescent lighting applications.

50-60 Hz fluorescent lighting has been extensively used in industrial and commercial environments for many years now. Compared with conventional incandescent bulbs, fluorescent lamps offer many advantages including lower energy consumption and longer life for the same light output. With these benefits it is hardly surprising fluorescent lighting has become prevalent in the above mentioned environments. On the other hand, due to their size, the need for extra control gear and the higher initial cost, they have not yet achieved extensive penetration of the domestic market. However, all this is now beginning to change.

In the last decade, advances in power semiconductor technology and the desire to produce cheaper and more efficient lighting sources has led to many innovations to both further improve fluorescent lighting and to replace household incandescent lighting. Many new products, such as semi-intelligent starters and higher efficiency ballasts have begun to penetrate the market. An additional influence, becoming more important by the day, is that of the Green Effect. The concern for the environment and the desire to conserve the earth's resources has intensified the drive towards more energy efficient lighting and enabled the producers to look further afield to new market opportunities. All of these combined, has led to the rapid introduction of semiconductors into lighting systems in recent years and produced a market enjoying sustained growth for these new products.

Texas Instruments has been a leading supplier of power products for many years and now offers a range of products specifically targeted to the fluorescent lighting market. The following pages will look at two of these high growth areas, namely the electronic starter for 50 Hz fluorescent lamps and the high frequency electronic ballast. The latter can be further sub-divided into standard high frequency ballasts used to control the conventional 2 to 8 foot linear lamps and compact fluorescent ballasts recently introduced to replace the incandescent light bulb.

Emphasis will be placed on giving the reader a brief overview of the systems, what benefits can be attained, what are the key design constraints and finally, a look at Texas Instruments product offerings and their key characteristics and benefits.

2. Fluorescent lamp starters

2.1. Overview

The control gear of any fluorescent lighting fitting provides two functions for the fluorescent tube, namely control and tube striking. In the running condition the gear provides a ballast function (series impedance from the supply source) to stabilise the electrical discharge in the gas. Under 50 Hz ac conditions, the voltage across the tube is approximately a square wave, which can range between 40 V and 200 V depending on tube type and length. The voltage difference between the sinusoidal supply voltage and the "square" tube running voltage is thus developed across the ballast. In ac applications, an inductive ballast or choke performs this function with relatively little loss, although the lagging current often necessitates using a further capacitor to ensure a unity power factor.

The gear must also provide the correct sequence and conditions for starting the discharge. Normally, the tube cathode will be heated for a period in order to produce electrons for easy starting. This is termed "preheating" time. Then a sufficiently high voltage must be applied to initiate the discharge, this operation being termed "striking."

The simple series arrangement of a ballast and tube across the ac supply is possible when the maximum tube running voltage is below 60% of the peak supply voltage. Higher running voltages would create an unstable discharge condition. The tube running voltage strongly depends on the tube length. Thus in Britain (240 V ac), tubes of 6 and 8 feet are common, whilst in the rest of Europe (220 V ac), the limit tends to be 5 feet. In countries where 110 V ac is used, such a series arrangement would severely limit tube length. As a result, control gear in these countries often incorporate a step-up auto transformer to boost the supply voltage.

2.2. Fluorescent lamp starters

Figure 6.1 shows the glow switch start configuration, which represents the lowest cost control gear system. The glow switch comprises a glass tube filled with a mixture of gases, such as helium and hydrogen, in which is mounted a contact pair. One of the contacts is fixed and the other is mounted on the free end of a moveable bimetallic strip.

When power is first supplied to the terminals, the full ac voltage is applied to the glow switch, which starts a glow discharge in the gases (the ballast reactance limits the maximum current). After a short period, the heat from the discharge causes the bimetallic strip to bend, closing the contacts. This shorts out the discharge and starts the cathode preheating. A heavy current, limited mainly by the ballast reactance, flows through a series circuit composed of the ballast, tube upper cathode heater, closed glow switch contacts and the tube lower cathode heater. This condition continues until the bimetallic strip cools sufficiently to separate the contacts. The random nature of the contact opening means that current will normally be flowing at the instant of opening. Interrupting the current flow results in a back electromotive force (EMF) spike from the ballast inductance which, if large enough, will initiate a discharge in the fluorescent tube. If the generated voltage spike is not sufficient to strike the tube, the glow switch cycle repeats until the tube does eventually strike.

The gas reaction time of the fluorescent tube is faster than the glow switch. Thus, during striking, the glow switch does not limit the voltage applied to the fluorescent tube. When the fluorescent tube is running, its discharge voltage is lower than the level necessary to activate the glow switch. Hence, tube running prevents further operation of the glow switch. The glow switch circuit shown in figure 6.1 is for a "lagging" ballast. To improve efficiency further, power factor correction has to be introduced and this can be achieved via a shunt capacitor connected across the supply terminals.

The virtues of the glow switch are simplicity and low cost. However, several problems arise from its electromechanical nature. The first is that its random operation relative to the supply conditions means that several pulses may be necessary to strike the fluorescent tube. This not only serves to reduce the lifetime of the tube but can be extremely annoying, particularly in environments where the light source is continually switched on and off. Tubes nearing the end of there lifetime will continually flash as the glow switch attempts to strike the failed tube over and over again. This can be disruptive to the work environment and will require immediate replacement of tube to correct the problem.

2.3. The Fluoractor

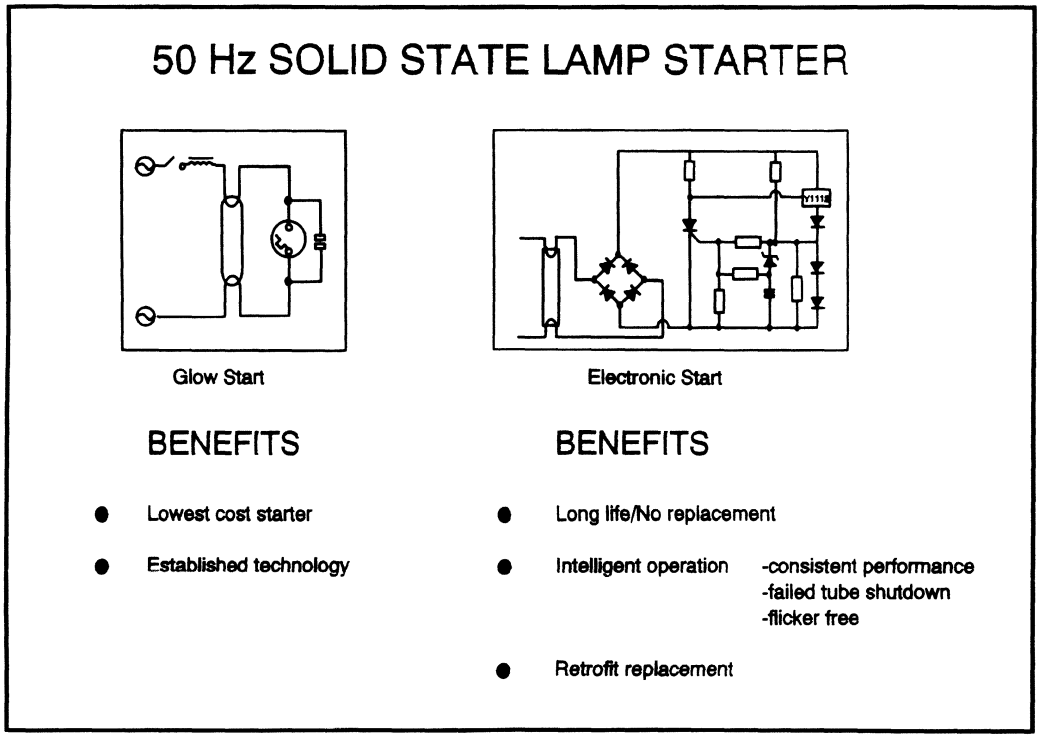


Figure 6.1 - Fluorescent lamp starters

To overcome the problems associated with the glow switch starter, Texas Instruments have introduced a solid state device, the Fluoractor^{TM} ,(Y1112), which enables the construction of a solid state starter with greatly enhanced functionality. The right hand side of figure 6.1 illustrates a typical applications circuit for this starter.

Electronic starters built around the Fluoractor allow flicker free start up of the fluorescent tube, extended tube lifetime and permanent shutdown of faulty tubes. Furthermore, it is often the glow switch itself that fails prematurely, so the extended lifetime of the electronic starter will considerably reduce maintenance costs. All of this circuitry for the Fluoractor based starter is small enough to fit into the glow switch starter canister, therefore making it a retrofit replacement requiring no redesign of existing systems.

It should be noted that the Fluoractor is a unidirectional device and requires being inside a full-wave diode bridge to become bi-directional for ac operation. When power is first applied a low level current path will supply enough current to the fluoractor gate to trigger the device into conduction. Once turn on occurs, the lamp cathode preheating period starts. During this period the Fluoractor is "on" and passing the full-wave rectified current. The ballast current, flowing through the Fluoractor cathode diodes, develops a voltage which forms the charging source for the capacitive timing network. Preheating ends and pulsing begins when the peak voltage reached at the turn off SCR gate is sufficient to cause triggering. Pulsing provides the back electromotive (EMF) spike which will strike the fluorescent tube, in this case, on the first attempt. Pulse duration is a function of zener voltage, supply voltage, choke inductance and Fluoractor holding current. At the end of the pulsing period, reached when the turn off SCR is triggered before the latched conduction in the Fluoractor is achieved, GTO action occurs. This results in the shutdown of the Fluoractor.

2.4. Fluoractor construction

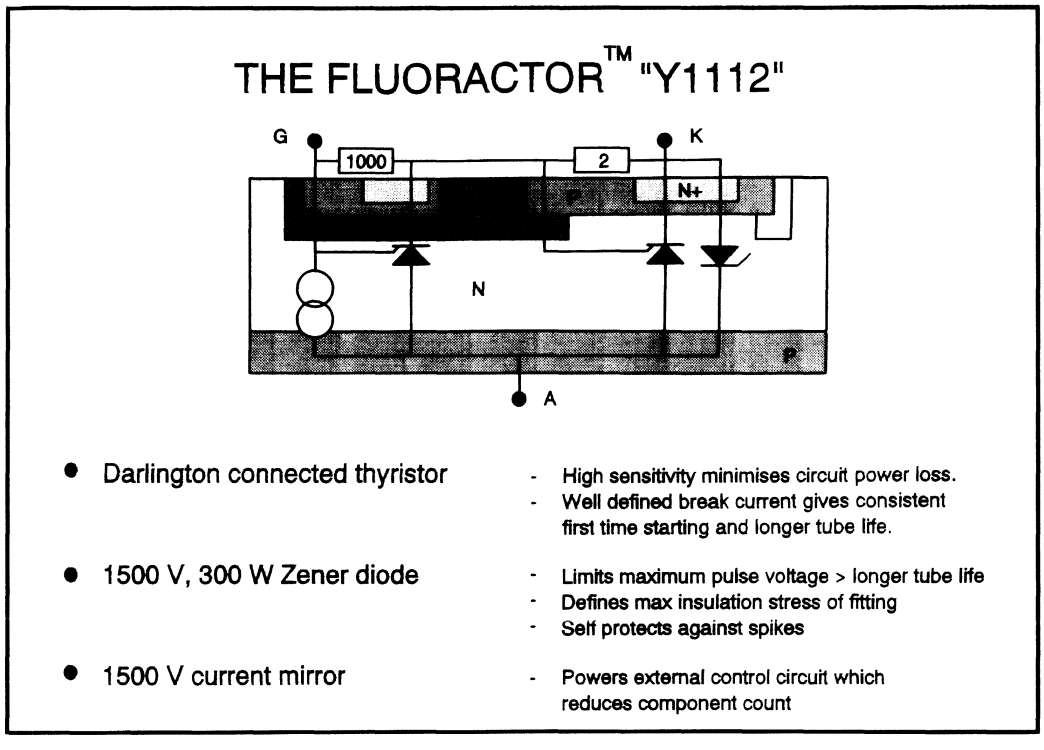


Figure 6.2 - Fluoractor construction

In order to minimise the drive power requirement, the Fluoractor is constructed using a high sensitivity darlington connected thyristor. Figure 6.2 illustrates both the device cross section and the lumped equivalent circuit of the Fluoractor. Once triggered, the Fluoractor will remain on until the anode current is reduced to a critical value called the holding current, I_H. Below the holding current, the Fluoractor will turn off unless gate drive is re-applied. The high sensitivity of the device is controlled by the 1 k ohm gate-cathode resistor of the driver thyristor section. The lumped equivalent of gate-cathode resistor of the output thyristor section is of the order of 2 ohms. This means the triggering sensitivity of this section is about 200 mA. More importantly, the holding current will be of the same order and it is this that defines the minimum switch breaking current which in turn leads to tube ignition.

The integral zener diode has a maximum voltage rating of 1500 V. This ensures sufficient volts are applied to the tube to ensure first time starting, but limits the maximum voltage seen in the circuit, therefore keeping the voltage ratings of the control circuitry down to about 1750 V.

A previously unmentioned function of the Fluoractor is the current mirror which considerably simplifies the required control circuitry. Once the Fluoractor is carrying current, a proportion of this flows out of the gate terminal. This current can be used as a power supply for the control circuit or a maintaining current if the Fluoractor is driven from an SCR type turn off device.

It is the Planar process used for the construction of the Fluoractor which allows very precise control of the holding current. This, along with the 1500 V rating of the zener are critical in determining the pulse duration. A precisely controlled pulse duration in turn leads to a soft start up with no tube flicker. An obvious benefit of soft start up is that of reduced stress on the tube cathodes and therefore, extended tube life.

A more detailed explanation of the Fluoractor, of both its construction and application can be found in the published application note. This can be obtained via the data request form included in the seminar hand out package.

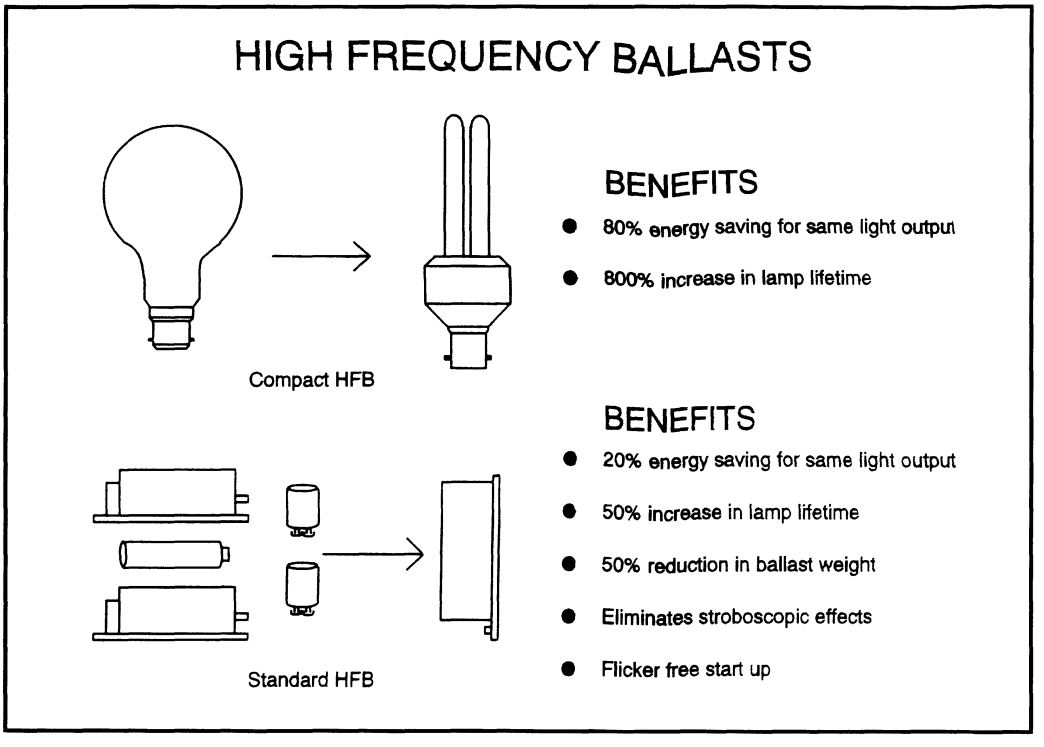
3. High Frequency Electronic Ballasts

3.1. Overview

As mentioned earlier, standard fluorescent lights are used extensively in industrial and commercial environments as a result of the many benefits they offer in terms of cost and energy consumption. Compared to a standard incandescent light bulb, 50 Hz fluorescent tubes offer the same light output for approx. one quarter of the power consumption and have longer life expectancy.

Recognising the need for smaller, lighter and more efficient forms of lighting, lamp manufacturers turned their attentions to high frequency operation of the ballast. By increasing the operating frequency of the ballast from 50 Hz to approx. 30 kHz, one is able to achieve in the region of a 20% energy saving for the same light output. Along with this very obvious financial enticement, many other benefits such as reduced weight, increased lamp life, the elimination of stroboscopic effects and flicker free start up are also achievable. It is hardly surprising then, in recent years the industry has experienced considerable growth as manufacturers vie for market share with their new product offerings.

Even newer to the market, is the relatively recent introduction of the compact fluorescent high frequency ballast. Compact meaning suitable for direct replacement of the incandescent household light bulb. Compacts can come in two forms; firstly where the ballast and fluorescent tube are combined as a single unit and secondly, where the tube is removable and consequently replaceable when it fails. These new ballast/lamp combinations offer an 80% energy saving over the incandescent light bulb for the same light output and, at the same time, are claimed to have eight limes the life expectancy.



3.2. High frequency lamp operation

Figure 6.3 - High frequency electronic ballasts

When a fluorescent lamp is running at a frequency of 50 or 60 Hz, the relatively slow rate of operation means that the conducting gas reacts faster than the ac line rate. This results in two phenomena. Firstly, when the lamp current falls to zero as the current polarity changes, the lamp stops conducting and has to restrike on the opposite current polarity. Second, is that the conducting gas has a negative impedance characteristic. To control the lamp current, the lamp must be connected in series with higher positive impedance (ballast). At ac line frequencies the ballast is usually an iron cored wound component.

When a fluorescent tube is operated at frequencies higher than a few kilohertz both these effects disappear. In this case, the lamp can be approximated to a resistive load. At these high frequencies, the persistence of the light emitting phosphor smoothes out any possible flicker. Some studies claim that the lack of flicker from high frequency operation reduces the incidence of headaches. The absence of flicker also removes the stroboscopic effects of conventional ac. line powered fluorescent lamps.

These stroboscopic effects can be highly dangerous as they can make rotating machinery appear stationary.

High frequency operation reduces the tube power required for a given light level. A 58 W, 50 Hz rated tube might only need 50 W at high frequencies to produce the same light output. At the system level the total power drawn from the ac supply might be 68 W for a 50 Hz ballast and only 55 W for a high frequency ballast. So generally an electronic ballast system draws less power than the 50 Hz equivalent.

3.3. Ballast operation

The basic function of an electronic ballast is to convert ac at line frequency to a much higher one, usually in the 30 kHz region. It is overly complex to do a direct low frequency to high frequency conversion, so normally a two stage process is used. The ac supply is first rectified to dc and then this dc is chopped at high frequency to produce the ac to power the lamp.

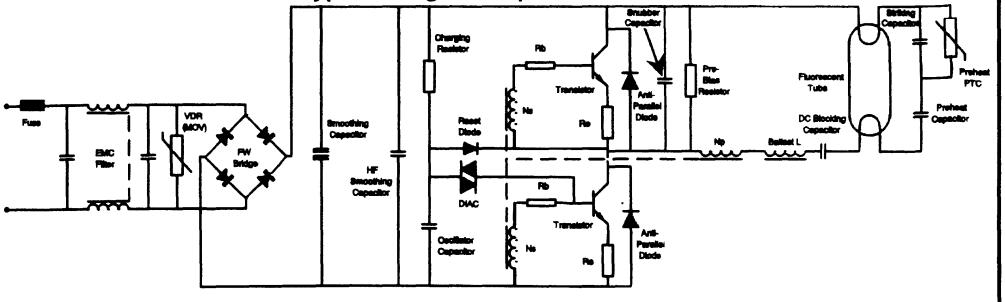
Most European electronic ballasts are based on the principle of full wave rectifying the 50 Hz ac supply to produce a dc supply voltage, V_S, in the range of 250 to 370 V. (Where a boost converter is used to provide electronic power factor correction the dc rail voltage is higher, typically in the region of 400 V.) This dc supply then feeds a half "H" bridge inverter switching at 20 to 30 kHz. The high frequency square wave then powers one or more fluorescent tubes via an LC filter network.

3.4. Transistor operation

This section looks in detail at the transistor operation. In normal operation, the transistor is expected to switch efficiently, but not turn-off the current so fast that an EMC problem is generated. These two requirements are conflicting, so the turn-off speed has to be a compromise between efficiency and possible EMC problems. Start-up and fault conditions increase the current levels and, to be reliable under these conditions, the transistor needs to has an adequate high current performance. Inverters which use the storage time of the transistor switches to determine the oscillation timing will need transistors with consistent storage times.

HIGH FREQUENCY BALLAST DESIGN CONSIDERATIONS

Typical Single Lamp Electronic Ballast



Supply Volts	240 V rail voltage	V_{CEO} > 370 V
Tube Power	Defines min current rating	2.5 A < 50 W, 4 A < 125 W
EMC	Restricts switching speed	t_{off} not too fast
Efficiency	Must minimise losses	Fast switching, low on losses
Start Up/Fault Conditions	4 X normal running current	High current gain (h_{FE})
Tube Output/Lifetime	Balanced transistor operation	h_{FE}/t_{off} matched pairs

Figure 6.4 -Ballast operation

3.5. Efficiency

Electronic ballasts are very efficient. Typically efficiencies in the 90% plus region are achieved. A ballast with 91% efficiency driving a 20 W lamp would have losses of about 2 W. Something like 0.5 W of these losses might be due to the inverter power switching transistors. This equates to a power loss of 0.25 W per transistor. It is important the characteristics of the transistors are chosen to minimise this power loss. These losses associated with the inverter transistors can be broken down into on-state and switching losses. The on-state losses are a combination of base-emitter and collector-emitter losses. Together, they constitute approx. 40% of the transistor losses, with collector-emitter accounting for two thirds of these. Switching losses account for approx. 60% of the overall losses and in particular, the 90% - 10% collector current fall time, t_{fi}, is the prime contributor to this.

It is possible to estimate the fall time switching loss, P_f, by using straight line approximations to the waveforms. The current waveform will start at a value of I_{cpk} and decrease to zero in time $1.25*t_{fi}$. Correspondingly, the voltage will start at zero and ramp at dv_r/dt during the fall time. At any instant, t, after the start, the instantaneous power, p_f, will be :-

$$p_f = I_{cpk}\left(1-\frac{t}{1.25t_{fi}}\right)\frac{dv_r}{dt}t$$

Integrating this power over the switching period and averaging at the operating frequency, f, gives:-

$$P_f = 0.26 I_{cpk} f\left(t_{fi}\right)^2 \frac{dv_r}{dt}$$

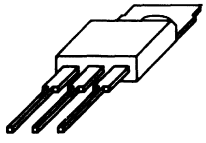
This shows that the power is proportional to the square of the fall time.

3.6. Start-up and fault conditions

In addition to normal running the transistor will also experience start-up and possibly fault conditions. Start-up can be considered a short term fault condition. Often for the start up condition, the operating transistor current is twice the normal running current until the lamp strikes. Under these conditions it is prudent to ensure the transistor has sufficient gain at twice the normal current to control the transistors' start up power loss. In the failed tube condition, the high current condition is not terminated by the tube striking. Further, when the PTC resistor switches, the circuit begins to develop much higher levels of voltage and current. If this condition persists, the transistor heating will lengthen the storage time resulting in further increases of the voltage and current. Hence, there will need to be some sort of fusing mechanism which will ultimately terminate the over load condition. More sophisticated systems will have electronic or electromechanical shut down, which will prevent damage to the circuit components.

3.7. BUL770/BUL791

HIGH FREQUENCY BALLAST TRANSISTORS



	Ballasts < 50 watts	Ballasts < 125 watts
	BUL770	BUL791
• V_{CEO} (min)	400 V	400 V
• I_C (peak)	6 A	8 A
• V_{CESAT} (max) *	0.25 V	0.3 V
• h_{FE} *	8 - 24	8 - 24
• t_{fi} (max) *	190 ns	180 ns

* Characteristics measured at typical ballast operating conditions

Figure 6.5 - BUL770/BUL791

The high voltage transistor requirements for electronic ballasts are different to those in the switching mode power supply. Recognising this, Texas Instruments have introduced the BUL770 and BUL791 specifically for electronic ballast applications. By careful analysis of electronic ballast systems and their requirements, it has been possible to develop products to satisfy these needs exactly.

These transistors have low power loss under the relatively low base turn-off current conditions typical for this application. Vcesat characteristics are specified at 0.25 V and 0.3 V for the BUL770 and BUL791 respectively (typical operating conditions). The collector current fall times of 190 ns and 180 ns ensure the optimum balance between fast switching for low loss and potential EMC problems.

Both devices have $V_{ceo's}$ of 400 V which is driven from the full wave rectification of the 50 Hz, 240 V ac. supply. Voltages of up to 370 V are often seen and where a boost converter is used to provide electronic power factor correction, the dc rail voltage is higher, typically in the region of 400 V.

Inverters which use the storage time of the transistor switches to determine the oscillation timing will need transistors with consistent storage times and high current gains. Otherwise, an unbalanced circuit will reduce light output and increase power loss. Both the BUL770 and the BUL791 have tightly controlled gains (also related to storage times) between 8 and 24 for typical circuit conditions.

The continuous collector current rating of the BUL770 is 2.5 A which makes it ideal for the compact high frequency ballast. Even though the normal operation current will only be in the region of 300mA for ballasts up to 20 W, the extra safety margin for start up and fault conditions is recommended. Similarly, for standard high frequency ballasts, up to 125 W, (where typical operating current is less than 1.5 A), the BUL791 with its 4 A continuous collector current (8 A peak) is recommended.

Hence the BUL770 and BUL791 provide ideal transistor operation for both compact fluorescent ballasts and standard ballasts up to 125 W.

Further details on Electronic Ballast operation and TI's products can be found in the recently released Application Notes available on request.

Section 7
Telecommunication Protection Circuits

Section Contributions by:

Mick Maytum
Brian Hipwood

Contents Section 7.

1. Telecommunication Protection Circuits

1.1. Section Overview

This section illustrates the need for overvoltage protection in telephone equipment and describes a range of power products specifically designed for the overvoltage protection of telecom equipment.

Lightning strikes and accidental mains voltage crossed on to the telephone line can create serious problems for modern telecommunications equipment.

Texas Instruments has introduced a range of compact dual wire bi-directional shunt overvoltage protectors with high surge current capability. This TISP (Texas Instruments Surge Protector) series of transient protectors meets the needs of new electronic exchanges, PABX, and telephone subsets. .

The TISP products are implemented using TI's high reliability ion-implanted planar process which permits precise control of electrical characteristics, extremely stable parameters, and the monolithic integration of two bi-directional overvoltage protectors in a single power package. In this way complete system shunt protection can be afforded by a single TISP device. Board packing density and layout problems are greatly improved.

1.2. The Need For Telephone Equipment Protection.

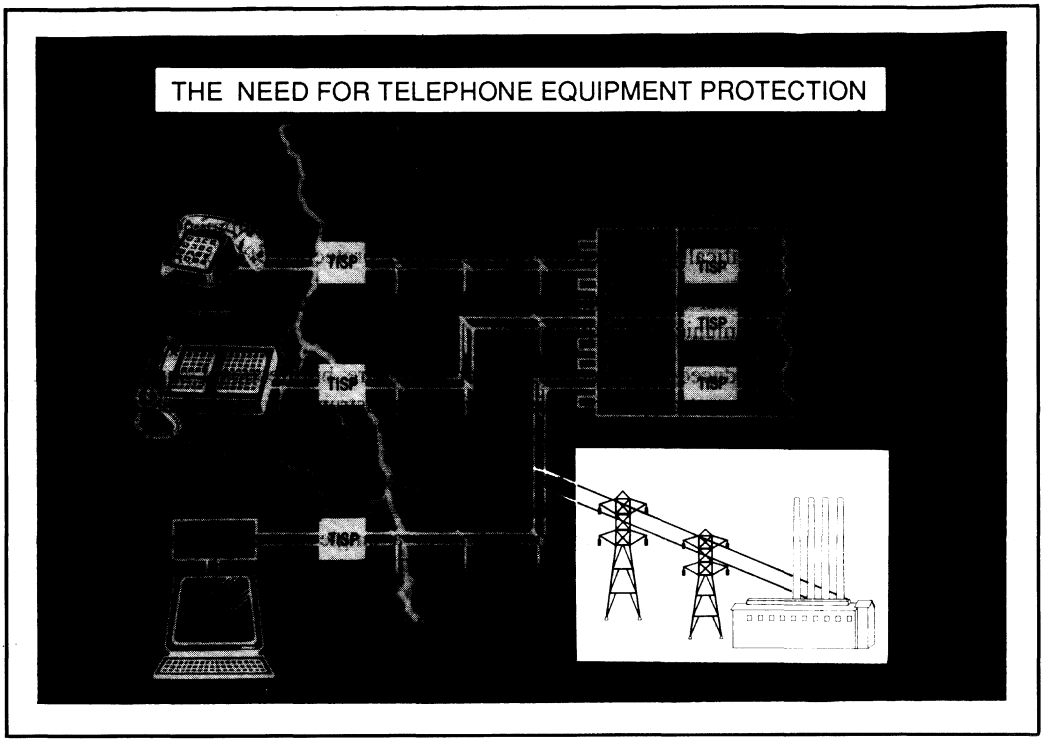


Figure 7.1 - The Need For Telephone Equipment Protection.

Disturbing voltages on the telephone line, either from direct contact or induction, can arise from lightning strikes or man made sources: the most common being AC power line. The exposed and distributed nature of the telephone network make it vulnerable to such problems and even buried cables are not immune. These disturbances are extremely difficult to quantify. As a result, each country has evolved standard tests which reflect local conditions and perceived requirements.

Generally two forms of test are specified, one set covers lightning, and the other emulates contact to AC power lines. These tests are applied between the line wires and the ground. Sometimes additional tests are made between the line wires. Most tests require the equipment to be functional afterwards, while some specify increasing the level of stress levels until equipment failure occurs. This is to ensure that the equipment fails in a safe and controlled manner under extreme conditions.

1.2.1. Lightning surge tests

Lightning is characterised by rapidly rising wave-fronts and longer decay times. A typical European test as specified in CCITT K17 specifies an artificial lightning generator circuit in which the open circuit output voltage waveform rises in 7 μs(10%-90%), initial rate 180 V/μs) and decays to 50% of its 1.5kV peak value in 730 μs. The short circuit output waveform rises in 4 μs(10%-90%, initial rate 18 A/μs) and decays to 50% of its 38 A peak value in 310 μs. In comparison, the capacitive energy of this test is over 100,000 times greater than the ESD test used to qualify CMOS 74HC logic. This enormous energy differential means that overvoltage protectors cannot be "hidden" under bond pads but require large amounts of dedicated silicon.

1.2.2. AC power line contact tests

AC power line contact tests are characterised by voltage levels up 650 V RMS, with current levels up to 10 A RMS applied either for a few cycles or continuously. Long term protection against this kind of hazard requires a series overcurrent protector such as a fuse, PTC (Positive Temperature Coefficient) resistor, or some kind of thermally activated trip. The complex interaction between the overcurrent and overvoltage protectors, together with the great variety of test specifications, has necessitated the manufacture of specialised in-house evaluation equipment, and the generation of computer simulation programmes.

1.3. Telephone Equipment Protection

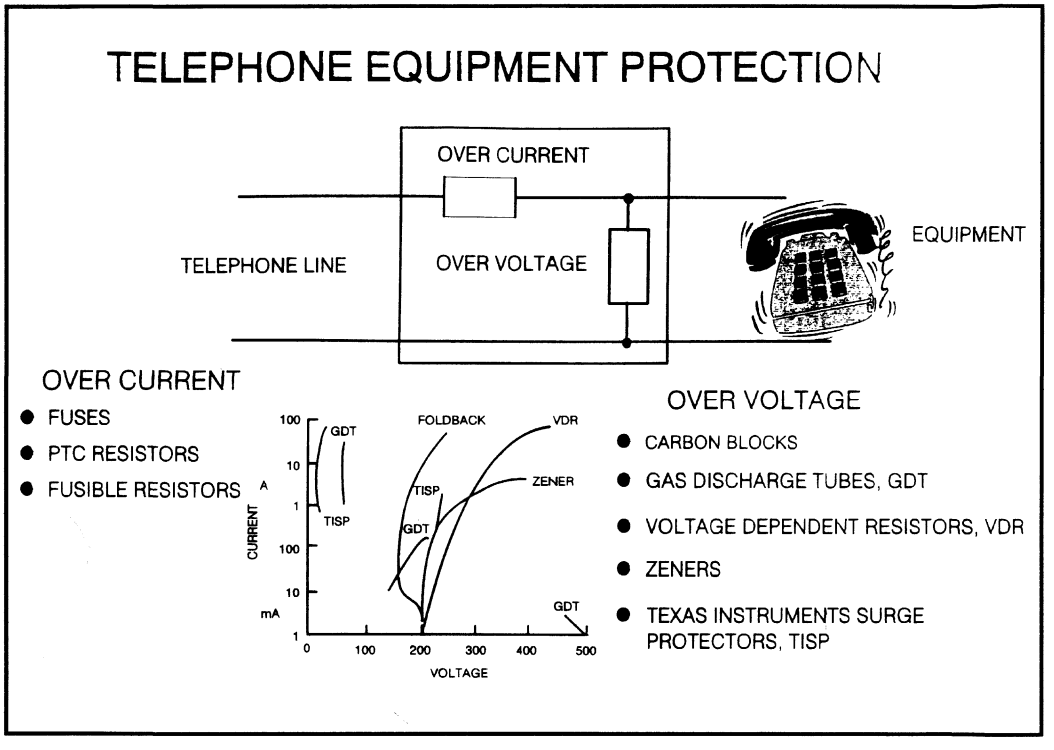


Figure 7.2 - Telephone Equipment Protection

In the protection network shown in Figure 2 the transient suppressor provides shunt overvoltage protection and the fuse, PTC (Positive Temperature Coefficient) resistor, or fuseable resistor is used for series overcurrent protection.

Overcurrent protectors "open" the line when overloaded. Fuses and fuseable resistors automatically dictate board rework after overstress. PTC thermistor based overcurrent protection systems are intended to recover once the overload is removed.

Figure 2 also compares the various types of overvoltage protectors in terms of operating principles, characteristics and pulse response. The characteristics shown are normalised to 1 mA at 200 V.

1.3.1. Zener diodes

Zener diodes for transient suppression are large area devices with special attention given to chip thermal management to absorb short term energy dumps. The zener is a very efficient clipper for short or low current level disturbances. The relatively low zener thermal capacitance results in high level transients causing large increases in junction temperature which in turn produces very large voltage increases, negating the protection.

1.3.2. Voltage Dependent Resistors

The most popular form of Voltage Dependent Resistor(VDR)/Metal-Oxide Varistor(MOV) is manufactured from zinc oxide compounds and is produced in a variety of shapes. The voltage current relationship of a VDR is given by:-

$$V = C*(I)^{\beta} + I*R_S$$

Where V = VDR voltage, I = VDR current, C = voltage coefficient, ß = non-linearity coefficient (typically 0.035), R_S = bulk ohmic resistance (typically 0.5 OHM for 10 mm disc) As the VDR does not have a sharp current initiation, like an avalanche diode, the specification point depends upon the amount of leakage current that can be tolerated. VDR's are available with a ± 10 % voltage tolerance on the voltage measured at 1 mA.

Inherently VDR clamping is inferior to that of a zener. However at high energy levels the lower thermal sensitivity of the VDR results in a better clamping voltage than a zener. A 50% increase on the 1 mA VDR voltage might be typical at these high levels. Unfortunately VDR's degrade as a result of operation which ultimately leads to a loss in protection.

1.3.3. Foldback Diodes

Foldback Diodes are not diodes but symmetrical (pnp or npn) three layer silicon structures. In transistor terms these devices conduct very little current until the voltage reaches the BV_{CEX} value. As the current increase the device voltage reduces by about 30% to follow a $BV_{CEO(SUS)}$ (type characteristic. This feature allows the foldback diode to absorb higher current surges than an equivalent area zener.

Under AC power line contact conditions, potentially destructive amounts of device power can be dissipated, without the series protection element operating.

The peak voltage level tolerance is typically about ±15%, which is better than a ±5% zener, after allowing for the zeners clamping performance.

1.3.4. Gas Discharge Tube

A Gas Discharge Tube(GDT) protector consists of a gas filled tube with an electrode at each end. At a certain voltage, gas breakdown (sparkover) occurs and the voltage falls to the medium voltage glow discharge region, which is maintained up to medium currents. Beyond this current level a high current, low voltage arc is formed, which passes very high currents (5 kA). This capability makes the GDT suitable for primary protection in an exchange main distribution frame (MDF) wiring. The low voltage conduction mode is not maintained, after the disturbance has subsided, as normal line currents are not high enough. Thus the arc is extinguished and normal operation resumes.

A major GDT problem is the reaction time of the gas to fast rising voltage wave-fronts. A GDT could initiate breakdown at 200 V DC, but delay to 500 V at 500 V/µs and 800 V at 1000 V/us. It is therefore essential that the secondary protector takes care of these high voltage edges let through by the GDT in the MDF.

1.3.5. Texas Instruments Surge Protector

The Texas Instruments Surge Protector, TISP, is based on a four layer thyristor structure. This gives a voltage triggered "crowbar", whose high holding current ensures delatching after the surge has subsided. This effectively gives a secondary protector which has the best advantages and non of the drawbacks of the Gas Discharge Tube(GDT), zener diode, Metal Oxide Varistor(MOV), and foldback diode devices.

The TISP possesses the same rapid response to fast rising voltage wavefronts as the zener, MOV or foldback diode devices. At low current levels the TISP limits the overvoltage in a manner similar to a zener protector.

Higher current levels initiate a crowbar action in the TISP. Important differences exist between the TISP and GDT crowbar characteristics. The TISP does not display an intermediate glow discharge region like the GDT, and hence any potential DC latchup problems are avoided. In addition the TISP has a much lower "on" state voltage than the GDT for the current range considered. As the current surge subsides, a current level is reached where the crowbar action terminates. Crowbar action is maintained to lower current levels with the TISP and so the remaining surge energy to be dissipated is much less.

Although not shown the TISP leakage currents are extremely low, as would be expected of a solid state device. In this respect it is similar to the zener or foldback diodes.

1.4. Exchange S.L.I.C. Protection

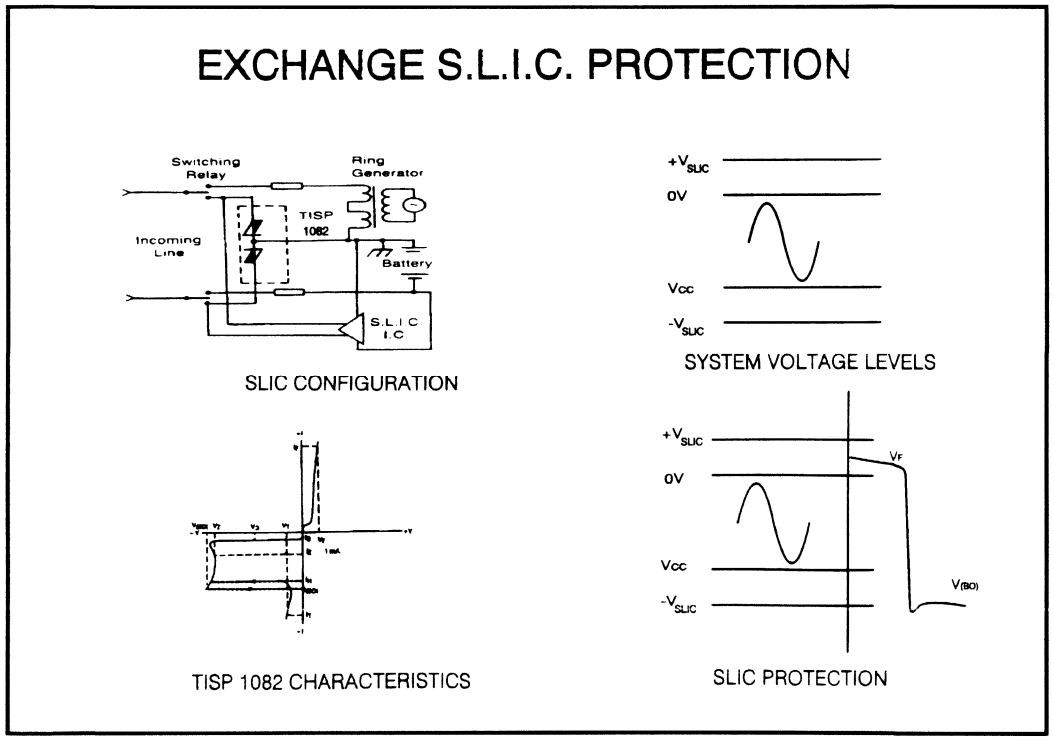


Figure 7.3 - Exchange S.L.I.C. Protection

The TISP1082 is a dual asymmetrical device in a TO220 package, to protect particular SLIC types. "Low voltage" SLICs develop their output between 0 V and -Vbat with relay isolation from the ringing voltage. Negative disturbing voltages are suppressed by voltage triggered crowbar action. In this protector the positive voltages are clipped to ground by diode action, because the usual positive voltage triggered crowbar sections have been replaced by diode sections.

1.5. Subscriber Equipment Protection

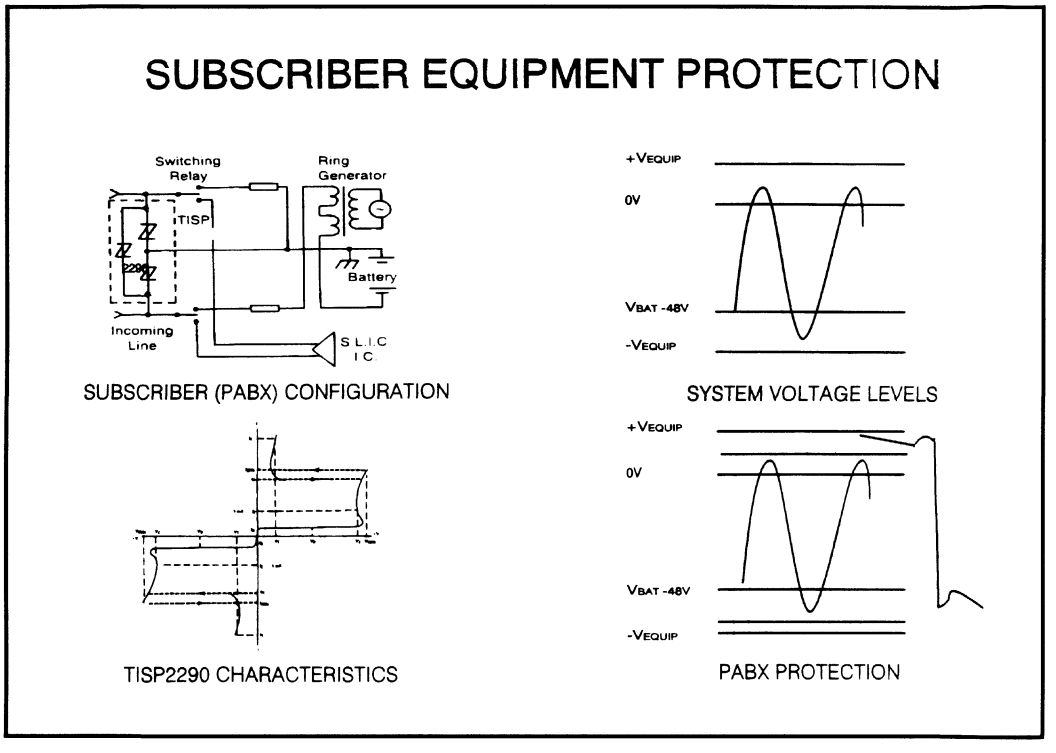


Figure 7.4 - Subscriber Equipment Protection

The TISP2290 is a triple symmetrical device in TO220 package for wire to wire and wire to ground protection, using a smaller symmetrical crowbar protector implemented between the line wires. This results in the clipping voltage being the same for wire to wire and wire to ground. A study of ringing configurations shows that this voltage condition only occurs in battery backed systems. In all other ringing configurations the wire to wire voltage exceeds the wire to ground value.

The TISP3180 is a dual symmetrical device in TO220 package, for wire to wire and wire to ground protection, in all ringing configurations.

1.6. Integrated Services Digital Network

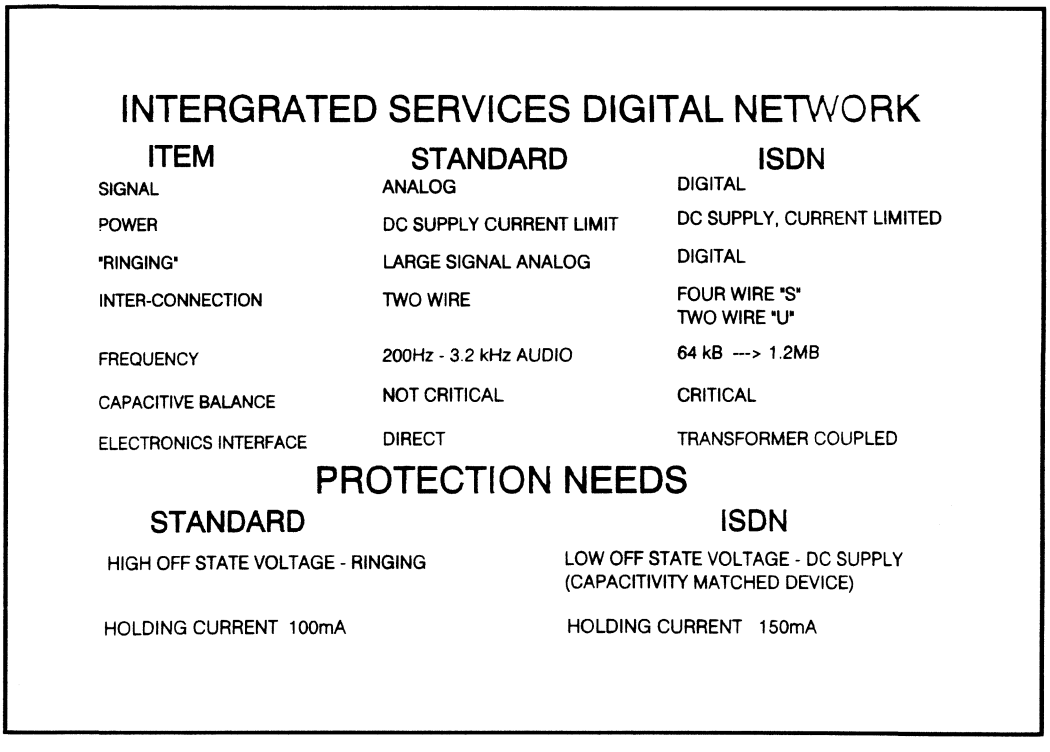


Figure 7.5 - Integrated Services Digital Network

Analogue signals are predominately used for both voice and data transmission on current subscriber lines. Modems are employed for conversion to and from the digital domain. A switching and transmission system using digital signals can have advantages to both the supplier and user of the telephone network. Digital signalling will allow the addition of new services for the user and enhanced system control and management for the supplier.

The major differences arising from the change from analogue to digital signalling are addressed in Figure 5. The change in frequency from the audio range to 64 kB and above results in line capacitive balance becoming a critical system parameter in ISDN systems.

These different system needs translate to different protector requirements. The analogue system protector needs to have a high off-state voltage due to the peak ringing voltage and a holding current of around 100 mA as defined by the SLIC short circuit line current. The ISDN system protector however

needs to have a lower off-state voltage as there is only a lower voltage DC supply. Maximum line currents tend to be higher than those present in analogue systems requiring a higher holding current. The ISDN protector must be capacitively matched between each wire to ground.

1.7. Integrated Services Digital Network Protection

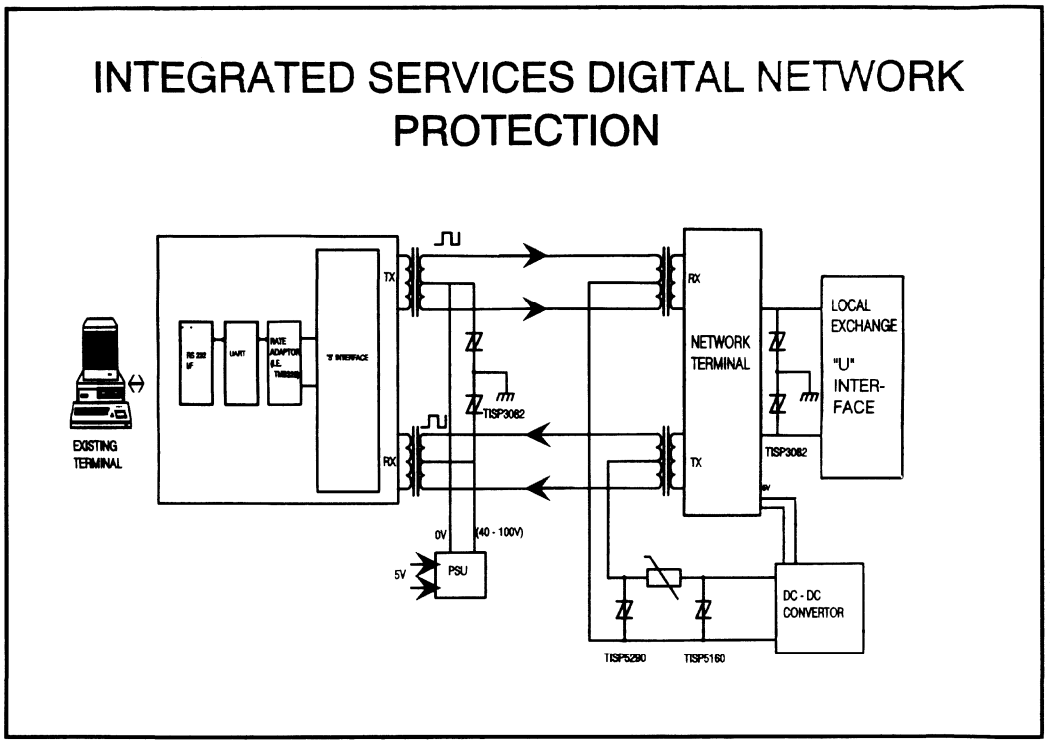


Figure 7.6 - Integrated Services Digital Network Protection

Figure 6 shows the implementation of a 4-wire "S" interface with transformer coupled transmit and receive. Additionally a 2-wire "U" interface is shown between the local exchange and the network termination.

The TISP3082 can protect both the "S" and "U" interfaces as it is a dual low voltage high holding current device in a single package. Power is fed from the network termination to the terminal equipment via the Tx and Rx wire pairs. By placing the TISP3082 protector at the transformer centre tap any capacitance unbalance effects from the protector are avoided.

This is not possible on the "U" interface as Rx and Tx functions are carried by the same two wires. The protector will add "unbalance" to the system as one of its sections is biased at around 0 V while the other section is biased at the power supply voltage. The capacitance of the low bias section will be higher than that of the higher bias section as the capacitance of the silicon junctions is a maximum at 0 V. The difference in capacitance between the two sections will determine the out off balance effect on the system. This in-balance will increase with increasing frequency. Typically the amount of capacitive unbalance introduced by the TISP3082 will be less than 120 pF.

1.8. Texas Instruments Surge Protectors

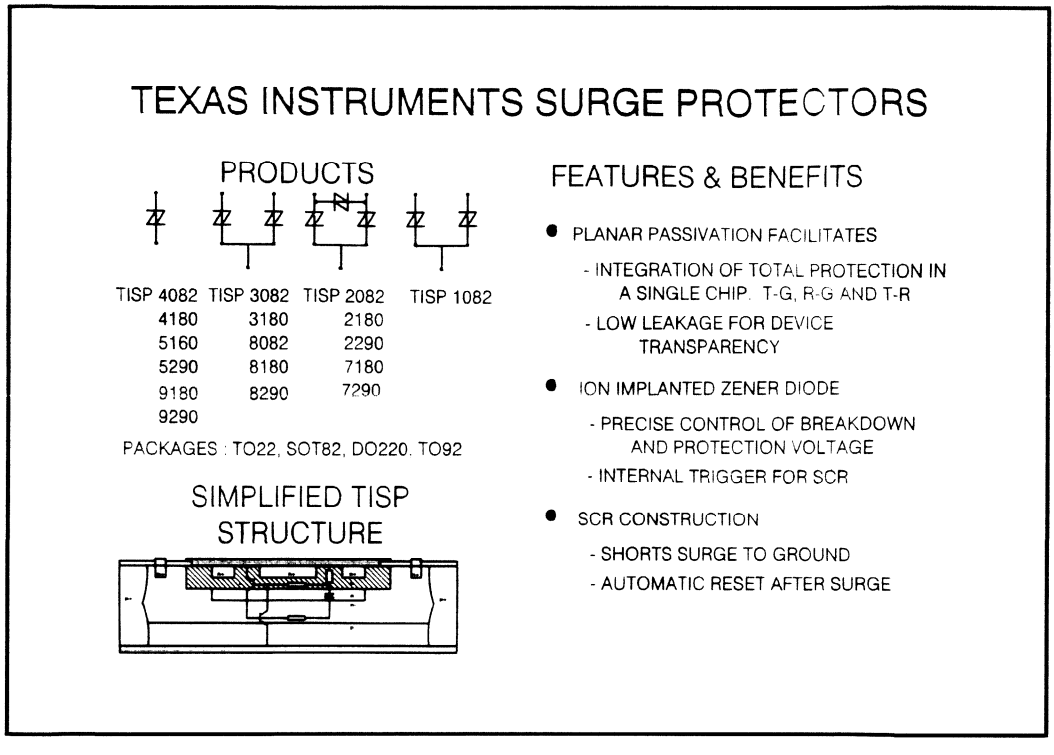


Figure 7.7 - Texas Instruments Surge Protectors

The voltage capability of the modern generation of solid state telecommunications circuits is such that they can be connected directly to the telephone line, thus saving the cost of an isolating transformer. However the voltage safety margin of these circuits is typically only 50% greater than the normal operating conditions. Very fast and precise voltage limiting is required to prevent damage from line transients caused by lightning and power line crosses. The Texas Instruments Surge Protector was designed to offer full protection to these new solid state circuits.

In the TISP, the opportunity was taken to integrate protection for both wires to ground and also between wires for both positive and negative overvoltage transients. This integration was greatly facilitated by the use of a high voltage planar passivation process which in addition to its low leakage, in the order of nA, resulting in low battery loading, also meets the 20+ year life reliability requirements demanded by the telecom industry.

The TISP uses a patented ion-implanted process to define the breakdown voltages. This is a more cost effective solution than setting voltages by selections of wafer resistivity, and gives precise control of stand-off and protection voltages.

Current flowing in the ion-implanted zener diode causes an integrated SCR to turn on and essentially shorts the surge to ground. This thyristor action allows much better silicon utilisation than standard zener diodes.

The additional advantage of the SCR is that as the surge current flowing decays, the SCR will automatically turn off when its holding current is reached.

The single chip, single package TISP is transparent to the line in normal operation, clamps the overvoltage surge by zener action, shorts the surge by SCR turn on and automatically resets when the surge decays.

Analysis of the telephone system shows that there are several fixed voltage protector configurations required for complete market coverage. This has resulted in four protector series, TISP1XXX, TISP2/7XXX, TISP3/8XXX, and TISP4/5/9XXX; where XXX is the protection voltage $V_{(BO)}$. These devices provide a complete system solution to line overvoltage protection in a single package. These protectors can be inserted into a PCB any way round. The standard pinout with line wires to the outer pins and ground to the centre pin allows for this.

The TISP family of programmable products provides the telecom system designer with a new and more precise form of overvoltage protection function. New system designs will utilise solid state relays and integrated SLICs. To make these designs a practical reality the superior protection performance given by the TISP device will become mandatory.